Agilent 81250 ParBERT Applications

Testing 10 Gbit/s Ethernet Devices

Agilent Technologies

Important Notice

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Application Overview

The purpose of this manual is to assist you when you are setting up and executing tests for 10 Gbit/s Ethernet (10GbE) devices.

The Agilent 81250 Parallel Bit Error Ratio Tester (ParBERT) allows you to stimulate such devices at data rates up to 10.8 Gbit/s and to capture and analyze the digital responses.

Focus of this manual

The focus of this manual is on testing devices that conform to the 10GBASE-R and XAUI specifications as defined in the IEEE 802.3 addendum for 10GbE (IEEE 802.3ae). These devices are electro-optical transceivers.

For testing such devices, the ParBERT User Software includes the 10Gb Ethernet Tool.

Xenpak devices

The 10Gb Ethernet Tool is particularly useful for testing transceivers that combine the 10GBASE-R PHY with an XGMII extender (PHY XGXS). Such devices are standardized and developed, for example, by the members of the Xenpak authority.

Additional software support

The ParBERT Measurement Software also greatly supports the analysis of received data. It provides tools for measuring the eye opening, timing and jitter characteristics, signal levels, and more. For details please refer to the ParBERT Measurement Software documentation.

Literature

For additional information on 10GbE devices and test methods, see also:

- *10 Gigabit Ethernet*, Agilent publication no. 5988-7260EN
- *10GbE Technology and Device Characterization*, Agilent publication no. 5988-6960EN
- *Agilent 81250 10GbE Testing with 81250 ParBERT / The 10GbE Ethernet Tool*, Agilent publication no. 5988-8278EN

Introduction to 10GBASE-R

Considering the Open Systems Interconnection (OSI) model of the ISO/IEC, the devices to be tested are part of the physical layer. The following figure illustrates the general components of the 10GbE physical and data link layers.

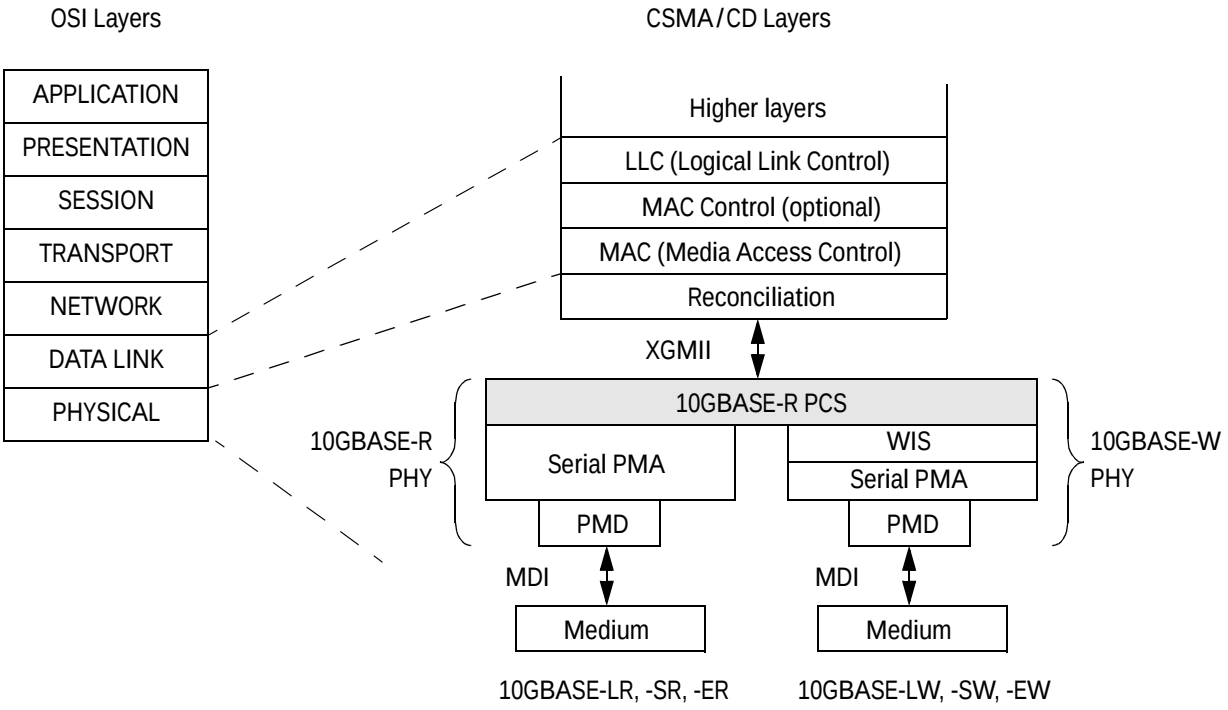


Figure 1 The 10 GbE PHY Reference Model

Explanation of the abbreviations:

Table 1 10GbE Abbreviations and Terms

Abbreviation	Meaning
MDI	Medium Dependent Interface
PCS	Physical Coding Sublayer
PHY	Physical Layer Device
PMA	Physical Medium Attachment
PMD	Physical Medium Dependent
L/S/E encoding	L = 1310 nm fiber wavelength (medium distance) S = 850 nm fiber wavelength (short distance) E = 1550 nm fiber wavelength (long distance)

Table 1 10GbE Abbreviations and Terms

Abbreviation	Meaning
R/W encoding	R = 64B/66B encoded without WIS W = 64B/66B encoded with WIS
WIS	WAN Interface Sublayer
XGMII	10 Gigabit Media Independent Interface

The figure shows also the difference between the 10GBASE-R PHY which is meant for LAN applications and the 10GBASE-W PHY which supports Wide Area Networks (WAN).

We will not discuss the properties of 10GBASE-W in this manual. The WIS implements its own data transmission protocol.

Common properties of the 10GBASE-R PHY and the 10GBASE-W PHY are generally described as 10GBASE-X PHY characteristics.

10GBASE-R PCS Features

A common component of the PHYs for LAN and WAN applications is the 10GBASE-R Physical Coding Sublayer.

The 10GBASE-R PCS provides all services required by the XGMII, including:

- Encoding (decoding) of eight XGMII data octets to (from) 66-bit blocks (64B/66B)
- Transferring encoded data to (from) the PMA in 16 bit transfers
- When connected to a WAN PMD, deleting (inserting) Idles to compensate for the rate difference between the MAC and PMD
- Determining when a functional link has been established and informing the management entity via the MDIO when the PHY is ready for use

10GBASE-R PHY Functional Overview

The following figure shows a functional block diagram of the 10GBASE-R PHY. Its core is formed by the 10GBASE-R PCS.

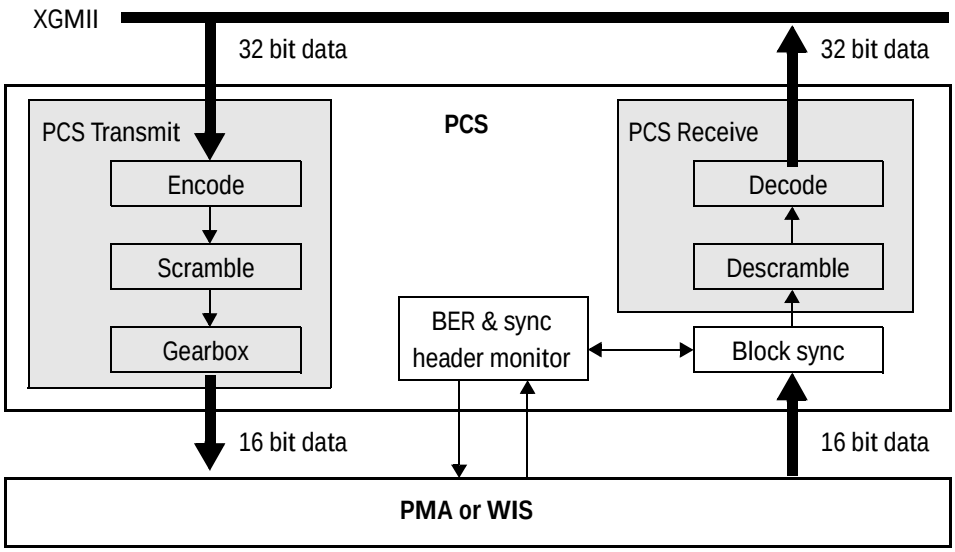


Figure 2 Functional Block Diagram of the 10GBASE-R PHY

PCS transmitter

The PCS transmit part consists of:

- Encoder

  to provide the 64-bit block data format required by the PMA or WIS

- Scrambler

  to convert long runs of zeros or ones into signal transitions. The scrambler is formed by a feedback shift register that implements the polynomial

  $G(x) = 1 + x^{39} + x^{58}$

- Gearbox

  to adapt the 66-bit blocks (64 + 2 sync bits) to the 16-bit width of the PMA interface.

PCS receiver The PCS receive part consists of:

- Synchronizaton stage

  for synchronizing on the incoming data blocks and for clock data recovery (CDR)

- Descrambler

  just the reverse of the scrambler used in the transmit part

- Decoder

  for decoding the received data blocks

Introduction to XAUI

XAUI is the acronym for 10 Gigabit Attachment Unit Interface. The XAUI is designed to extend the physical distance between a 10 Gbit/s capable MAC and a 10 Gbit/s PHY. Where the XGMII is electrically limited to distances of approximately 7 cm, the XGMII Extender allows distances up to approximately 50 cm.

This interface is not strictly necessary to ensure communication, but it is highly recommended, because it allows maximum flexibility in intermixing PHYs and DTEs at 10 Gbit/s speeds.

The XAUI is intended for use as a chip-to-chip interface. No mechanical connector is specified for use with the XAUI.

The XAUI is part of the XGMII Extender. This extender, positioned between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS), consists of two XGMII Extender Sublayers (XGXS), interconnected via the XAUI. This is illustrated in the following figure.

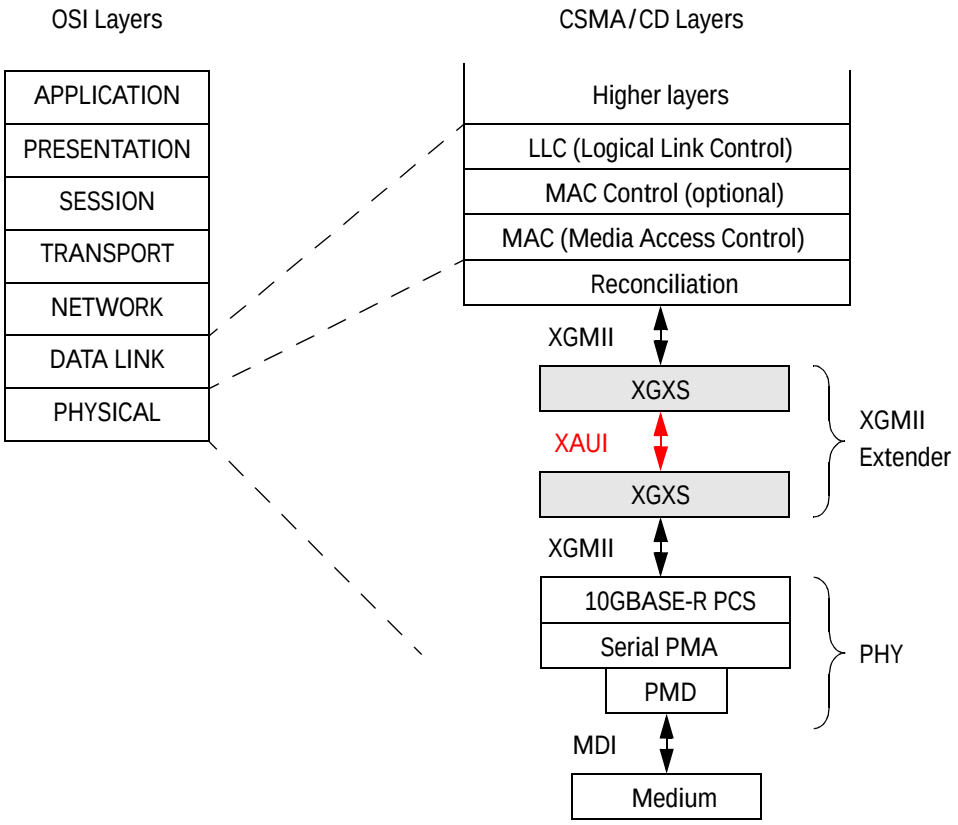


Figure 3 XGMII Extender and XAUI

Explanation of the abbreviations:

Table 2 XAUI Abbreviations and Terms

Abbreviation	Meaning
MDI	Medium Dependent Interface
PCS	Physical Coding Sublayer
PHY	Physical Layer Device
PMA	Physical Medium Attachment
PMD	Physical Medium Dependent
XAUI	10 Gigabit Attachment Unit Interface
XGMII	10 Gigabit Media Independent Interface
XGXS	XGMII Extender Sublayer

XGXS and XAUI Features

The purpose of the XGMII Extender, which is comprised of an XGXS at the RS end (DTE XGXS), an XGXS at the PHY end (PHY XGXS) and a XAUI between them, is to extend the operational distance of the XGMII and to reduce the number of interface signals.

This supports the design of circuit boards and can also be used to separate MAC and PHY components physically.

The XGMII Extender has the following characteristics:

- Simple signal mapping to the XGMII
- Independent transmit and receive data paths
- Four lanes conveying the XGMII 32-bit data and control
- Differential signaling with low voltage swing
- Self-timed interface allows jitter control to the PCS
- Shared technology with other 10 Gbit/s interfaces
- Shared functionality with other 10 Gbit/s Ethernet blocks
- Utilization of 8B/10B coding

XGMII to XAUI Signal Conversion

The XGMII Extender converts the 10 Gbit/s data stream into four lanes conveying differential signals. The byte stream of each lane is 8B/10B encoded by the XGXS for transmission across the XAUI at a nominal rate of 3.125 Gbit/s. The PHY XGXS and the DTE XGXS may operate on independent clocks.

The following figure shows the correspondence of the signals between XGMII and XAUI.

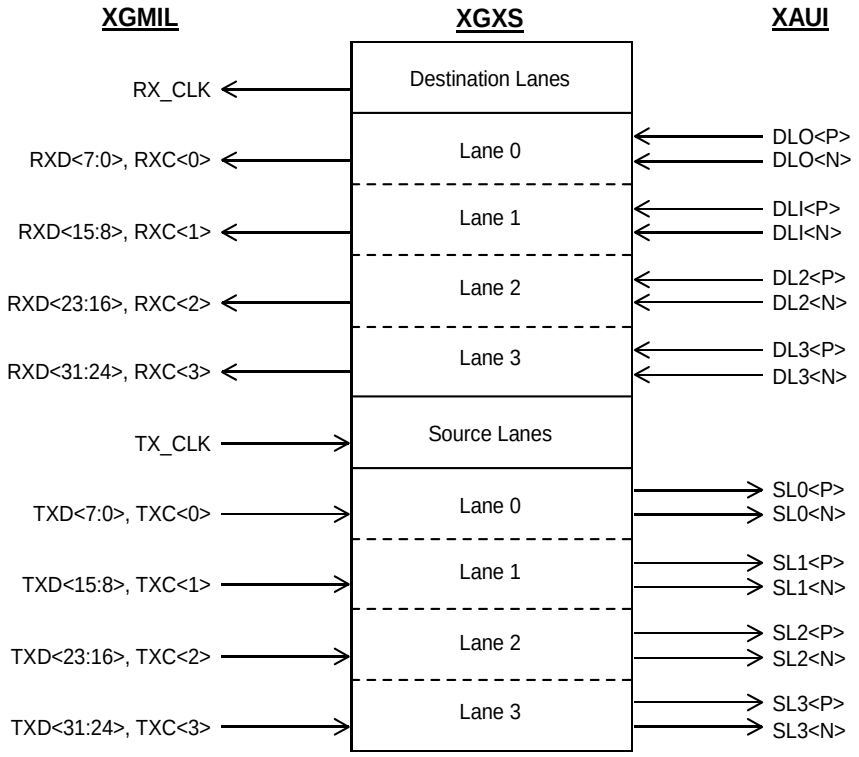


Figure 4 The Correspondence Between XGMII and XAUI

ParBERT Support for 10GbE Devices

The ParBERT hardware supports all required data rates.

10Gb Ethernet Tool

The ParBERT User Software provides you with the 10Gb Ethernet Tool.

This tool allows you to generate data streams that conform to the 10GBASE-R and XAUI specifications. These data streams can be used for

- stimulating the Device Under Test (DUT)
- analyzing the captured response from the DUT

The 10Gb Ethernet Tool includes a frame generator and a post-processor.

Pattern Generation

With the10Gb Ethernet Tool, you can generate data frames formatted for 10GBASE-R as well as for XAUI. These frames are treated like normal ParBERT data segments and can be included into any test sequence. You can forward a generated pattern directly to an active ParBERT system. You can also store the generated pattern in a file that can be imported into any ParBERT system.

The payloads proposed in IEEE 802.3ae for test purposes are readily available. You can also use arbitrary payloads.

Data Format Overview

Ethernet data consists of frames and inter-packet gaps (IPGs).

The following figure illustrates the contents of a frame.

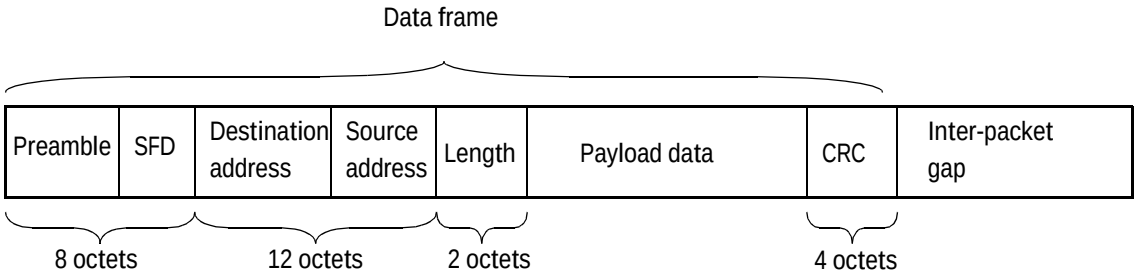


Figure 5 Ethernet Frame Components

Explanation:

Table 3 Ethernet Abbreviations and Terms

Abbreviation	Meaning
SFD	Start Frame Delimiter
CRC	Cyclic Redundancy Check
IPG	Inter-Packet Gap

The 10Gb Ethernet Tool calculates the IPG automatically so that the generated frame fits into a valid ParBERT data segment.

You can choose between 10GBASE-R and XAUI encoding:

- 10GBASE-R encodes the frame by 64B/66B coding with scrambling (scrambling can be switched off); the length of the IPG will be adjusted to the next 64-bit block.
- XAUI encodes the frame by 8B/10B coding (coding can be switched off); the length of the IPG will be adjusted so that the frame ends in lane 3.

Patches

If necessary, the 10Gb Ethernet Tool adds data to the payload. The reason for this is that most often many frames have to be applied and analyzed.

To ensure proper reception of a repetitive pattern without resynchronization of the scrambler/descrambler (10GbE) or a break in the running disparity (XAUI), a patch has to be inserted in a way that scrambler and disparity have the same value at the beginning and end of the pattern.

Therefore, both frame types include a patch inserted at the end of the payload. Note that this feature can also be disabled.

10GBASE-R patch This patch consists of 64 bits (8 octets). It is inserted before the last block which holds the CRC. In 64B/66B encoding, this looks as follows:

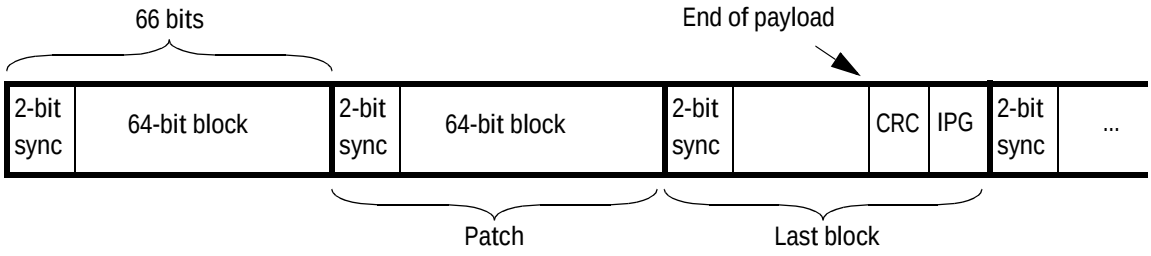


Figure 6 10GbE Payload Patch

XAUI patch For XAUI, the patch consists of four bytes. It is set in the last complete column of the payload (of 4 lanes) before the CRC.

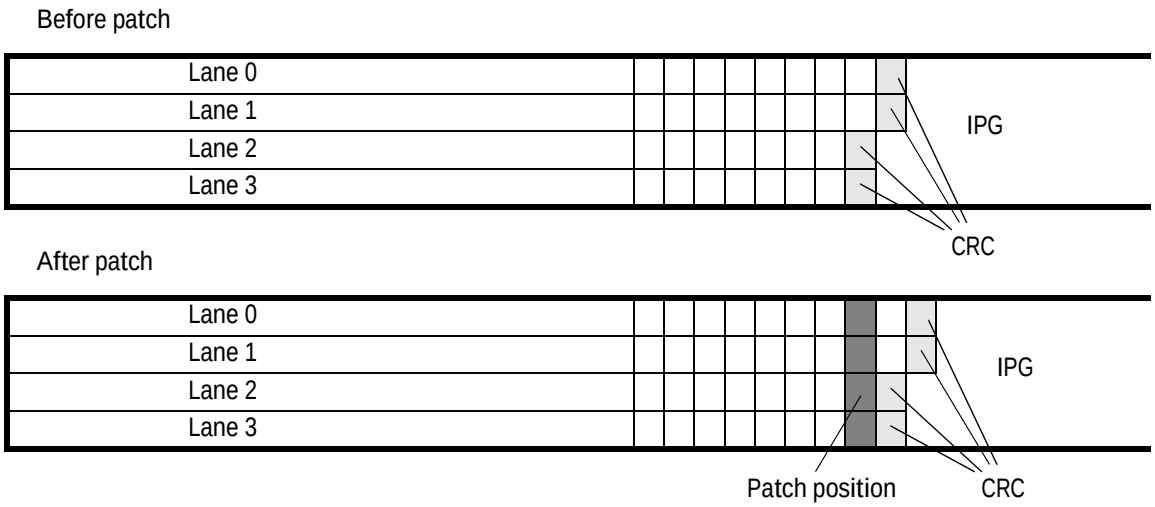


Figure 7 XAUI Payload Patch

NOTE If a patch is inserted, the CRC is calculated anew.

Note also that the post-processor of the 10Gb Ethernet Tool is unable to recognize patches if they are used in conjunction with non-PRBS payload data patterns.

Post Processing

The post-processor of the 10Gb Ethernet Tool uploads and analyzes captured data.

What the Post-Processor Does in General

The post-processor

- Checks the setting for validity
- Initiates the start of data acquisition
- Uploads the captured data
- Analyzes the received data
- Displays the results

What the Post-Processor Does for 10GBASE-R Tests

For 10GBASE-R tests, the post-processor performs the following tasks:

- Check for valid sync bits (01, 10). If error rate is too high, stop and show error message.
- Descramble found blocks. Save received block, descrambler register, and descrambled 64-bit value.
- Search for first control block with start block type (0x33, 0x66, 0x78) and analyze Idles. If start block is not found, stop and show error message.
- Extract and check received frames (CRC).
- Generate expected pattern according to the setting on the *Generation/Expected* page.
- Generate blocks of scrambled pattern with expected data in the received block scheme.
- Compare every bit in received block with expected block.
- Mask patched frames (only possible for PRBS payload).

What the Post-Processor Does for XAUI Tests

For XAUI tests, the post-processor performs the following tasks:

- Search for the preamble on first lane. If not found, stop and generate error message.
- Decode all lanes (8B/10B coding). Save running disparity and decoded values.

- Extract and check received frames (CRC).
- Generate expected pattern according to the setting on the *Generation/expected* page.
- Code expected data.
- Compare every bit in coded received pattern with coded expected data.
- Mask patched frames (only possible for PRBS).

Post-Processor Results

The post-processor can report:

CRC Errors: Every CRC is calculated from expected data. The calculated value is then compared against the received value. If not identical, the CRC error counter is increased. Every bit in the CRC is additionally compared and differences are shown as bit errors.

Bit Errors: Idle and Frame characters are checked. Regarding XAUI patterns, the rules for Idle generation are not checked. If an Idle character appears to be wrong, every possible Idle is compared and the Idle character with the least bit errors defines the bit error counter increase.

BER: The Bit Error Rate is calculated by dividing the bit errors per lane by counted bits per lane including Idle and Frame characters divided by the number of lanes.

For 10GBASE-R, the number of lanes is one, for XAUI it is four.

$$\text{BER} = \frac{\text{Bit errors per lane}}{\Sigma(\text{Bits in Idle} + \text{Bits in Frames}) \ / \ \text{No of lanes}}$$

No of Frames: If possible, patched frames are excluded (PRBS payloads have to be used). Excluded frames are not counted—bit errors are not shown.

Block Errors: Only 10GBASE-R: Blocks with wrong sync bits and/or wrong block type are shown as block errors; data is not compared.

Prerequisites

Testing parallel devices or buses (DUTs with n input lines and n output lines) is a standard function of every ParBERT system. In this section, we concentrate on devices that expect 10GBASE-R data on one side and return XAUI data on the other—and vice versa.

With ParBERT, you can test the XAUI-side of a 10GbE transceiver device. You can also test the 10GBASE-R serial side.

Prerequisites for Testing the XAUI Side

Pattern generator requirements

The test equipment that generates the 10GBASE-R formatted pattern has to be able to provide:

- one 10GbE data channel
- data generation clock

You could use a ParBERT 81250 with the following setup for this:

- One E8491B IEEE 1394 interface (FireWire)
- One E4808A clock module
- One E4866A 10.8 Gbit/s data generator module
- One 10.3125 Gbit/s E/O converter

NOTE You may also wish to add an N4868A 10.8 Gbit/s Booster module to the generator. It depends on the input characteristics of your DUT whether this module is necessary or not.

Pattern analyzer requirements

For analyzing the XAUI signals, you need a second ParBERT system.

You could use a ParBERT 81250 with the following configuration:

- One E8491B IEEE 1394 interface (FireWire)
- One E4808A clock module
- Two 3.35 Gbit/s E4861B Data Generator/Analyzer modules, each equipped with two E4863B, 3.35 Gsa/s, differential/single-ended analyzer frontends

NOTE You can install both systems into one VXI mainframe. When this is done, both systems can be operated through one E8491B IEEE 1394 interface.

Setup Example

The clock signal can be generated by the built-in clock module or an external instrument. A sample setup is illustrated in the figure below:

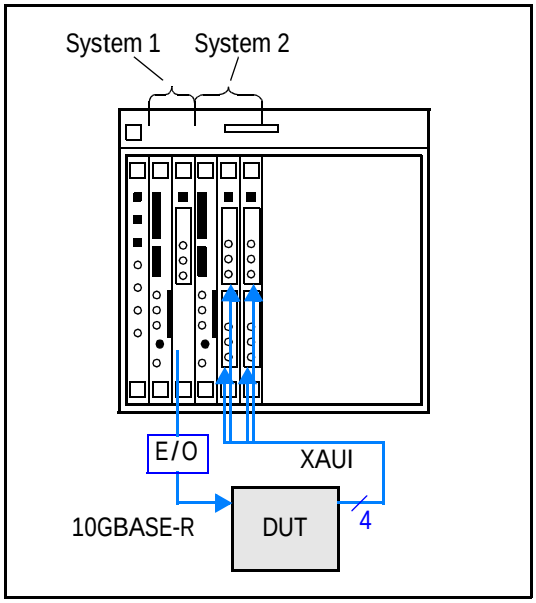


Figure 8 Hardware Setup for Testing the XAUI Side of a Transceiver

Prerequisites for Testing the Serial Side

Pattern generator requirements

The pattern generator must be able to provide the test pattern to the four XAUI lanes:

- four 3.125 Gbit/s data channels
- data generation clock

You could use a ParBERT 81250 with the following setup for this:

- One E8491B IEEE 1394 interface (FireWire)
- One E4808A clock module
- Two 3.35 Gbit/s E4861B Data Generator/Analyzer modules, each equipped with two E4862B, 3.35 Gbit/s, differential output frontends

Pattern analyzer requirements

The error detector must be able to handle the following input:

- One 10GbE data channel
- One clock channel

You could use a second ParBERT system with the following configuration:

- One E8491B IEEE 1394 interface (FireWire)
- One E4808A clock module
- One E4867A 10.8 Gbit/s data analyzer module
- One 10.3125 Gbit/s O/E converter

NOTE You can install both systems into one VXI mainframe. When this is done, both systems can be operated through one E8491B IEEE 1394 interface.

Setup Example A sample setup is illustrated in the figure below:

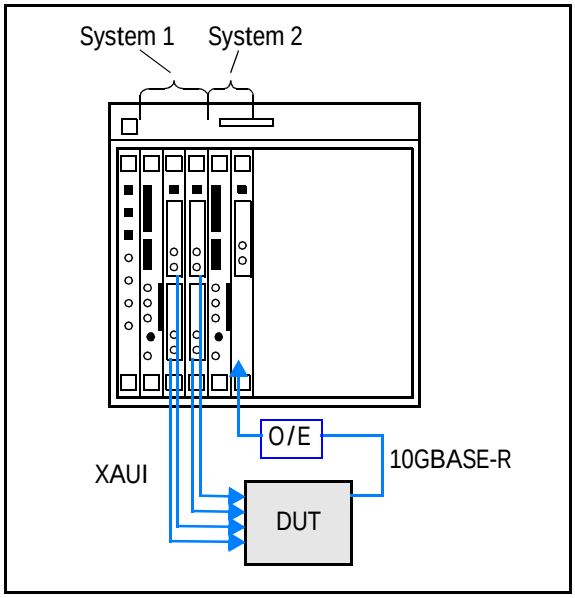


Figure 9 Hardware Setup for Testing the Serial Side of a Transceiver

Setup for Testing Both Sides

If you wish to test both sides of a Xenpak device (or similar), you need four ParBERT systems. They require at least:

- Four E4808A clock modules
- One E4866A 10.8 Gbit/s data generator module
- Two 3.35 Gbit/s E4861B Data Generator/Analyzer modules, each equipped with two E4863B, 3.35 Gsa/s, differential /single-ended analyzer frontends
- Two 3.35 Gbit/s E4861B Data Generator/Analyzer modules, each equipped with two E4862B, 3.35 Gbit/s, differential generator frontends
- One E4867A 10.8 Gbit/s data analyzer module

This adds up to 10 modules. That means, you can add one E8491B IEEE 1394 interface module and install all these 11 modules into one VXI mainframe that is controlled via “FireWire” by a remote computer.

This configuration is illustrated in the figure below.

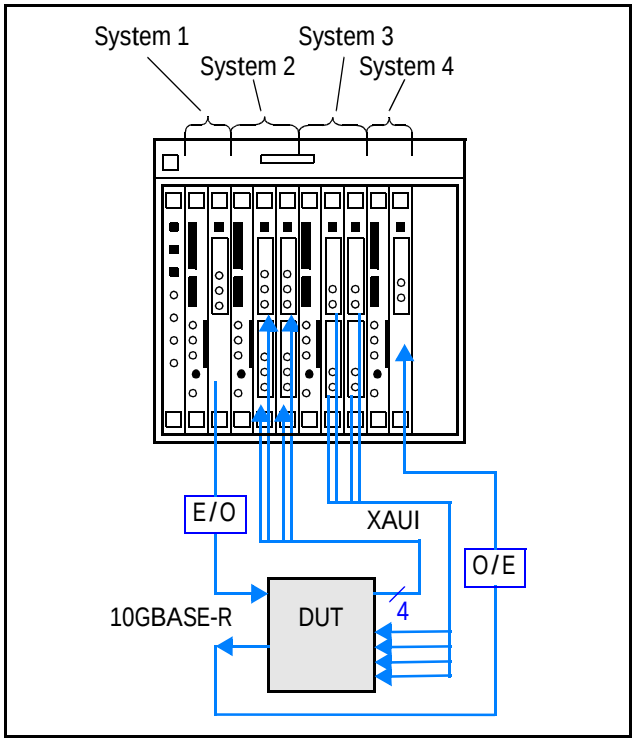


Figure 10 Setup for Testing Both Sides of a Xenpak Device

Dependencies

It has already been mentioned that the 10Gb Ethernet Tool actually combines two tools:

- a frame generator
- a post-processor

Dependencies exist between the usage of these tools and the current system configuration.

Online vs. Offline Frame Generation

The 10GbE frame generator creates ParBERT data segments of type “memory”. You can create segments of various lengths. You need only take care that they fit into the available memory of the ParBERT module(s). See also *“Block Length Considerations” on page 26*.

Long segments improve the resolution of BER measurements. Short segments reduce the test time.

The 10GbE frame generator can be used in offline and online mode.

Offline operation

If the 10Gb Ethernet Tool is not connected to a suitable and running ParBERT system, the generated data segments can be stored on disk.

Segments that are stored in individual files can be freely moved around. Before they can be used on a ParBERT system, they have to be imported into that system.

They can be imported into the system’s global segment pool or into the local segment pool. The latter is associated with and only accessible from the presently loaded setting. The global segment pool can be accessed by all settings.

Online operation

When the 10Gb Ethernet Tool is online connected to a suitable ParBERT pattern generator system, the frame generator also allows you to send the generated data segment directly to that system.

"Suitable" means that the ParBERT system has to be set up as required. The frequency must be set, a DUT input port with one or four terminals must exist, and the connections to the generator(s) must be made. If a suitable setting has been saved, all this can be done by loading that setting.

NOTE

The direct transfer is only available for 10GbE-formatted segments. The frame generator also allows you to generate special test patterns. These patterns have to be stored in files and imported afterwards.

Block Length Considerations

The segments created by the 10Gb Ethernet Tool are memory segments that have a limited length. The lengths of the sequence blocks have to be adapted.

The upper limit is the memory of the modules. For example, up to 16,777,216 bits for E4861B modules.

The lower limit is not the segment resolution that may be proposed by the Sequence Editor.

Generator block length

The minimum block length for a generator system is one Ethernet frame plus the Inter Packet Gap (IPG). The IPG is automatically calculated.

Analyzer block length

The minimum block length for an analyzer system is two Ethernet frames plus the IPG.

For an XAUI frame with a length of 1500 bytes and an IPG of 500, you may estimate:

```
Minimum segment length (bytes) = 2 × (1500 + IPG) / 4
```

This yields a minimum length of roughly 1000 bytes or 10.000 bits (10B coding).

For the analyzer system, you can choose between a fast measurement (by capturing few data) or a more precise measurement (by capturing bulk data).

A reasonable approach is to capture a moderate amount of data and to repeat the measurement, for example 100 times. Thus, you can capture and analyze many frames and achieve a good ratio of usable frames vs. patched frames.

Post-Processing

The post-processor uploads and analyzes captured data from an analyzer system. This requires that the ParBERT analyzer system is powered and the 10Gb Ethernet Tool is connected to it.

The post-processor has its own Start and Break buttons. They control the analyzer system. You can choose between executing a single measurement or multiple measurements.

Multiple measurements can be terminated by a repetition counter, a bit error, or by clicking the Break button.

NOTE The generator system has to generate an endless data stream (infinite loop). It must be started manually. This has to happen before the analyzer system is started.

Capture Data mode

In order to acquire all data, the analyzer system must be operated in *Capture Data* mode.

Manual delay adjustment

In *Capture Data* mode, the functions for automatic analyzer sampling delay adjustment are not available. A suitable analyzer sampling delay has to be found and set manually.

This can be done for the DUT output port as a whole. Depending on the DUT characteristics, you may also need to fine-tune every single terminal or analyzer frontend, respectively.

Post-processing criteria

The post-processor expects the data pattern that is defined on the *Generation/Expected* page of the 10Gb Ethernet Tool.

This is no problem if you have just created the segment to be generated and now connect the 10Gb Ethernet Tool to the analyzer system. Your setup is still there.

But if you are generating the pattern from a stored segment or if you have restarted the 10Gb Ethernet Tool, you have to set up the *Generation/Expected* page so that the expected data is identical with the generated pattern.

This is also necessary if you load a setting on the generator system that references a stored segment.

TIP When you are creating segments with 10GbE-formatted frames that are going to be used later-on, it is recommended to document the setup parameters of the *Generation/Expected* page for each of these segments.

A simple screenshot, for example, manually labeled with the name of the segment, makes it easy to specify the expected data afterwards.

How the post-processing works

The generating ParBERT system must be up and running before the analyzer system is started.

Once it has been started, the analyzer system captures data until either its test sequence has finished (generally after one sequence block) or its memory is full.

The post-processor uploads the captured data which is an arbitrary section of the continuous DUT output data stream.

Now, the first task of the post-processor is to align the captured data with the expected. For this purpose, it uses the same pattern generator that created the generated data segment. The pattern generator generates a number of frames internally and the post-processor compares them with the first captured frames.

As soon as they coincide, the post-processor has found its starting frame and is ready for checking the consistency.

Treatment of Patches

Before comparing captured and expected bits, the post-processor also attempts to remove all patched frames.

Patches are inserted to ensure a repetitive pattern without resynchronization of the scrambler/descrambler (10GbE) or a break in the running disparity (XAUI). See also *"Pattern Generation" on page 13*.

Patches are not considered to be valid data that should be compared. The removal, however, works only reliably, if the payload is pure PRBS. Therefore, the generation of patches can be disabled.

In addition, there are different patches for 10GbE and XAUI. To stay consistent, the frame generator parameters set on the *Generation/Expected* page of the 10Gb Ethernet Tool apply for both sides.

That means, if you generate a serial 10 Gbit/s signal, use the same setup for the post-processor, even if it analyzes XAUI data, and vice versa.

Test Setup Procedures

This section provides an overview of the steps you have to perform for testing a 10GbE transceiver device (for example, a Xenpak device). These steps lead you up to the point where you begin with the post-processor of the 10Gb Ethernet Tool.

Your hardware setup may look as shown in the figure below:

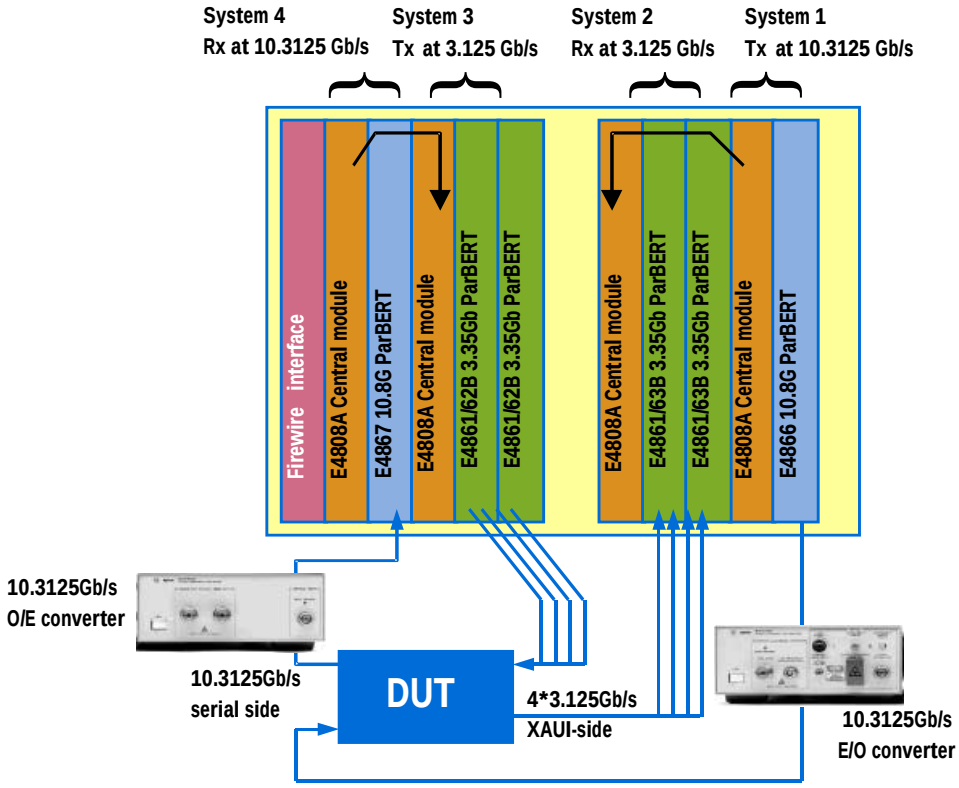


Figure 11 Hardware Setup Example

The systems 1 and 2 are used for stimulating the serial and testing the XAUI side. The systems 3 and 4 are used for stimulating the parallel and testing the serial side. The clock connections will be discussed in the following sections.

Setup Procedure for Testing the XAUI Side

You need one system with one 10.3125 Gbit/s generator for stimulating the DUT and a second system with four 3.125 Gbit/s analyzers for capturing and analyzing the response.

XAUI Test Stimulator Setup Procedure

Proceed as follows:

1 Start the ParBERT user interface for the generator system (this is system 1 in the figure *"Hardware Setup Example" on page 31*).

2 Use the Connection Editor to create a one-terminal DUT input port and to connect the terminal with the 10.8 Gbit/s data generator module.

3 With the Parameter Editor, set the system clock frequency.

You have two possibilities:

– You can use the oscillator built into the clock module: On the *Frequency* page, set the *Segment Resolution* to 256, the *Trigger Frequency Multiplier* to 1/16th, and the *Frequency* to 10.3125 GHz. The TRIGGER OUTPUT of the clock module will now generate a clock signal of 644.53125 MHz (in *Clock Generator* mode, of course).

– You can also use an external clock, provided by a precision generator or by the DUT itself. This signal has to be connected to the CLOCK/REF INPUT of the clock module. External clock frequencies that fit to both sides of the DUT are, for example, 156.25 MHz, 312.5 MHz, 625.0 MHz.

Then, on the *Clock/REF Input* page, enable *External Clock Source* and click the Measure button. Adjust the *Clock Multiplier* to generate the desired frequency (for a 156.25 MHz source, this would be 66).

4 Start the 10Gb Ethernet Tool. Use this tool to create a suitable memory-type data segment, formatted for 10GBASE-R.

This tool allows you to generate data segments formatted for 10GBASE-R as well as for XAUI with PRBS or arbitrary payloads.

When the ParBERT firmware server is running locally or on a remote computer, you can connect to the generator system and transfer the generated segment directly into the global segment pool of this system. If you have loaded a setting, you can also transfer the generated segment into the local segment pool.

If you have no connection to the target system, you can store the generated segment in a file. The contents of this file can be imported into any ParBERT system (see the *ParBERT System User Guide*).

NOTE The 10Gb Ethernet Tool will be explained in detail in *"Using the 10Gb Ethernet Tool" on page 75*.

TIP Do not terminate the 10Gb Ethernet Tool if you plan to use the post-processor of the 10Gb Ethernet Tool. The post-processor requires the information on the generated signal.

If you wish to make a break, take a note that documents the settings used for the generated segment, or make a screenshot of the tool's *Generation/Expected* page.

5. If necessary, import the generated segment into the generator system.
6. Use the Segment Editor to check the segment length.
7. Use the Detail Mode Sequence Editor to create the generator sequence.

   The proposed generator sequence for a simple test consists of one sequence block that is endlessly looped.
8. Include the generated segment into the block. Adjust the block length so that the generated segment fits into the block.

Example The following figure illustrates the setup we have made so far.

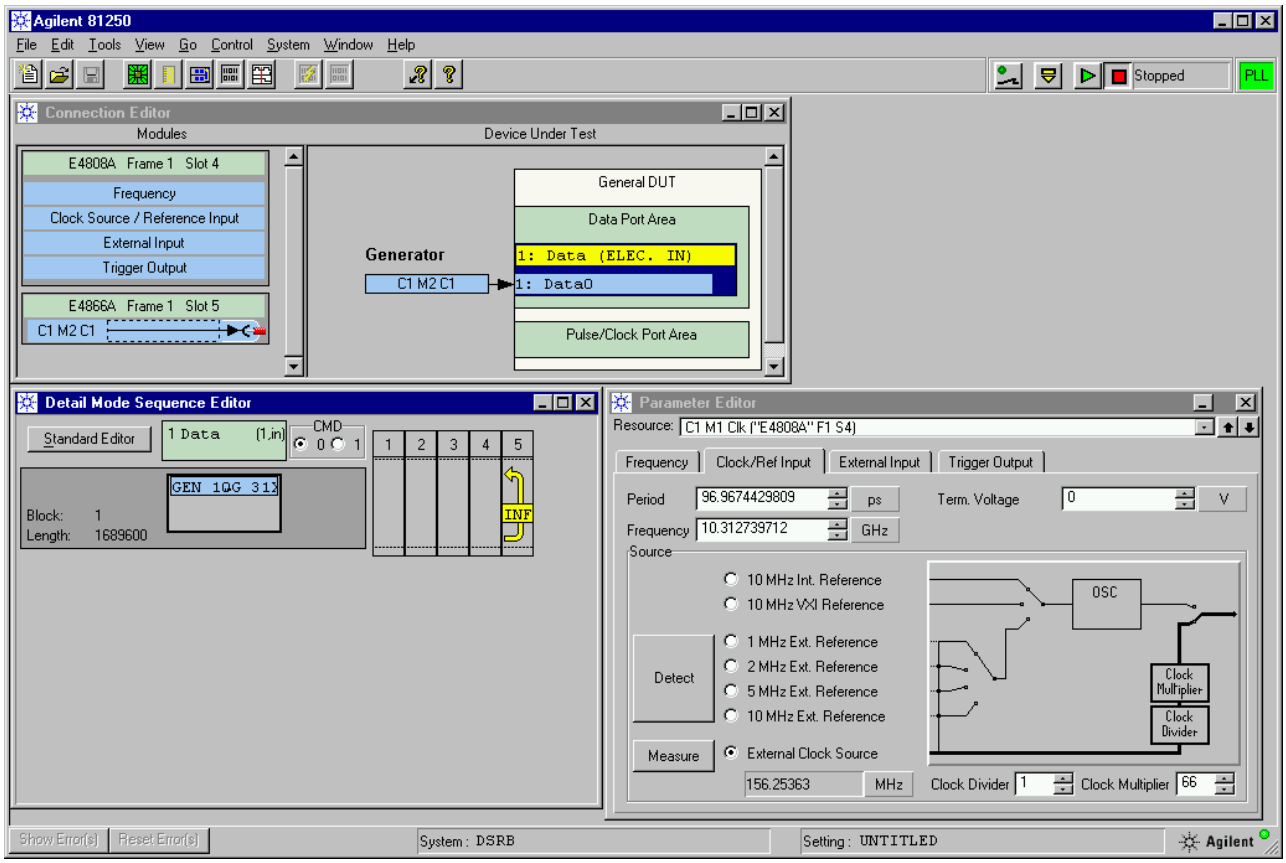


Figure 12 Generator Setup for XAUI Tests

You can see the DUT connection. The example shows how an external clock source can be set up. The Detail Mode Sequence Editor shows one block that is endlessly looped. The generated segment (the payload is a $2^{31} - 1$ PRBS) contains 100 frames. It has a length of 1,689,600 bits.

9 Use the Parameter Editor to adjust the generated signal levels to the requirements of the E/O converter.

10 Click the Run button. From now on, the generator system will produce the specified pattern.

XAUI Test Analyzer Setup Procedure

Proceed as follows:

1 Start a second instance of the ParBERT user interface for the analyzer system (this is system 2 in the figure *"Hardware Setup Example" on page 31*).

2 Use the Connection Editor to create a four-terminal DUT output port and to connect the terminals with the four 3.35 GSa/s data analyzer frontends.

3 With the Parameter Editor, set the system clock frequency.

The analyzer clock has to be provided by an external source. The source must be connected to the CLOCK/REF INPUT of the analyzer system's clock module.

For a completely synchronous device and test, the source can be the TRIGGER OUTPUT of the clock module of the stimulating system. This is illustrated in the figure *"Hardware Setup Example" on page 31*).

However, the DUT output clock may differ from the DUT input clock. In general, the DUT output clock has to be used for the capturing system. Therefore, the external clock can also be provided by the DUT itself or a precision clock generator.

So, there are two possibilities:

– If you are using the clock module of the 10 Gb/s stimulating system for providing the analyzer clock, the source provides a clock pulse of 644.53125 MHz. (if set up as described above).

On the *Clock/REF Input* page of the analyzer system, enable *External Clock Source* and click the Measure button.

To generate the desired analyzer frequency of 3.125 GHz, you have to divide the external source frequency by 33 and to multiply the result by 160. This exceeds the capabilities of the external clock divider/multiplier (for details see the *ParBERT System User Guide*).

To solve the problem, you can, for example, adjust the *Clock Divider* to 33 and the *Clock Multiplier* to 10. This gives you a system frequency of 195.3125 MHz. Then, on the *Frequency* page, click the Allow Multiple Frequencies button and set the clock multiplier of the port to 16.

– If you are using an external clock source, connect it.

  On the *Clock/REF Input* page of the analyzer system, enable *External Clock Source* and click the Measure button. Adjust the *Clock Multiplier* to generate the desired frequency (for a 156.25 MHz source, this would be 20).

4 If not already done, start the 10Gb Ethernet Tool

5 Connect it to the analyzer system.

6 On the *Generation/Expected* page, you need exactly the same setup as was used for creating the generator segment. If you have restarted the tool, you have to reproduce the original settings as defined for the generator.

NOTE The 10Gb Ethernet Tool will be explained in detail in *"Using the 10Gb Ethernet Tool" on page 75*.

7 In the ParBERT user interface, set the *Measurement Configuration* to *Capture Data*.

8 Use the Detail Mode Sequence Editor to create the analyzer sequence.

– Delete the endless loop.

  One block will be captured.

– Set the segment-type to "Acquire".

  Captured data will be post-processed.

– Adjust the block length to capture more than two frames.

Example The following figure illustrates the setup we have made so far.

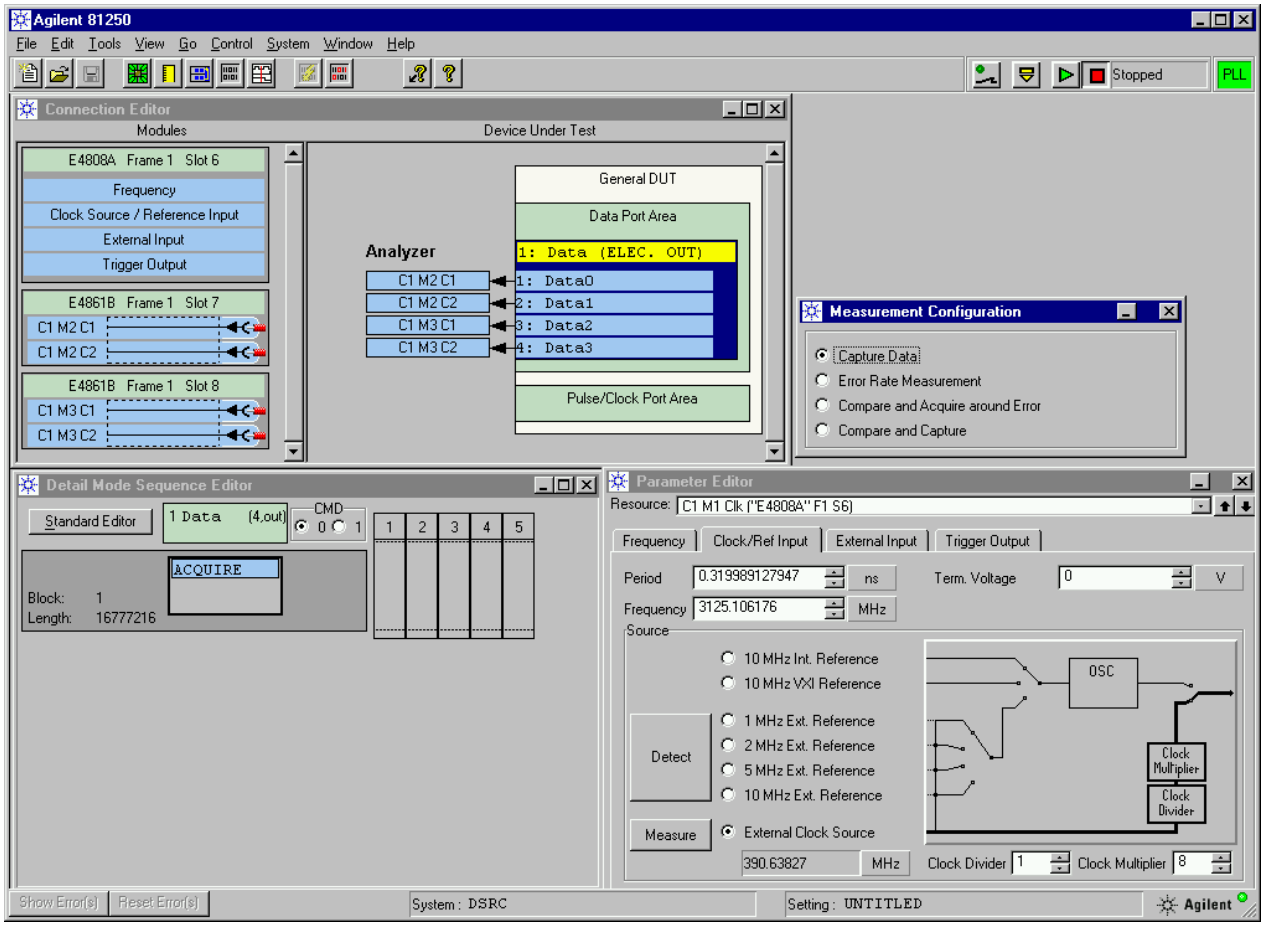


Figure 13 Analyzer Setup for XAUI Tests

You can see the DUT connections. The measurement mode is *Capture Data*. An external clock source is used. The Detail Mode Sequence Editor shows one block. The segment to be captured has a length of 16,777,216 bits. This is the maximum memory size of the E4861B modules.

9 Use the Parameter Editor to adjust the expected signal levels to the characteristics of the DUT (double-click the port area shown in the Connection Editor).

10 Use the Parameter Editor to set the analyzer sampling delay.

There are several ways to find the optimum sampling delay:

– If the DUT is able to generate a defined test pattern by its own, you may be able to run a preliminary test with automatic analyzer delay adjustment (*Auto Bit Synchronization* or *Auto*

Delay Alignment). You can then enter the delays that have been determined.

– You can also start a repetitive test with an initial delay of 0.5 periods. While the test is running, you can then move the delay vernier of the Parameter Editor until the measured BER is acceptable.

– It can happen that a uniform sampling delay for the port is not the optimum. If this is the case, you can move the delay verniers of the analyzers individually while the test is running.

11 Open the *Post Processing* page of the 10Gb Ethernet Tool and enable the XAUI test.

12 Decide on the Mode: *Single Measurement* or *Multiple Measurements*.

TIP *Multiple Measurements* is recommended if you are setting up the test for an unknown device. This mode allows you to fine-tune the analyzer sampling delay.

13 Ensure that the generator system is running.

14 To execute the test, click the Start button on the *Post Processing* page of the 10Gb Ethernet Tool.

15 To terminate the test, click the Break button.

Note that Break recognition and final stop may take some time, especially if a large capture memory is used (up to three measurement cycles).

Setup Procedure for Testing the Serial Side

Here, four E4862B, 3.35 Gbit/s, differential output frontends can generate the necessary data stream.

The analyzer system has to have at least one E4867A 10.8 Gbit/s data analyzer module.

Serial 10GbE Test Stimulator Setup Procedure

Proceed as follows:

1 Start the ParBERT user interface for the generator system (this is system 3 in the figure *"Hardware Setup Example" on page 31*).

2 Use the Connection Editor to create a four-terminal DUT input port. Connect the terminals with the 3.35 Gbit/s data generator frontends.

3 With the Parameter Editor, set the system clock frequency.

   You have two possibilities:

   – You can use the oscillator built into the clock module: On the *Frequency* page, set the *Segment Resolution* to 64, the *Trigger Frequency Multiplier* to 1/8th, and the *Frequency* to 3.125 GHz. The TRIGGER OUTPUT of the clock module will now generate a clock signal of 390.625 MHz (in *Clock Generator* mode, of course).

   – You can also use an external clock, provided by a precision generator or by the DUT itself. This signal has to be connected to the CLOCK/REF INPUT of the clock module. External clock frequencies that fit to both sides of the DUT are, for example, 156.25 MHz, 312.5 MHz, 625.0 MHz.

     Then, on the *Clock/REF Input* page, enable *External Clock Source* and click the Measure button. Adjust the *Clock Multiplier* to generate the desired frequency (for a 156.25 MHz source, this would be 20).

4 Start the 10Gb Ethernet Tool. Use this tool to create a suitable memory-type data segment, formatted for XAUI.

The 10Gb Ethernet Tool allows you to generate data segments formatted for 10GBASE-R as well as for XAUI with PRBS or arbitrary payloads.

When the ParBERT firmware server is running locally or on a remote computer, you can connect to the generator system and transfer the generated segment directly into the global segment pool of this system. If you have loaded a setting, you can also transfer the generated segment into the local segment pool.

If you have no connection to the target system, you can store the generated segment in a file. The contents of this file can be imported into any ParBERT system (see the *ParBERT System User Guide*).

NOTE The 10Gb Ethernet Tool will be explained in detail in *"Using the 10Gb Ethernet Tool" on page 75*.

TIP Do not terminate the 10Gb Ethernet Tool if you plan to use the post-processor of the 10Gb Ethernet Tool. The post-processor requires the information on the generated signal.

If you wish to make a break, take a note that documents the settings used for the generated segment, or make a screenshot of the tool's *Generation/Expected* page.

5 If necessary, import the generated segment into the generator system.

6 Use the Segment Editor to check the segment length.

7 Use the Detail Mode Sequence Editor to create the generator sequence.

The proposed generator sequence for a simple test consists of one sequence block that is endlessly looped.

8 Include the generated segment into the block. Adjust the block length so that the generated segment fits into the block.

Example The following figure illustrates the setup we have made so far.

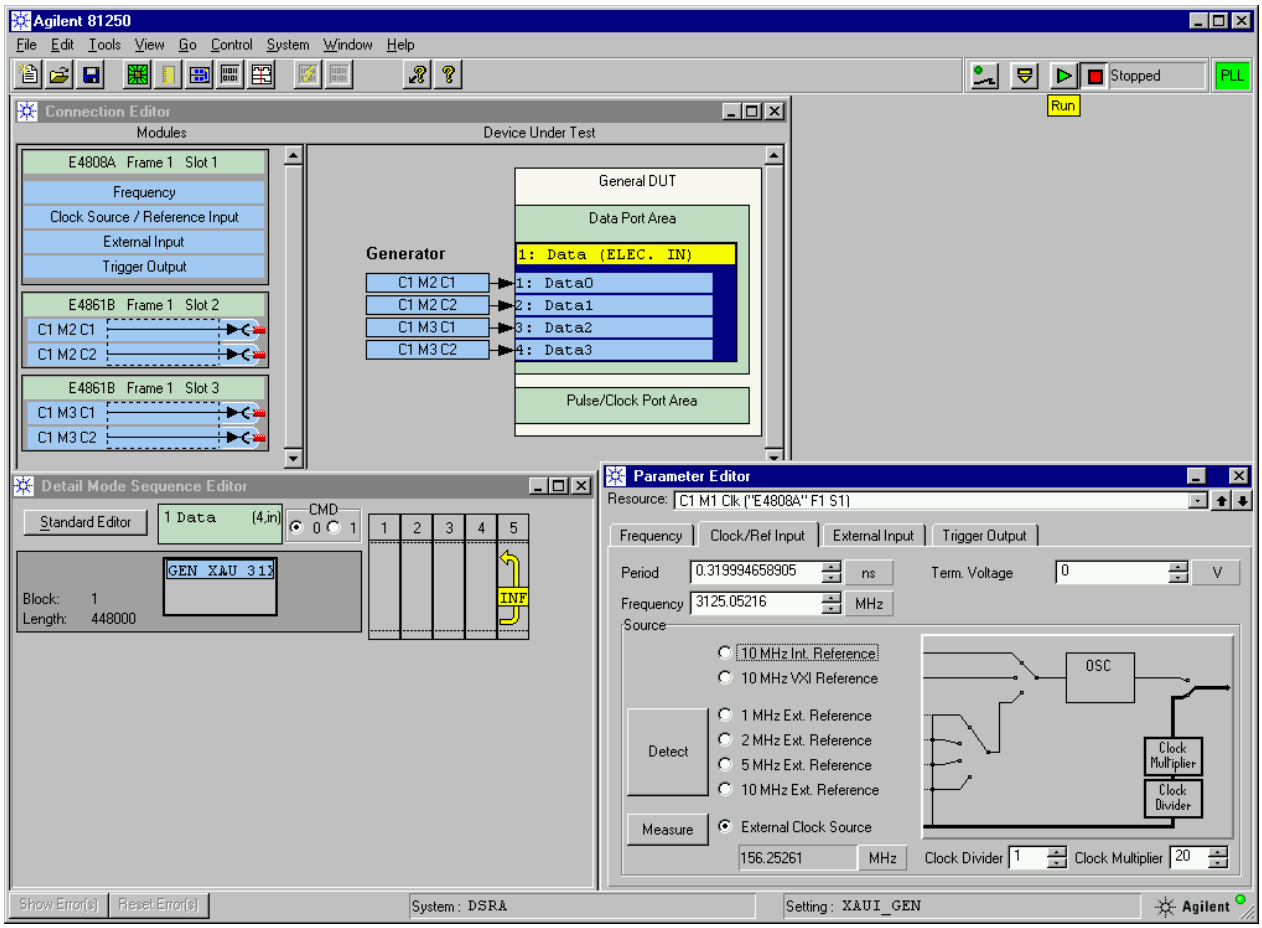


Figure 14 Generator Setup for 10GBASE-R Tests

You can see the DUT connections. The example shows how an external clock source can be set up. The Detail Mode Sequence Editor shows one block that is endlessly looped. The generated segment (the payload is a $2^{31} - 1$ PRBS) contains 100 frames. It has a length of 448000 bits.

9 Use the Parameter Editor to adjust the generated signal levels to the requirements of the DUT.

10 Click the Run button. From now on, the generator system will produce the specified pattern.

Serial 10GbE Test Analyzer Setup Procedure

Proceed as follows:

1 Start a second instance of the ParBERT user interface for the analyzer system (this is system 4 in the figure *"Hardware Setup Example" on page 31*).

2 Use the Connection Editor to create a one-terminal DUT output port and to connect the terminals with the four 3.35 GSa/s data analyzer frontends.

3 With the Parameter Editor, set the system clock frequency.

The analyzer clock has to be provided by an external source. The source must be connected to the CLOCK/REF INPUT of the analyzer system's clock module.

For a completely synchronous device and test, the source can be the TRIGGER OUTPUT of the clock module of the stimulating system. This is illustrated in the figure *"Hardware Setup Example" on page 31*).

However, the DUT output clock may differ from the DUT input clock. In general, the DUT output clock has to be used for the capturing system. Therefore, the external clock can also be provided by the DUT itself or a precision clock generator.

So, there are two possibilities:

– If you are using the clock module of the 3.35 Gb/s stimulating system for providing the analyzer clock, the source provides a clock pulse of 390.625 MHz. (if set up as explained above).

  On the *Clock/REF Input* page of the analyzer system, enable *External Clock Source* and click the Measure button.

  To generate the desired analyzer frequency of 10.3125 GHz, you have to divide the external source frequency by 5 and to multiply the result by 132. This is well in the range of the external clock divider/multiplier.

– If you are using an external clock source, connect it.

  On the *Clock/REF Input* page of the analyzer system, enable *External Clock Source* and click the Measure button. Adjust the *Clock Multiplier* to generate the desired frequency (for a 156.25 MHz source, this would be 66).

4 If not already done, start the 10Gb Ethernet Tool

5 Connect it to the analyzer system.

6 On the *Generation/Expected* page, you need exactly the same setup as for the generator. If you have restarted the tool, you have to reproduce the original settings as defined for the generator.

NOTE The 10Gb Ethernet Tool will be explained in detail in *“Using the 10Gb Ethernet Tool” on page 75*.

7 In the ParBERT user interface, set the *Measurement Configuration* to *Capture Data*.

8 Use the Detail Mode Sequence Editor to create the analyzer sequence.

– Delete the endless loop.

  One block will be captured.

– Set the segment-type to “Acquire”.

  The captured data will be post-processed.

– Adjust the block length to capture more than two frames.

Example The following figure illustrates the setup we have made so far.

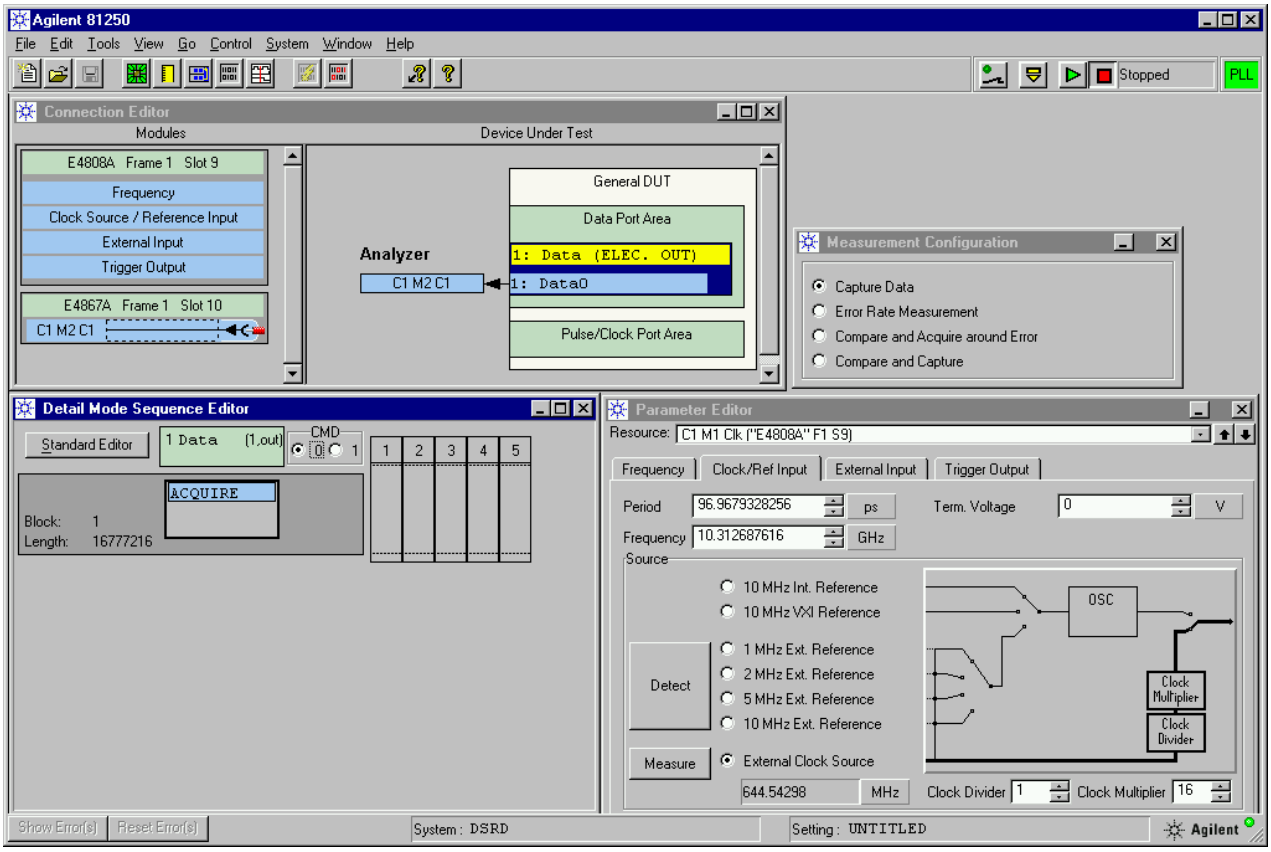


Figure 15 Analyzer Setup for 10GBASE-R Tests

You can see the DUT connection. The measurement mode is *Capture Data*. An external clock source is used. The Detail Mode Sequence Editor shows one block. The segment to be captured has a length of 16,777,216 bits.

9 Use the Parameter Editor to adjust the expected signal levels to the characteristics of the O/E converter.

10 Use the Parameter Editor to set the analyzer sampling delay.

There are two ways to find the optimum sampling delay:

- If the DUT is able to generate a defined test pattern by its own, you may be able to run a preliminary test with automatic analyzer delay adjustment (*Auto Bit Synchronization* or *Auto Delay Alignment*). You can then enter the delays that have been determined.
- You can also start a repetitive test with an initial delay of 0.5 periods. While the test is running, you can then change the delay values with the Parameter Editor until the measured BER is acceptable.

11 Open the *Post Processing* page of the 10Gb Ethernet Tool and enable the 10GBASE-R test.

12 Decide on the Mode: *Single Measurement* or *Multiple Measurements*.

TIP *Multiple Measurements* is recommended if you are setting up the test for an unknown device. This mode allows you to fine-tune the analyzer sampling delay.

13 Ensure that the generator system is running.

14 To execute the test, click the Start button on the *Post Processing* page of the 10Gb Ethernet Tool.

15 To terminate the test, click the Break button.

Note that Break recognition and final stop may take some time, especially if a large capture memory is used (up to three measurement cycles).

Setting up a XAUI Test

This example demonstrates how you can set up the test of the XAUI side of a Xenpak device using two ParBERT systems and pseudo random data.

See:

- *"Focus of this Example" on page 46*
- *"Hardware Setup" on page 47*
- *"Pattern Generator Setup" on page 48*
- *"Pattern Analyzer Setup" on page 59*
- *"Running the Test" on page 68*
- *"Setting up Additional XAUI Tests" on page 71*

Focus of this Example

This example uses two ParBERT systems.

- We use one ParBERT 10.8 Gbit/s pattern generator system that generates the serial data stream for stimulating the device under test (DUT).
- We use a second ParBERT system that analyzes the response of the DUT.
- The DUT has one input terminal and 4 output terminals.
- Pure, undistorted PRxS data is generated and expected.
- The data is captured and processed by the 10Gb Ethernet Tool.
- The sampling delay of the analyzers is manually set.
- The bit error rate (BER) is measured.

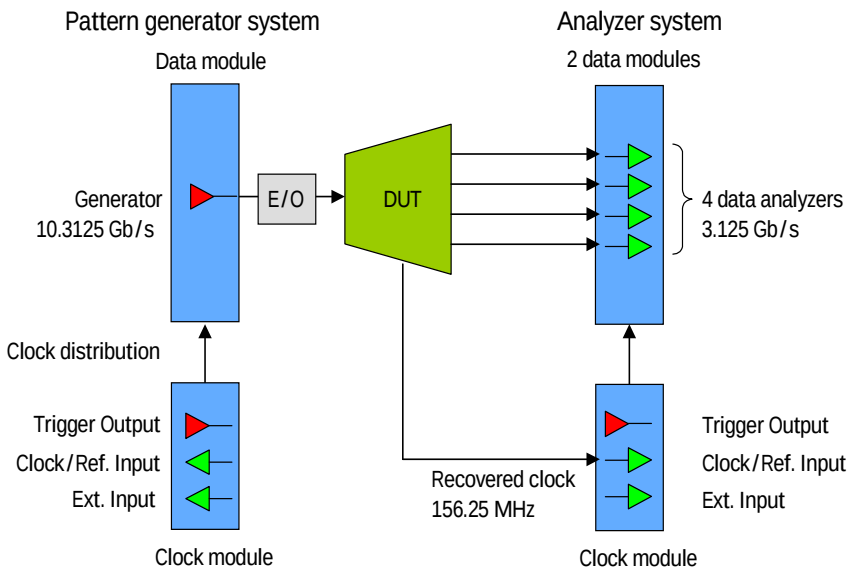
What you will learn

You will learn:

- How to set up the pattern generator system
- How to create the stimulating pattern
- How to set up the analyzer system
- How to use the 10 Gb Ethernet Tool for running the test
- How to set up additional XAUI tests

Hardware Setup

The hardware setup is illustrated in the figure below:



A ParBERT pattern generator applies a 10.3125 Gbit/s serial data stream to the DUT. An electrical-to-optical (E/O) converter generates the optical signal. The parallel DUT output on the XAUI side is captured by four 3.35 Gbit/s analyzers.

The DUT in this example has its own Clock Data Recovery (CDR) circuit. It generates a clock signal in the range of 156 MHz. This clock is fed into the CLOCK/REF INPUT of the analyzer system's clock module.

This setup, of course, refers to a certain type of DUT. For completely synchronous operation, an external clock generator could be used as well. You may also consider using an additional analyzer for conditioning the recovered clock.

TIP After setting up the hardware and connecting the cables, a *cable and propagation delay compensation* procedure has to be performed. This is a general requirement for every test setup and should be done at the expected channel frequencies. The procedure is described in the section *How to Compensate for Internal and External Delays* of the *ParBERT System User Guide*.

Pattern Generator Setup

Proceed as follows:

1 Start the ParBERT user interface for the generator system.

2 Create a one-terminal DUT input port and connect the terminal.

TIP Using the mouse, drag the connector from the *Modules* section to the *Device Under Test* section and drop it on the green *Data Port Area*.

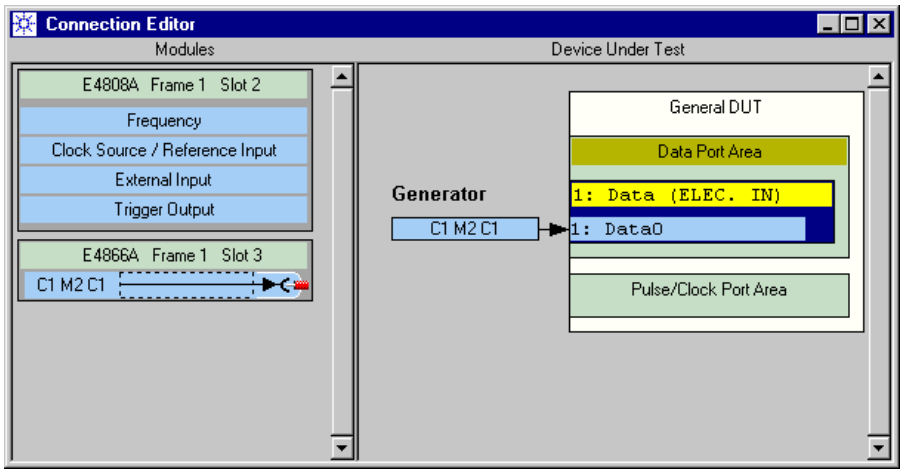


Figure 16 Connection Editor of the Pattern Generator System

3 Set the system clock frequency to 10.3125 GHz.

To open the Parameter Editor, double-click the *Frequency* field of the clock module in the *Modules* section of the Connection Editor.

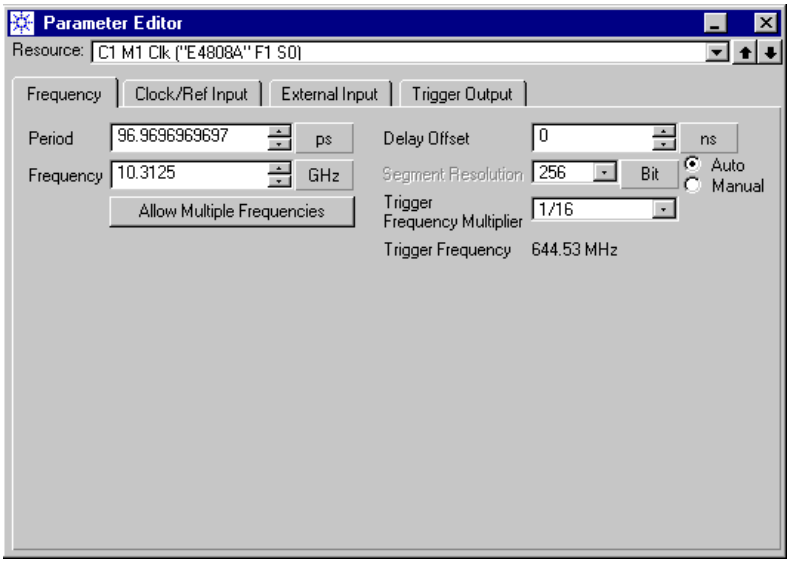


Figure 17 Clock Frequency Setting of the Pattern Generator System

Note that for this system with a 10.8G module, the general *Segment Resolution* is automatically set as required.

4 Close the Parameter Editor window.

You will now:

- Specify the generator output parameters (see *"Setting the Output Characteristics" on page 50*)
- Create the data segment to be used for the test (see *"Creating the Data Segment" on page 51*)
- Create the data sequence (see *"Specifying the Generator Sequence" on page 56*)

Setting the Output Characteristics

You have to adapt the signal voltages and expected termination to the properties of the DUT. In this example, the requirements are given by the electrical-to-optical converter.

1 In the *Modules* section of the Connection Editor, double-click the channel identifier.

   This opens the Parameter Editor for setting the output parameters.

   Alternatively, you could also double-click the port or terminal in the *Device Under Test* section.

   We keep the default timing.

2 Open the *Levels* page.

   We use the following levels and termination:

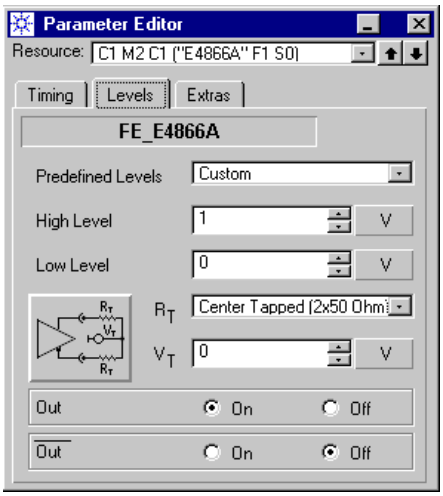


Figure 18 Pattern Generator Output Parameters

   Our E/O converter has a single input; a signal voltage between 0 V and 1.0 V is adequate.

3 Close the Parameter Editor window.

Save the setting

   This is not a must but highly recommended:

4 Open the *File* menu and choose *Save Setting As ...*

5 Save the setting under the name **`XAUI_GEN`**.

   Once the setting has been saved, you can always return to the present status.

After you have saved the setting for the first time, it is recommended to update it occasionally and save the last changes by clicking the Save Setting button.

Creating the Data Segment

A segment for 10GbE tests must contain one or several full 10GbE frames plus IPGs. It must also conform to the segment resolution given by the ParBERT hardware. Such segments can be created with the 10Gb Ethernet Tool.

1 Start the 10Gb Ethernet Tool.

If you have not yet put a link onto your desktop, select *Programs – Agilent Digital Verification Tools – Utilities – 10G Ethernet Tool* from the Windows Start menu.

The tool comes up with the *Connection* page:

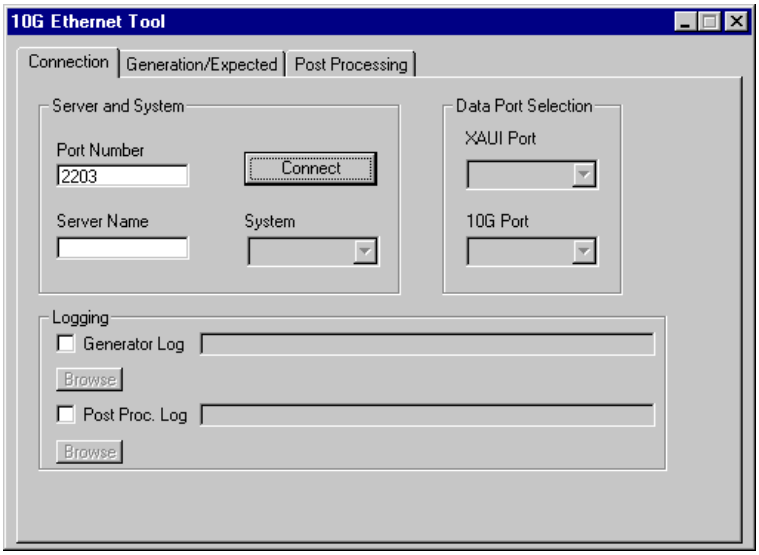


Figure 19 10Gb Ethernet Tool Connection page

NOTE You do not have to connect to the stimulating system. You can skip this page. But connecting is easy and convenient. When you are connected, you can transmit the generated segment directly to the stimulating system.

2 If the ParBERT firmware server is running on a remote computer, enter the network name of this computer in the field *Server Name*, for example 'bid118dc'. Do not enter leading slashes.

If the firmware server is running on your computer, leave the field *Server Name* empty.

3 Click the Connect button to connect to the firmware server.

4 Select the generator system from the *System* list.

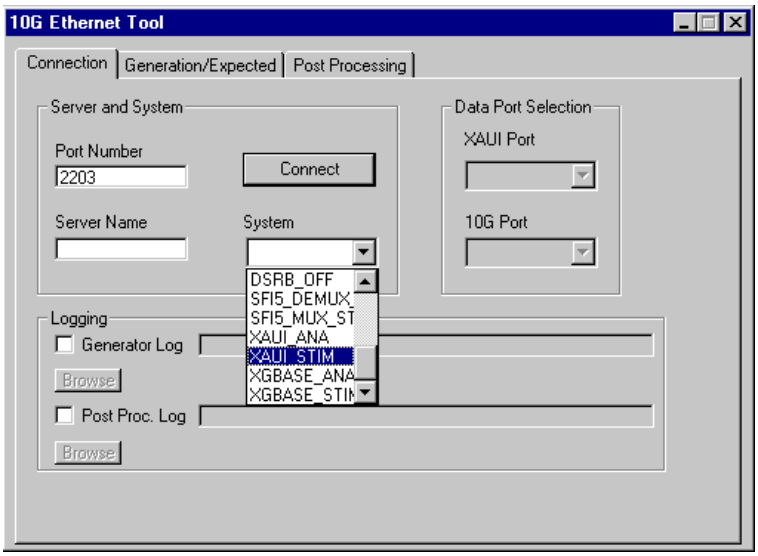


Figure 20 Generator System Selection

TIP By default, the ParBERT software identifies available systems as DSRA, DSRB, DSRC, and so on, and additionally provides some offline systems for demonstration and learning purposes. You can assign your own system names by editing the file `dvtsys.txt` in the ParBERT subdirectory "`cfg`".

5 Open the page *Generation/Expected*.

This opens the 10GbE frame generator.

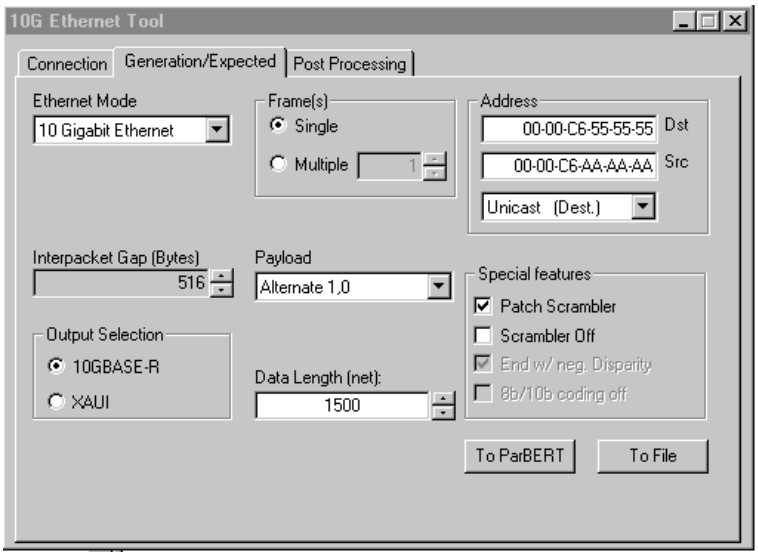


Figure 21 Generation / Expected Page

6 In the *Frame(s)* box, enable *Multiple* and set the value to 100.

We will generate a segment holding 100 frames (plus IPGs).

This is not absolutely mandatory, but we will keep the *Patch Scrambler* enabled. That means that the last frame may be patched and therefore discarded by the post processor at the analyzing side.

Generating 100 frames ensures that 99 frames will be evaluated (see also *"Treatment of Patches" on page 28*).

7 Set the *Payload* to PRBS 31.

We use a pseudo random bit stream of polynomial $2^{31}-1$ for this test.

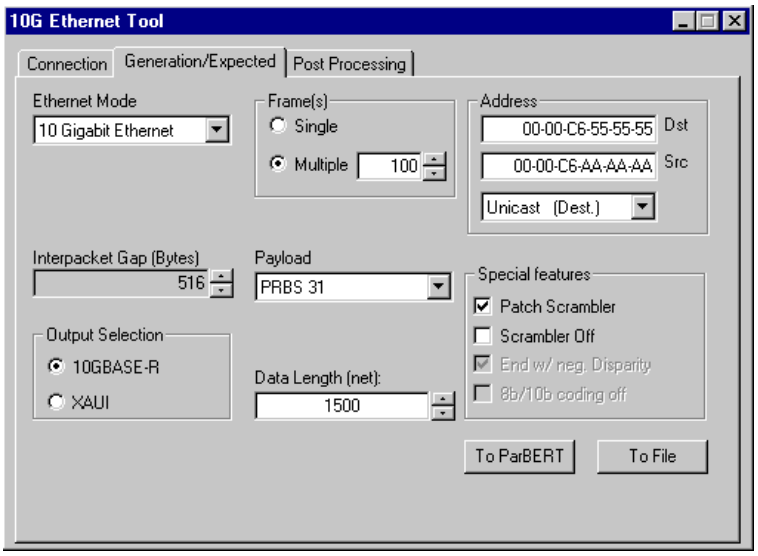


Figure 22 Ethernet Frame Generator Setup

We have now specified a ParBERT segment, coded for 10GBASE-R, that holds 100 frames, each with 1500 bytes of PRBS data. The PRBS polynomial is $2^{31}-1$. To achieve a reasonable ratio between patched and unpatched frames, (the last frame will be patched) we have included 100 frames into the segment.

8 Click the To ParBERT button.

This button is only available if you are connected to a pattern generator system. If not, you have to store the segment in a file and import it afterwards.

9 Enter a segment name and click *OK*.

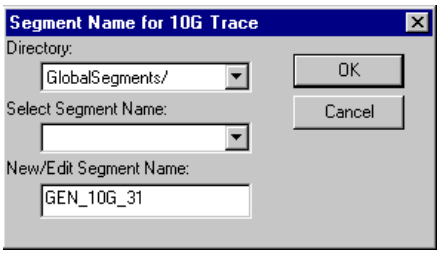


Figure 23 Segment Transfer Dialog

NOTE The proposed (and recommended) directory is the global segments pool. This ensures that the segment can then be accessed from all system settings. You can also choose the local segments pool, but then the segment is only accessible from your present setting.

10 Do **not** terminate the 10Gb Ethernet Tool.

You will need the same setup on the analyzing side for the post-processor of the 10Gb Ethernet Tool.

11 Return to the ParBERT user interface and start the Segment Editor.

Click the Segment Editor icon and select the generated segment.

12 Check the length of the segment.

TIP Right-click the address column and choose the decimal format.

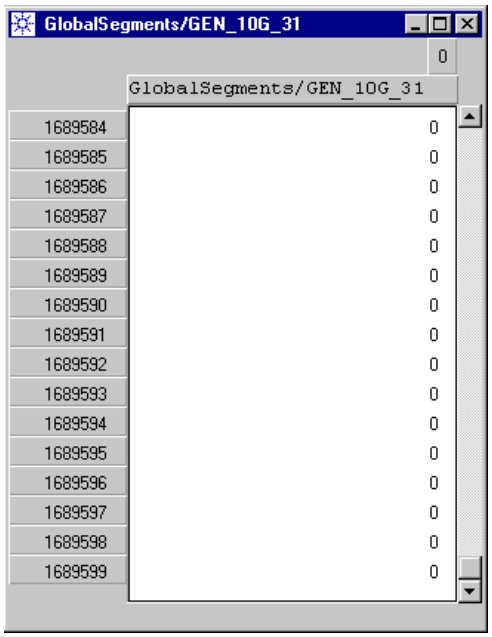


Figure 24 Checking the Segment Length

Note that the segment contains 1,689,600 vectors (see also *“Calculating the Segment Length” on page 85*).

Specifying the Generator Sequence

The sequence of generated and expected data can be specified with one of three available Sequence Editors.

1 Click the Sequence Editor button.

This opens the Standard Mode Sequence Editor.

The Standard Mode Sequence Editor shows one port with one terminal. The default segment is PAUSE0. That means for the associated generator “keep zero voltage”.

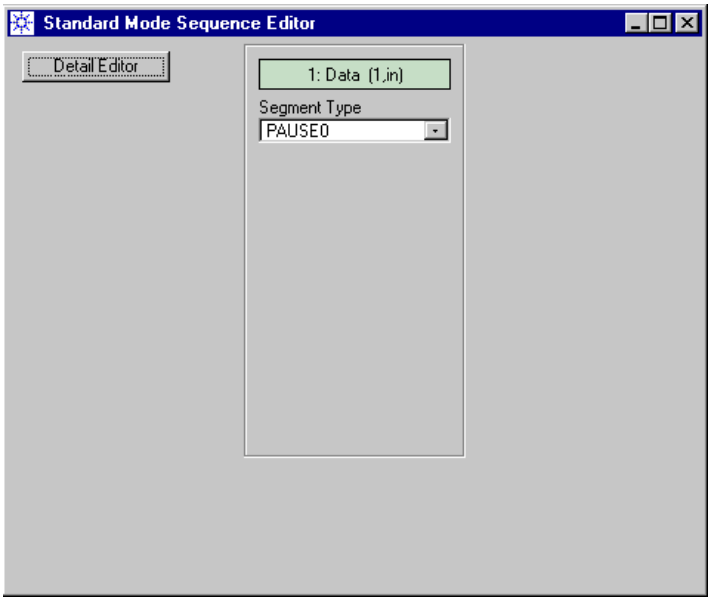


Figure 25 Empty Sequence of the Pattern Generator

2 Switch to the Detail Mode Sequence Editor.

The Detail Mode Sequence Editor shows one block that is endlessly looped.

3 Right-click the segment name and choose *Select Segment*.

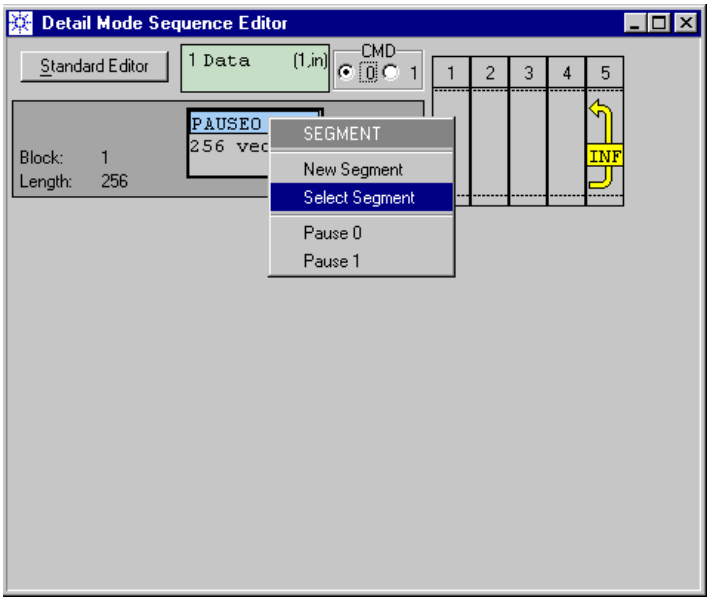


Figure 26 Segment Context Menu

4 Replace the default segment by the previously generated segment.

5 Adjust the block length to the length of the segment.

Double-click the block area and enter the correct length.

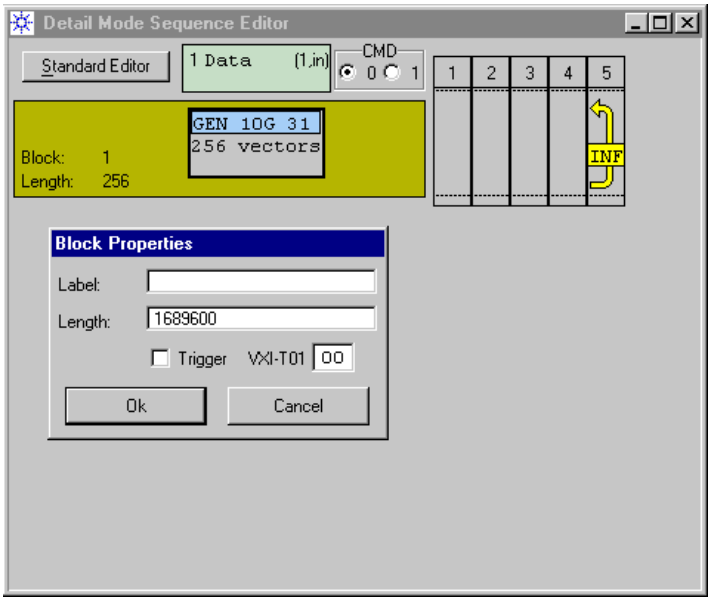


Figure 27 Adjusting the Block Length

Once it is started, the generator system will now continually generate 10 GbE formatted frames until you click the Stop button.

Now that you are done with the generator system, it might be a good idea to update its setting:

6 Click the Save Setting icon.

Pattern Analyzer Setup

This example requires two ParBERT systems and hence two ParBERT user interfaces.

On the XAUI side, we use a system with four analyzers. After starting the user interface of that system, the Connection Editor appears as shown in the figure below:

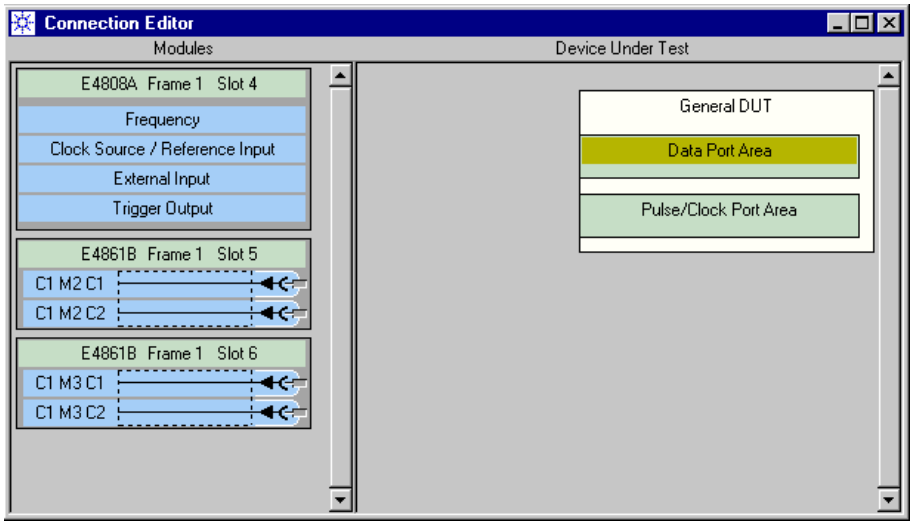


Figure 28 Connection Editor of the Analyzer System

You will now:

- Set up the connections to the DUT (see *"Setting Up the Analyzer Connections" on page 60*)
- Set the analyzer system frequency (see *"Setting the Analyzer System Clock Frequency" on page 61*)
- Specify timing, expected voltages and termination (see *"Setting Port Parameters" on page 64*)
- Set the measurement mode (see *"Setting the Measurement Mode" on page 65*)
- Define the test sequence (see *"Specifying the Analyzer Test Sequence" on page 66*)

NOTE You should keep in mind that the analyzer system requires a cable and propagation delay compensation. This is done with the Deskew Editor.

The procedure is described in the section *How to Compensate for Internal and External Delays* of the *ParBERT System User Guide*. It will not be discussed in this example.

The compensation should be performed at a system clock frequency as close to the final test frequency as possible.

Setting Up the Analyzer Connections

ParBERT offers you many ways to to set up ports, terminals, and connections. The fastest way is the following:

1 Drag the green title of the upper data module to the *Device Under Test* section and drop it on the green *Data Port Area*.

   This creates a DUT output port with two connected terminals.

2 Drag the green title of the second data module to the *Device Under Test* section. Position the cursor on the lower border line of the port (the border turns from blue to red) and drop it there.

   This appends two connected terminals to the port.

   The result is shown in the figure below:

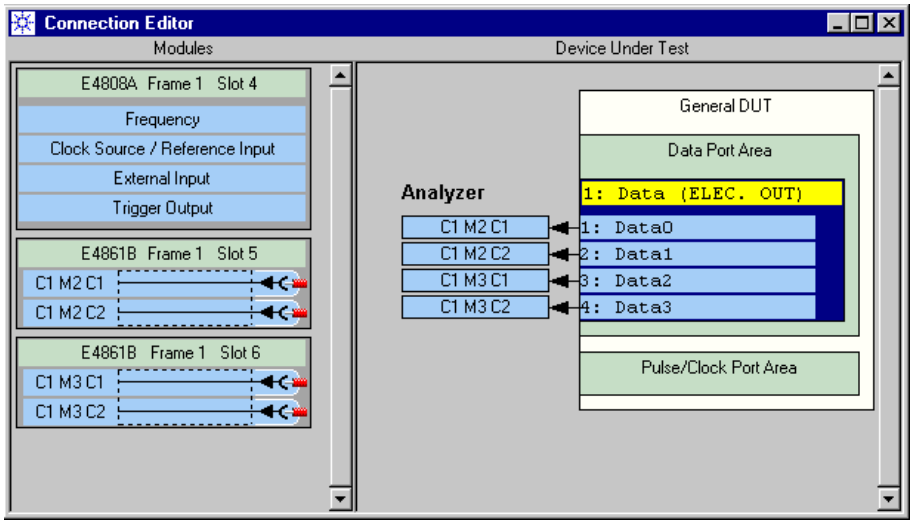


Figure 29 DUT Connections

Note that you have to make the physical connections of the four XAUI lanes accordingly.

Setting the Analyzer System Clock Frequency

The test setup shown in *"Hardware Setup" on page 47* requires that the generator system is running. The DUT is installed and working and delivers the clock signal which is fed into the analyzer system's clock module.

The frequency of the external source clock must exceed 1.302083 MHz. The maximum frequency is 10.8 GHz for the E4808A clock module.

Start the Generator System

1 Connect the output of the generator system to the DUT.

2 Connect the clock output of the DUT to the CLOCK/REF INPUT of the analyzer system's clock module.

3 Apply power to the DUT.

4 Click the Run button of the generator system.

From now on, the DUT receives a continuous serial data stream. It recovers the clock signal that will be used by the analyzers.

Set Up the Analyzer Clock

To use the external clock signal:

1 In the Connection Editor, double-click *Frequency*.

This opens the Parameter Editor for the clock module.

2 Set the global *Segment Resolution* to 128.

This is the minimum segment resolution for frequencies above 2.7 GHz (see also the section *Timing Principles* in the *ParBERT System User Guide*).

3 Set the *Trigger Frequency Multiplier* to 1/16.

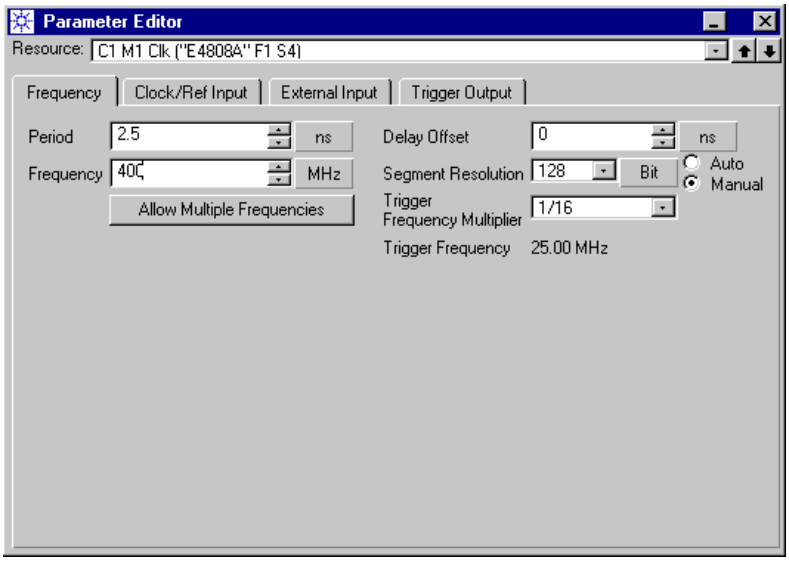


Figure 30 Frequency Page of the Parameter Editor

TIP You can also set the TRIGGER OUTPUT of the clock module to *Sequencer* mode. When this is done, you do not have to worry about the *Trigger Frequency Multiplier*.

4 Open the Clock/Ref Input page.

5 Click the Measure button.

The external clock frequency is measured and indicated.

6 Use the *Clock Multiplier* to achieve the desired analyzer system frequency.

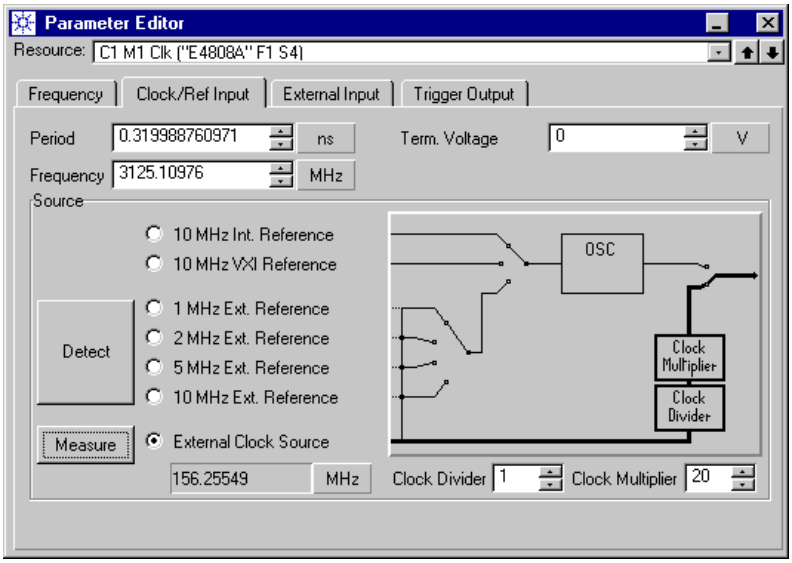


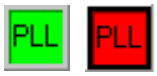
Figure 31 Clock / Ref Input Page of the Parameter Editor

We have multiplied the external clock frequency by 20.

7 Close the Parameter Editor window.

TIP As long as the test (and this example) is not complete, do **not** stop the run of the generator system. The pattern generator system continually feeds the DUT, which in turn generates the clock signal onto which the analyzer system has locked.

If you would stop the stimulator system, the green PLL indicator in the upper right-hand corner of the analyzer system would turn to red.



This indicates that the phase locked loop of the analyzer system has lost its clock synchronization. In order to re-synchronize, you would have to repeat the procedure described in this section.

Save the setting

This is a good moment for saving the analyzer setting.

8 Use *File – Save Setting as ...* to save the setting under the name **XAUI_ANA**.

Once the setting has been saved, you can always return to the present status.

After you have saved the setting for the first time, it is recommended to update it occasionally and save the last changes by clicking the Save Setting button.

Setting Port Parameters

The properties of the signal analyzers have to be set up according to the characteristics of the DUT. You can set up all the channels connected to a port in one go.

1 In the Connection Editor, double-click the DUT output port.

This opens the Parameter Editor for that port. It comes up with the *Timing* page.

2 Set a suitable *Start Delay*.

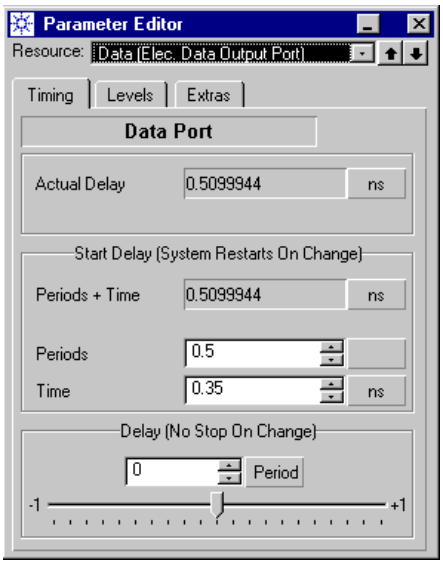


Figure 32 Port Timing Parameters

NOTE The analyzer start delay is a very critical parameter. We will use the post-processor of the 10Gb Ethernet Tool and therefore just capture data. In this mode, the automatic synchronization methods cannot be used, because we cannot specify expected data.

That means, you have to find the optimum sampling delay by other means. It can even happen, that the port delay is not the optimum for all four channels. See also *"XAUI Test Analyzer Setup Procedure" on page 35*.

3 Open the *Levels* page.

4 Choose the *Frontend Mode*, the *Analyzed Inputs*, and the *Termination*.

We expect a low voltage differential signal. Your level setup may look as shown below:

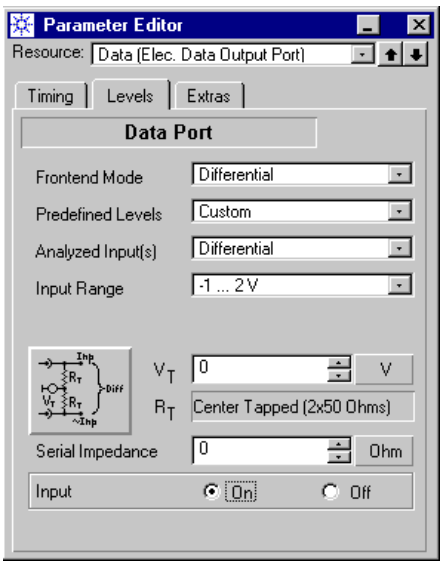


Figure 33 Port Level Parameters

5 Close the Parameter Editor window.

Setting the Measurement Mode

The measurement mode has an impact on the segments that can be used in the data sequence. For example, you cannot acquire data if a BER test is specified.

To avoid unnecessary error messages, it is recommended to set the measurement mode before creating the sequence.

1 Click the Measurement Configuration button.

2 Enable *Capture Data*.

This is the mode to be used in conjunction with the post-processor of the 10Gb Ethernet Tool.

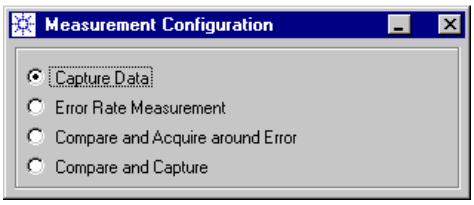


Figure 34 Measurement Configuration Window

3 Close the Measurement Configuration window.

Specifying the Analyzer Test Sequence

We will use the Detail Mode Sequence Editor for the analyzer system. The post-processor of the 10Gb Ethernet Tool requires a sequence the Standard Mode Sequence Editor cannot handle.

1 Click the Sequence Editor button.

The Standard Mode Sequence Editor shows one port.

2 Switch to the Detail Mode Sequence Editor.

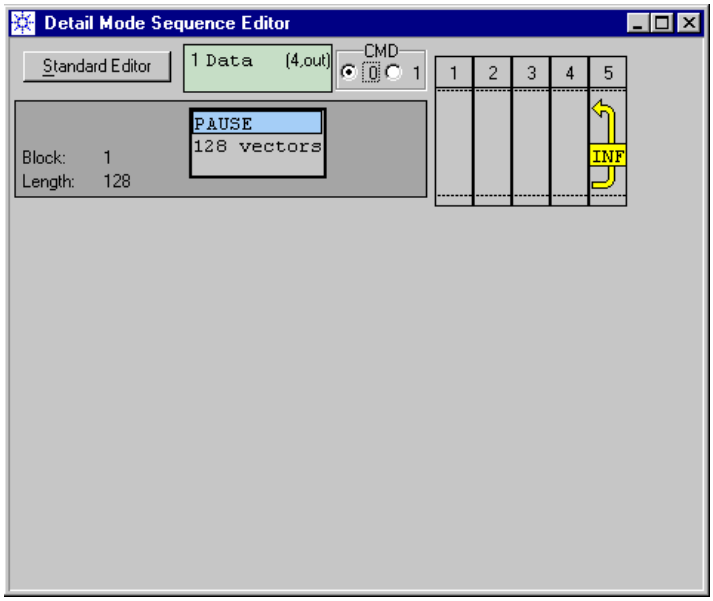


Figure 35 Detail Mode Sequence Editor of the Analyzer System

The Detail Mode Sequence Editor shows one block that is endlessly looped.

3 Right-click the infinite loop and delete it.

4 Right-click the segment name and select *Acquire*.

NOTE In Capture Data mode, the only available segments are *Pause* and *Acquire*. When *Acquire* is chosen, the system will capture data until the sequence expires or the capture memories are full—whatever comes first.

5 Increase the block length.

Double-click the grey block area.

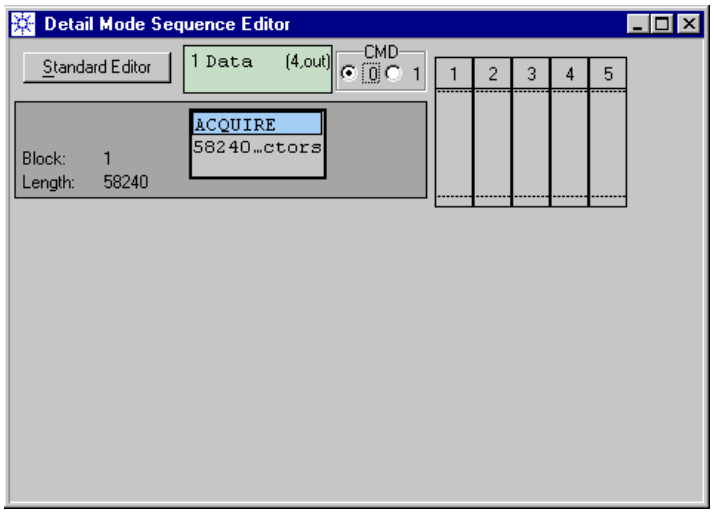


Figure 36 Creating the Data Port Sequence

We have set the block length to 58,240 vectors in this example.

NOTE For E4861B modules, you can increase the block length up to 16,777,216 vectors. With the maximum setting, you can measure bit error rates down to 6×10^{-8} in one go.

The block length has an impact on the duration of every single measurement. But uploading and processing 64 MB of captured data takes its time.

You can also choose a moderate block length and repeat the measurement a couple of times. The post-processor supports multiple measurements and accumulates the results after each measurement. This allows you to measure lower bit error rates.

Considering the settings we have made for the 10GBASE-R pattern generator, our system will capture 13 corresponding XAUI frames (see also *"Calculating the Segment Length" on page 85*).

TIP A moderate block length (just some frames) and multiple measurements are recommended if you need to find out the optimum sampling delay. While data is captured, you can fine-tune the delay with the Parameter Editor and do not have to wait long for the results.

Running the Test

We are now going to use the 10Gb Ethernet Tool again. If you have followed the procedure given in this example, it is still active and shows the following page:

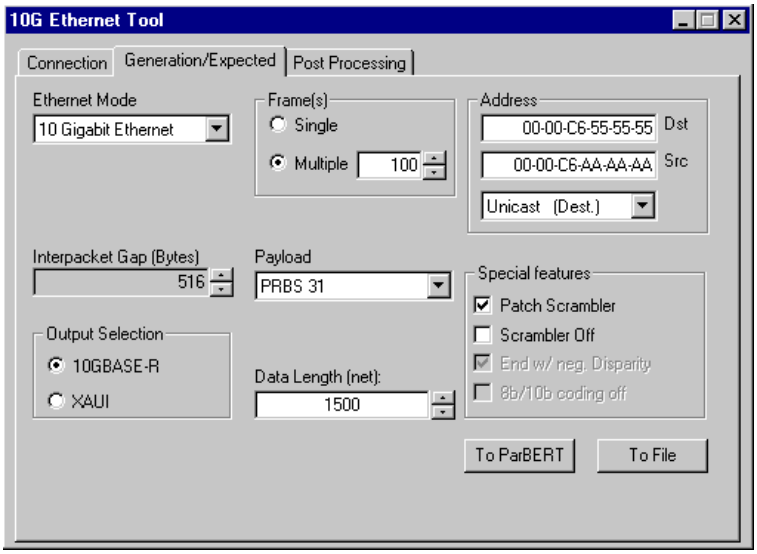


Figure 37 Ethernet Frame Generator Setup

This page defines not only the generated data, but also the data expected by the post-processor.

Proceed as follows:

1 Open the *Connection* page.

2 Click the Connect button.

3 Select the analyzer system from the *System* list.

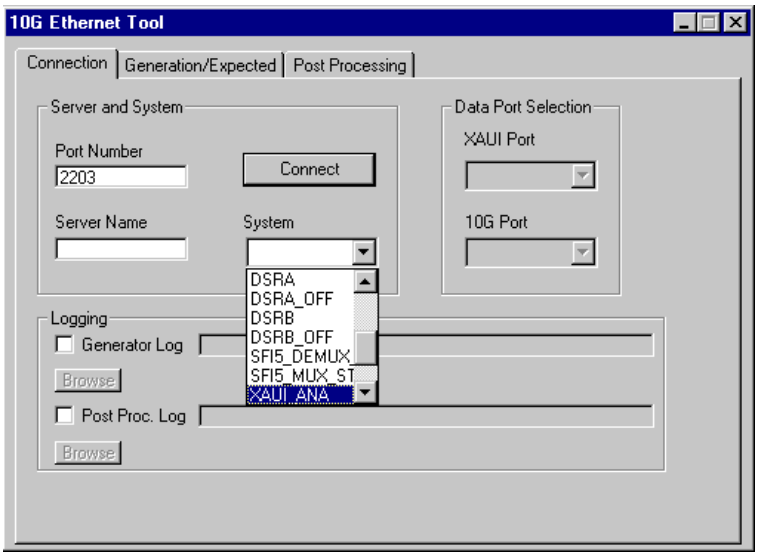


Figure 38 Analyzer System Selection

You can now control the start and stop of the analyzer system from the 10Gb Ethernet Tool.

The 10Gb Ethernet Tool also identifies the DUT output ports of the connected system. If the system has more than one acceptable port, select the port that shall be used for the test.

4 Open the *Post Processing* page.

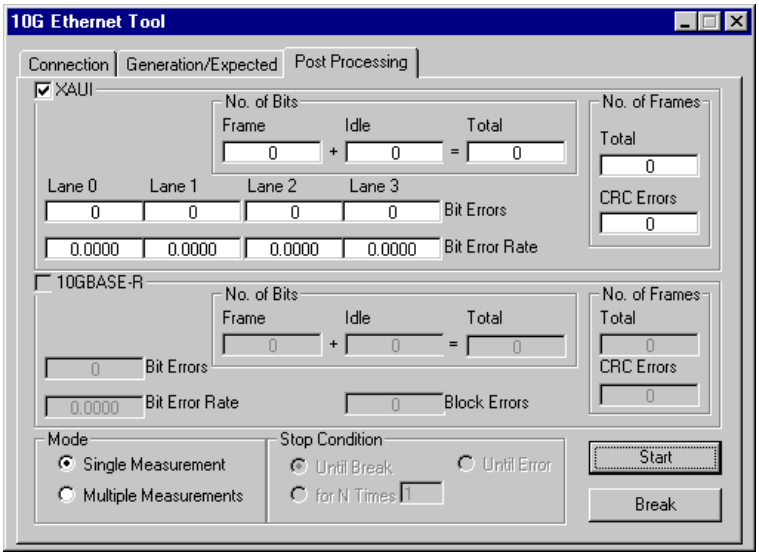


Figure 39 Default Post-Processing Page

The XAUI test results panel is automatically enabled.

5 Set the *Mode* to *Multiple Measurements*.

A single measurement runs once. After it has finished, the Post Processing page shows the results.

A multiple measurement runs repeatedly. The Post Processing page is updated after each measurement and shows the accumulated results.

6 Set the *Stop Condition* to *Until Break*.

This is the default. The measurement will be repeated until you click the Break button.

TIP Measuring very low bit error rates takes time. With this setup, you can run the test over night.

7 Click the Start button to start the analyzer system.

Observe the results.

8 Click the Break button to stop the analyzer system.

Your final result may look as shown below:

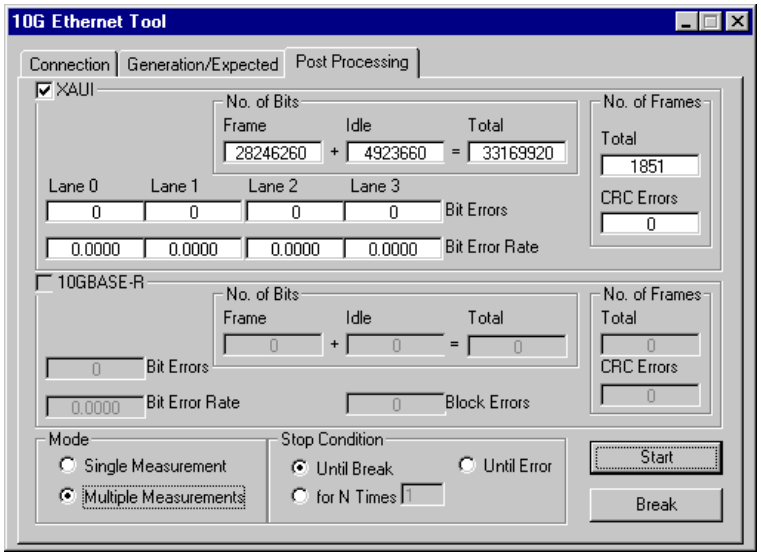


Figure 40 XAUI Test Results

For an explanation of the results, please refer to *"Interpreting the Test Results" on page 90*.

Setting up Additional XAUI Tests

In Annex 48A, the IEEE 802.3ae specification defines five jitter test patterns for XAUI:

- High frequency (HF) test pattern
- Low frequency (LF) test pattern
- Mixed frequency (MF) test pattern
- Continuous random test pattern (CRPAT)
- Continuous jitter test pattern (CJPAT)

The ParBERT software provides these patterns in the form of memory type segments that can be imported into any ParBERT system (see also *"Generating 10GbE Formatted Data" on page 81*).

These segments are ready for use—that means, they consider both pattern and ParBERT requirements. You do not have to bother about fitting segment and block lengths.

The segments are available for generators as well as for analyzers. In combination with these segments, you can use the automatic methods for analyzer sampling point adjustment and perform standard BER tests or use the ParBERT Measurement Software.

TIP The sampling delays found by automatic synchronization can help you to determine the *Start Delay* for direct in-to-out measurements (from 10GBASE-R to XAUI and vice versa). The resulting delays can be inspected by double-clicking the terminals or channels in the Connection Editor. Please refer to the *ParBERT System User Guide*.

The stimulating system generates the chosen pattern in an infinite loop. The XAUI loop-back function of the DUT may be used for testing the XAUI output.

This section gives you some hints on how to set up a suitable analyzer test sequence.

Analyzer Sequence for CRPAT / CJPAT

For these patterns, Automatic Bit Synchronization is recommended. The software provides for each of the two patterns one segment for synchronization and one segment for the test.

A sequence for a test with CRPAT might look as shown in the following figure:

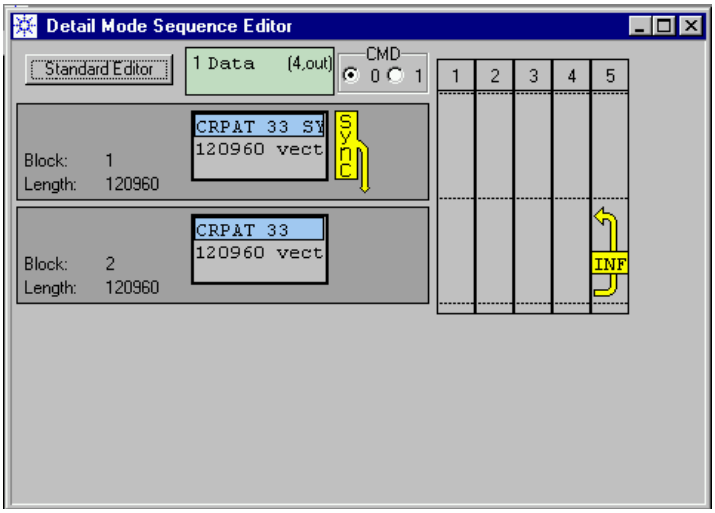


Figure 41 Analyzer Sequence for CRPAT

We have enabled Automatic Bit Synchronization.

The synchronization block holds the segment CRPAT_33_SYNC. The measurement block holds the segment CRPAT_33. Both segments have been imported from the "`Eth10G_XAUI_Analyzer`" subdirectory. Their only difference is the state coding. The sync segment allows you to ignore bits.

The sync block is looped until the sync criteria are fulfilled. The measurement block is endlessly looped.

The block length has been set according to the segment length.

The segment length of 120,960 vectors is the minimum common multiple of 1512 (the CRPAT packet length in octets, including the IPG) and 128 (the minimum ParBERT segment resolution for frequencies above 2.7 GHz).

Similar segments are provided for CJPAT. These segments have a length of 122,240 vectors. This is the minimum common multiple of 1528 (the CJPAT packet length in octets, including the IPG) and 128.

Analyzer Sequence for HF, LF, MF Test Patterns

These patterns are not formatted.

They have no unique detect word which is required for Automatic Bit Synchronization. But Automatic Delay Alignment can be used.

A sequence for a test with HF, LF, or MF test patterns might look as shown in the following figure:

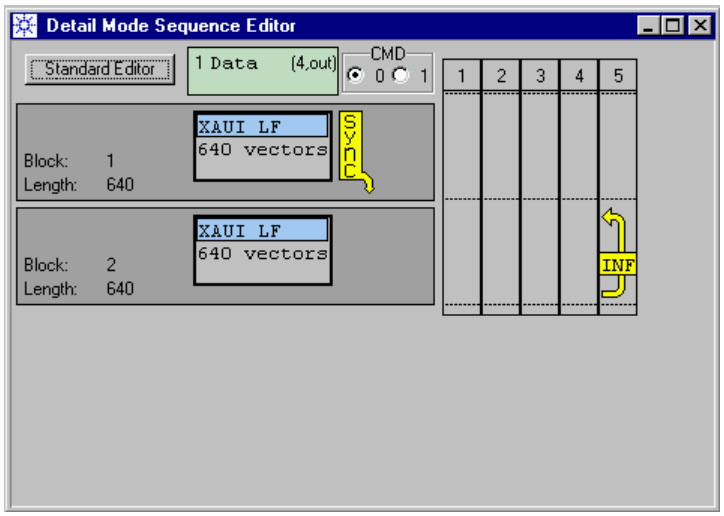


Figure 42 Analyzer Sequence for a LF Pattern

We have enabled Automatic Delay Alignment.

The synchronization block and the measurement block refer to the segment XAUI_LF. The segment has been imported from the "`Eth10G_XAUI_Analyzer`" subdirectory.

The block length conforms to the segment length.

The segment length of 640 vectors is five times 128 (128 is the minimum ParBERT segment resolution for frequencies above 2.7 GHz).

You may wish to increase the segment and the block length to 20 × 128 or a multiple thereof. A low frequency pattern repeats after 10 octets, a mixed frequency pattern after 20.

Using the 10Gb Ethernet Tool

You can start the 10Gb Ethernet Tool from the *Utilities* panel of the *Agilent Digital Verification Tools*.

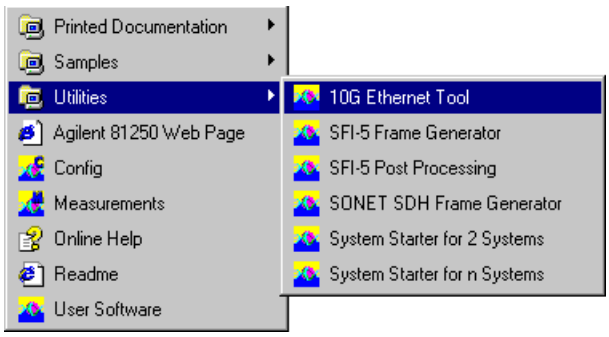


Figure 43 Agilent Digital Verification Tools Utilities Panel

The 10Gb Ethernet Tool has three pages:

- On the *Connection* page, you can connect to a running firmware server and to any suitable ParBERT system defined for this server.
- On the *Generation/Expected* page, you can generate ParBERT memory-type data segments. These segments contain either 10GbE-formatted data frames with selectable payload or data patterns as defined in the IEEE 802.3ae specification.
- On the *Post Processing* page, you can control the post-processor, execute tests, and investigate the results.

For details see:

- *"How to Connect to a ParBERT System" on page 76*
- *"How to Use the 10GbE Frame Generator" on page 80*
- *"How to Use the 10GbE Post-Processor" on page 88*

How to Connect to a ParBERT System

Once it has been started, the 10Gb Ethernet Tool shows its *Connection* page.

If a ParBERT firmware server is running locally (on your computer) or remotely (in your LAN), this page allows you to connect to that server and to communicate with any appropriate system it provides.

When Should You Connect?

Connection to the data generator

Connecting to a stimulating ParBERT system is optional. You can store every generated pattern in a file and import that file later into the stimulating system.

However, if you wish to set up a test with 10GbE-formatted data frames quickly and efficiently, connecting to the stimulating ParBERT system is recommended. Once you are connected to the stimulating system, you can transfer the generated data segment(s) directly into the global or local segment pool of the generator system.

NOTE This works only for 10GbE-formatted data. If you wish to generate unformatted test patterns, these have to be saved in files.

Connection to the data analyzer

Connecting to the capturing ParBERT system is mandatory if you wish to use the 10GbE post-processor. The post-processor can only be used when the 10Gb Ethernet Tool is connected to the capturing ParBERT system.

Prerequisites for the Connection

Before the connection can be established, the following requirements have to be met:

- The ParBERT firmware server must be up and running, either on your computer or somewhere in the LAN.
- Once you are connected to the firmware server, you have to choose a ParBERT system. This system should meet the requirements for testing 10GbE devices (see *"Prerequisites" on page 19*).
- At least one data port must be set up on that system.

- The successful connection to a *capturing* system requires additionally that at least one 1-terminal or a 4-terminal DUT output port is defined on this system.

The ParBERT system can be set up manually with the Connection Editor or by loading an appropriate setting.

Making the Connection

The *Connection* page looks as shown below:

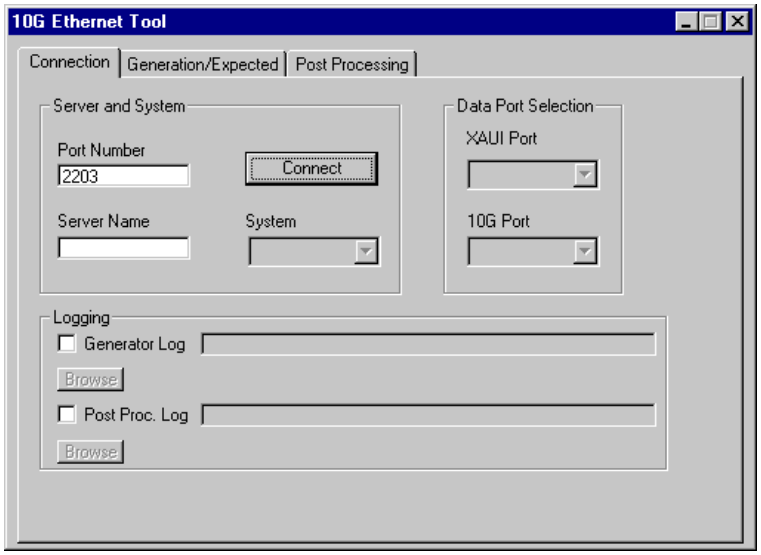


Figure 44 Connection Page

To establish the connection, proceed as follows:

1. If the ParBERT firmware server is running on a remote computer, enter the network name of this computer in the field *Server Name*, for example 'bid118dc'. Do not enter leading slashes.

   If the firmware server is running on your computer, leave the field *Server Name* empty.

2. Click the Connect button to connect to the firmware server.

3 Select a system from the *System* list.

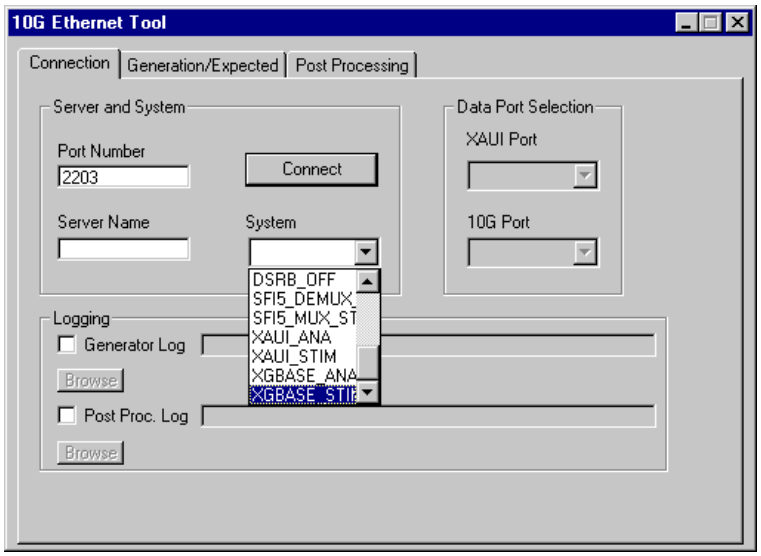


Figure 45 System Selection

If the chosen system has no DUT with data ports, the message

"*Unable to set port Information*"

will be displayed.

4 If you have chosen a system with suitable DUT *output* ports (that means, one or four terminals wide), the port names are displayed in the *Data Port Selection* box.

If the chosen system has more than one suitable DUT output port, choose the port you wish to use for capturing and post-processing data from the corresponding drop-down list.

5 Decide on creating log files.

You can generate log files of the last generated segment and/or the post-processor operation. You can specify directories and names for the log files.

The log files are ASCII files that can be inspected with any text editor.

Be aware that the generated log files consume disk memory. Post-processing log files of multiple measurements can consume some 10 MBytes of disk space.

Changing the Connection

When you are setting up a 10GbE test, you may wish to change the connection.

For example, you first connect to the stimulating system, create a suitable data segment with the 10Gb Ethernet Tool, and transfer the generated segment to that system. If you now wish to use the post-processor, you have to change the connection.

To connect to a different system:

1 Click Connect.

2 Choose the new system from the *System* list.

How to Use the 10GbE Frame Generator

The frame generator allows you to generate ParBERT segments that contain

- 10GbE-formatted data frames with arbitrary payload
- Test patterns as defined in the IEEE 802.3ae specification

The frame generator is controlled from the *Generation/Expected* page. This name has been chosen, because the same page defines also the data expected by the post-processor.

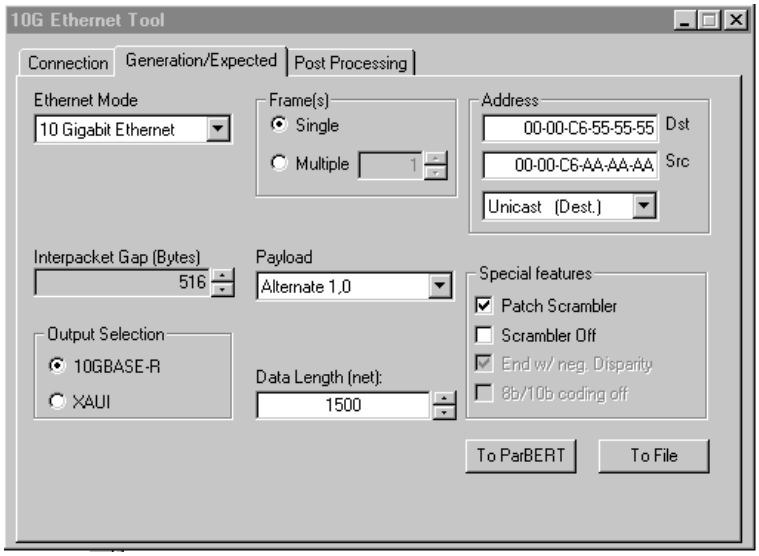


Figure 46 Generation / Expected Page

The *Ethernet Mode* browser makes it possible to switch the operating mode from generating 10GbE frames to test patterns.

Generating 10GbE Formatted Data

To generate a ParBERT memory segment with 10GbE-formatted data:

1 Keep the *Ethernet Mode* as *10 Gigabit Ethernet*.

2 Select the number of frames to be included in that segment.

– *Single* creates a segment with one single frame.

– *Multiple* allows you to include a number of frames into the segment.

Multiple is recommended, if you have activated the *Patch Scrambler* (active by default). If this option is enabled, a patch is inserted into the last frame to ensure that the segment can be repeated (looped) without resynchronization of the receiver.

If the payload is PRBS, patched frames will be ignored by the post-processor. If the payload is not PRBS, the post-processor will report bit and CRC errors for these frames.

If the *Patch Scrambler* is enabled, it is recommended to specify 100 or more repetitions to ensure an acceptable ratio between unpatched and patched frames.

3 Check the *Address* fields.

Destination and source address belong to every Ethernet frame. You can change the defaults.

If desired, you can also change the type of the destination address to *multicast* or *broadcast*.

4 Specify the *Payload*.

Choose from the list. Simple patterns and PRBS up to polynomial $2^{31} - 1$ are available. You can also specify your own binary file.

NOTE Frames with payload data from a file cannot not be evaluated by the post-processor.

5 Specify the *Data Length*.

This is the payload length in octets. You can choose between 46 and 1500.

6 Proceed to *Output Selection*.

Here, you decide wether the generated segment will have one trace (10GBASE-R) or four traces (XAUI).

This decision has an impact on the coding and therefore some more consequences. See also *"Pattern Generation" on page 13*.

7 Check the *Special Features*.

If you have enabled *10GBASE-R encoding*, you can:

– Disable/enable the *Patch Scrambler*.

With this checkbox, you can disable the insertion of patches. This can be useful if you are generating and post-processing frames with non-PRBS payload data.

– Disable/enable the *Scrambler*.

This refers to the scrambler built into a 10GBASE-R PHY. This feature enables you to create a segment that bypasses the scrambler.

If you have enabled *XAUI encoding*, you can:

– Disable/enable the *End With Negative Disparity*.

Ending with negative disparity is the default. This setting inserts patches (if necessary).

– Disable/enable the *8B/10B coding*.

By default, 8B/10B coding is enabled.

Your setup may now appear as shown in the figure below:

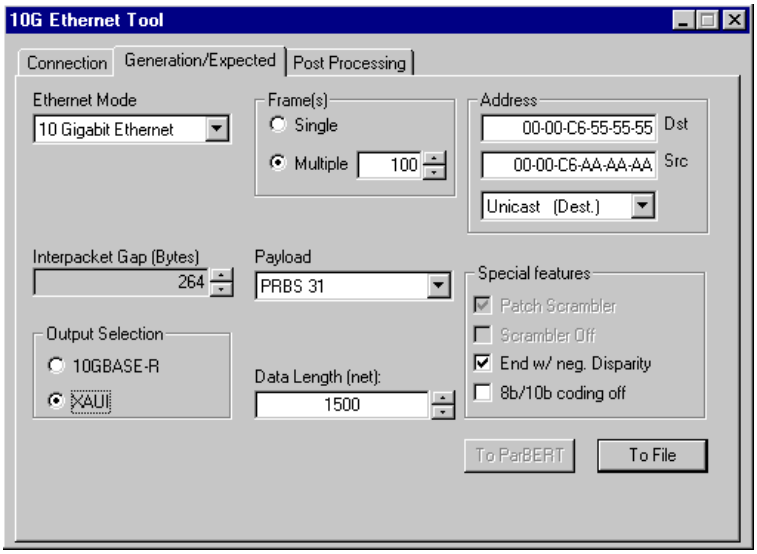


Figure 47 Ethernet Frame Generator Setup Example

Here, we have specified a frame, coded for XAUI, which holds 1500 bytes of PRBS data. The PRBS polynomial is $2^{31} - 1$. To achieve a good ratio between patched and unpatched frames, we will include 100 frames into the segment.

8 Check the length of the *Interpacket Gap*.

NOTE The *Interpacket Gap* (IPG) is automatically calculated. If you generate more than one frame, it applies to all generated frames.

The program calculates this value so that the generated Ethernet frame(s) including the IPG fit into a valid ParBERT segment. Segments used for 10GbE tests have to have a length that is a multiple of 64.

Changes of *Data Length*, *Output Selection,* and of the checkbox *8B/10B coding* affect the calculation as soon as such changes are confirmed by pressing the 'Tab' key.

Therefore, if you wish to change the length of the IPG, this should be the last step after all the other settings have been made.

You can increase or reduce the length of the IPG by clicking the up/down arrows. Then press the 'Tab' key.

If you have increased the IPG, it will be adjusted to the next higher possible length. If you have decreased the IPG, it will be adjusted to the next lower possible length.

9 Save the segment.

– If you have connected the 10Gb Ethernet Tool to the generator system, click To ParBERT.

  This is convenient. You can place the generated segment directly into the global or local segment pool of the connected system. You need only enter a name. Alternatively, you can also overwrite an existing segment.

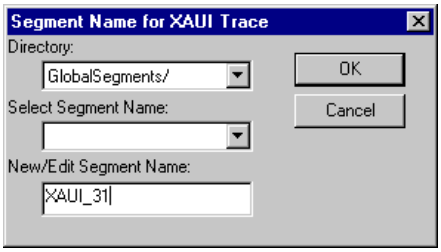


Figure 48 Segment To ParBERT Transfer Dialog

– To save the generated segment in a file, click To File.

Choose a directory and enter a file name.

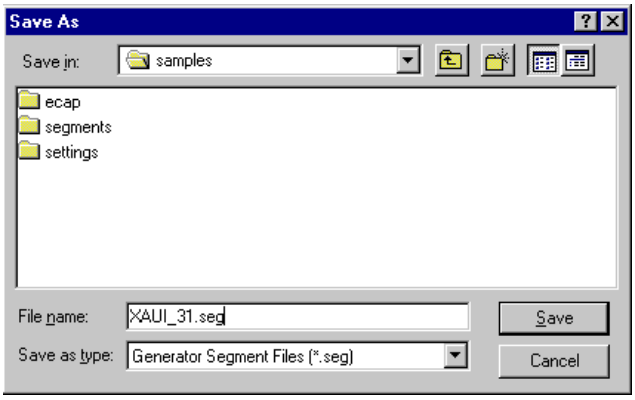


Figure 49 Segment To File Transfer Dialog

The generated file is an ASCII file. It has to be imported into the stimulating system. In the ParBERT user interface, choose *File – Import – Segments*.

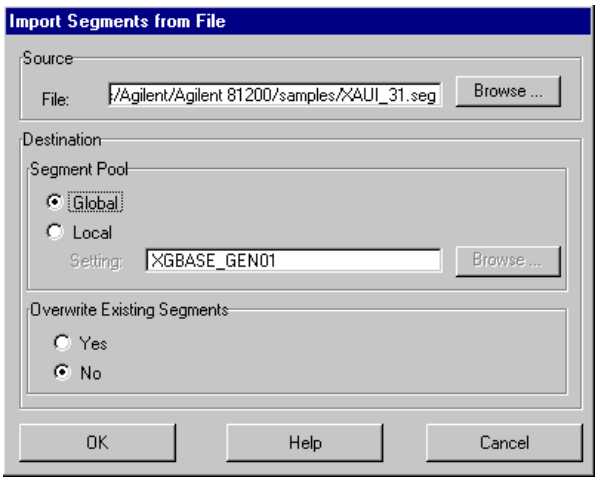


Figure 50 Segment Import Dialog

Once you have located the file, you can import it into the global or local segment pool.

Calculating the Segment Length

You may want to know how the length of a generated segment is calculated.

Here are two examples:

Assume you have specified one single frame with a payload length of 1500 bytes (octets).

10GBASE-R segment

A 10GBASE-R segment has one trace. The calculated IPG has a length of 516 bytes.

The framing data (preamble, SFD, destination and source address, length, CRC) consists of 26 bytes (see also *"Pattern Generation" on page 13*). Therefore:

```
Data to be transmitted = 1500 + 26 + 516 = 2,042 bytes =
16,336 bits (8-bit encoding)
```

This would yield 255.25 blocks of 64 bits each. Since only full blocks can be transmitted, we will send 256 blocks and fill the gap of 48 bits with six Idles.

256 blocks are then coded with 66 bits per block. This yields:

```
Final segment length = 256 × 66 = 16,896 vectors
```

XAUI segment

A XAUI segment has four traces that have to be filled. The calculated IPG has a length of 264 bytes.

The framing data (including terminator) consists of 27 bytes.

```
Data to be transmitted = 1500 + 27 + 264 = 1,791 bytes =
17,910 bits (10-bit encoding)
Preliminary segment length = 17,910 / 4 = 4,477.5 vectors
```

Since we cannot specify half vectors, we will add one Idle character and send 17,920 bits.

```
Final segment length = 17,920 / 4 = 4,480 vectors
```

Generating Test Patterns

NOTE If you have not accidentally deleted ParBERT files, test patterns for 10GbE devices are readily available. The samples include also the 'low frequency', 'high frequency' and 'mixed frequency' test patterns for XAUI.

These segments are stored as ASCII files (file names "`*_seg.txt`") in the following directories:

- `C:\Program Files\Agilent\Agilent 81200\samples\settings\Eth10G_10G_Analyzer`
- `C:\Program Files\Agilent\Agilent 81200\samples\settings\Eth10G_10G_Generator`
- `C:\Program Files\Agilent\Agilent 81200\samples\settings\Eth10G_XAUI_Analyzer`
- `C:\Program Files\Agilent\Agilent 81200\samples\settings\Eth10G_XAUI_Generator`

You can import these segments into any ParBERT system.

TIP Before you import one of the segments, it is recommended to read the `Readme.txt` file provided for each directory. It informs you about the contents of the segments.

Before importing a segment, it is also recommended to open it with a text editor and to inspect its title, because the segment name differs from the file name. This way, you can enter your own segment name before importing it.

NOTE The directories listed above contain also complete settings for each of the four systems described in *"Setup for Testing Both Sides" on page 22*.

These settings are stored as ASCII files (file names "`*_set.txt`"). They can be imported and then loaded into ParBERT systems that have precisely the required minimum configuration. Because settings are hardware dependent, they cannot be loaded on systems with different hardware.

TIP Before you import one of the settings, it is recommended to open it with a text editor and to inspect it.

It informs you about the hardware requirements and (for generator systems) the segment that is going to be used.

To generate test patterns with the 10Gb Ethernet Tool:

1 Open the *Ethernet Mode* browser.

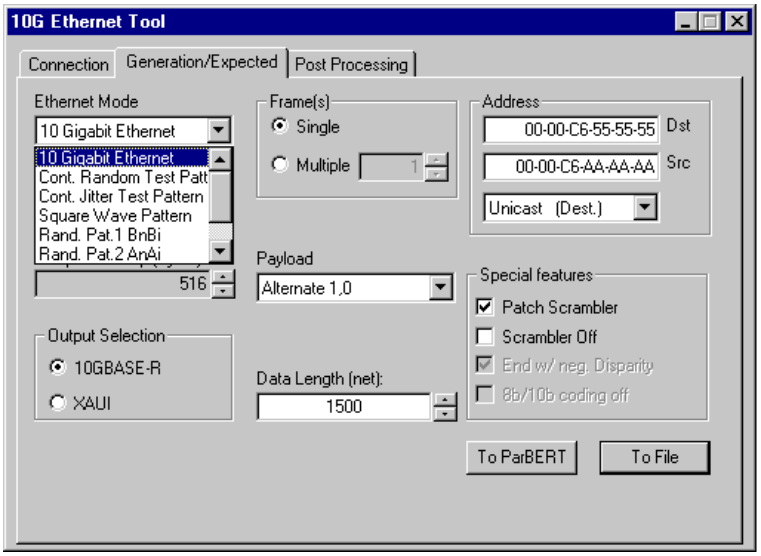


Figure 51 Selecting a Pattern

2 Choose a pattern from the list.

Once you have chosen a pattern, only the To File button remains active.

The patterns conform to the IEEE 802.3ae specification. They are:

- Continuous random test pattern (CRPAT)
- Continuous jitter test pattern (CJPAT)
- Square wave pattern (the zero to one ratio can be chosen between 4:4 and 11:11)
- Four random patterns. These patterns, normal (n) and inverted (i), conform to the test patterns proposed in clause 52.9.1 of the IEEE specification.

3 Click the To File button to save the generated segment in a file on disk.

4 Choose a directory and enter a file name.

After the segment has been stored, you can import it into any ParBERT system.

How to Use the 10GbE Post-Processor

The 10GbE post-processor is controlled from the *Post Processing* page of the 10Gb Ethernet Tool.

Prerequisites for Using the Post-Processor

Before the 10GbE post-processor can be used, the following requirements have to be met:

- The stimulating ParBERT system must be set up correctly (see *"Test Setup Procedures" on page 31*). It must be in Run mode and sending a continuous data stream to the DUT.
- The capturing ParBERT system must be set up correctly and ready to run (see *"Test Setup Procedures" on page 31*).
- The 10Gb Ethernet Tool must be connected to the capturing ParBERT system.
- The Generation/Expected page of the 10Gb Ethernet Tool must show precisely the same parameter settings that were used for creating the generated pattern.

  This is mandatory, because the post-processor has no information about the stimulating ParBERT system. It compares the captured data with the data specified on the *Generation/Expected* page.

NOTE If the *Generation/Expected* page shows that you have generated 10GBASE-R encoded data, the post-processor expects a patch for the serial data (if not disabled).

If the *Generation/Expected* page shows that you have generated XAUI encoded data, the post-processor expects the specified disparity.

Controlling the Post-Processor

The *Post Processing* page of the 10Gb Ethernet Tool looks as shown below:

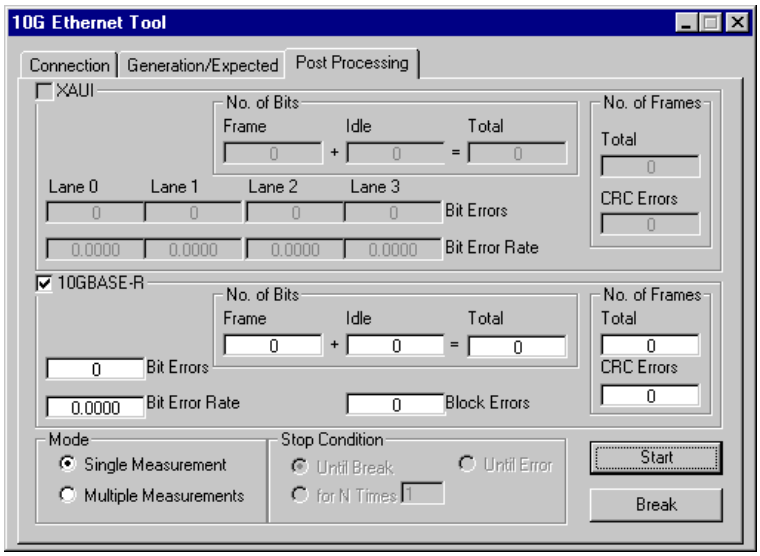


Figure 52 Post Processing Page

The window shown in the figure above appears, if you have connected to a ParBERT system that has been configured for capturing 10GBASE-R data from a one-terminal DUT output port.

If you had connected to a ParBERT system configured for capturing XAUI data from a four-terminal DUT output port, the upper block would be enabled.

To run the test:

1 Choose the *Mode*.

- A *Single Measurement* captures, uploads, and analyzes one sequence block. The display shows the results of that measurement.
- A *Multiple Measurement* is automatically repeated. The display is updated after every repetition and shows the added results.

2 If you have enabled *Multiple Measurements*, choose the *Stop Condition*.

- *Until Break*: This refers to the Break button. The measurement continues until the Break button is clicked.

  Note that Break recognition and final stop may take some time, especially if a large capture memory is used (up to three measurement cycles).

– *for N Times*: The measurement stops after the specified number of repetitions is reached. It stops also if the Break button is clicked.

– *Until Error*: The measurement stops after a bit error has been detected. It stops also if the Break button is clicked.

3 Click Start to execute test.

Interpreting the Test Results

The operation of the post-processor is described in *"Post Processing" on page 16*.

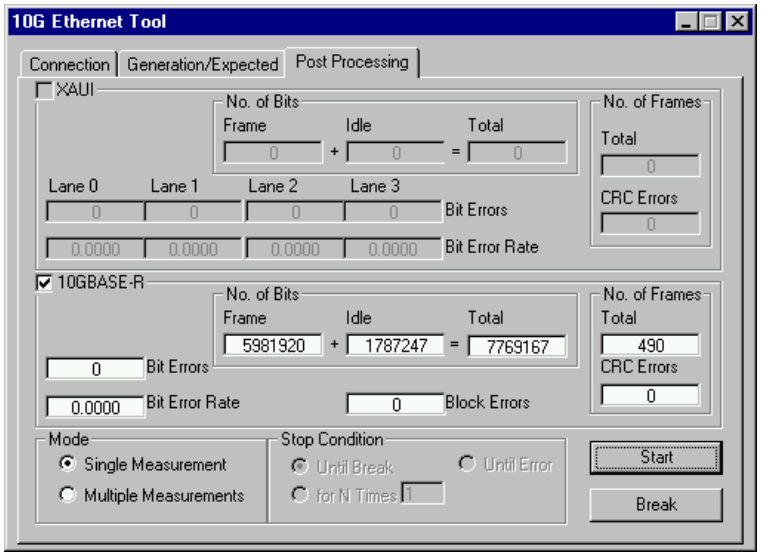


Figure 53 Post Processing Results

The post-processor extracts and checks received frames.

If a PRBS payload is used, patched frames are masked out (ignored).

TIP If you are using a non-PRBS payload, the post-processor will report bit and CRC errors. In this case you may consider disabling the *Patch Scrambler* or the *End With Negative Disparity* option when you generate the stimulating data.

This does not remove all errors but may help you to distinguish between errors caused by patches and transmission errors.

The post-processor identifies Idles and shows the number of bits contained in Idles and in the remainder of the frame(s).

It shows also the number of analyzed frames and the CRC errors found.

It indicates the number of bit errors and the calculated bit error rate.

For 10GBASE-R tests, it decodes 66B encoded blocks and reports the number of block errors. These are blocks with wrong sync bits or block type. Blocks with error are not evaluated.

NOTE The results depend much on the analyzer sampling delay. Cable delays can (and have to) be compensated before starting the test. But the overall phase shift between the generator outputs, the delay caused by the DUT, and the clock phase of the analyzer system is most often undefined.

If unacceptable error rates are displayed, check the analyzer sampling delay.

TIP With ParBERT, you can shift the analyzer sampling point even while a test is running.

When you are setting up tests for an unknown 10GbE device, it is recommended to set the post-processor to *Multiple Measurement*s. While repetitive measurements are performed, you can fine-tune the analyzer sampling delay.

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