6 Tips for Successful Logic Analyzer Probing

Application Note 1501

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Introduction

To design today's increasingly complex digital systems, engineers need sophisticated analysis tools. For system validation tasks, most engineers rely on logic analyzers. As system speeds have skyrocketed and system complexity has multiplied, logic analyzer vendors have boosted instrument performance and functionality to give engineers the capabilities they need. In many cases, the logic analyzer has more than adequate performance for the task at hand, but the physical probe connection from the analyzer to the target system causes a performance bottleneck. If the signals received by the logic analyzer are degraded, the analyzer's powerful triggering and analysis tools are useless.

This application note explores basic probing concepts you need to master a successful logic-analyzer-probing connection. We examine probe form factor choices, probe loading and signal quality concerns, and common problems associated with grounding. Finally, we discuss two common mistakes: probing at the wrong line location and choosing the wrong interconnect.

Take full advantage of your logic analyzer's capabilities and performance by knowing and following probing basics.

Tip 1 Probing form factor

When you decide to use a logic analyzer, you also must choose which type of probing connections you will use. Probing connections fit in two classes: "designed-in" and "after-the-fact." In designed-in logic-analyzer probes, the probing test points are incorporated into the initial design. Connector-based and connectorless probes are members of the designed-in class. With connector-based and connectorless probes, the designer puts down the appropriate pads on the PC board and routes the signals of interest to the pads. The logic-analyzer probe has the appropriate interconnect to mate to these contacts. For a connector-based probe, the probe contains the opposite-sexed connector as the target. For a connectorless probe, the probe has a compression interconnect that will contact the pads on the PC board (Figure 1a).

After-the-fact probe connections are for systems in which testability isn't incorporated into the design. Instead, you make the connection using an individual probe tip that includes various interconnect accessories (solder, grabber, and so forth). The most common type of after-the-fact probe is a "flying-lead" probe (Figure 1b).

Before we discuss the relative advantages and disadvantages of the various probing form factors, let's look at some of the issues you face when you connect a logic-analyzer probe to your system.

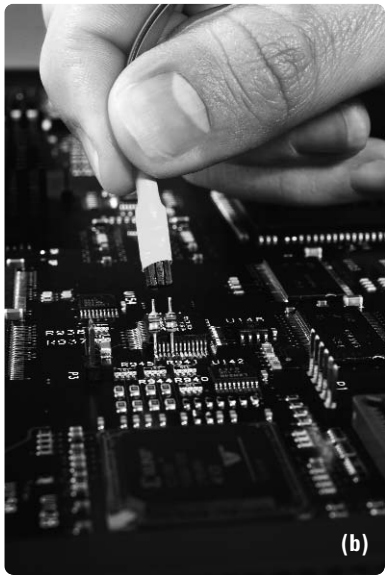


Figure 1. These photos compare a "designed-in" versus an "after-the-fact" probe. The Agilent E5390A shows the connection scheme for the new soft touch connectorless probe (a). In this case the user must put the landing pads in the initial design. The Agilent E5381A shows a possible connection method for a signal that didn't have predefined testability (b).

Tip 2 Probe loading

You want your probe to present the smallest possible electrical load to the system. If the probe alters the system's performance too drastically, the probe doesn't help you validate the system; failures may be caused entirely by the probe. Loading has two major impacts. First, it degrades the signal quality on the target PC board, which may lead to system failures. Second, it can degrade the signal quality of the observed waveform entering the logic analyzer. This could create false negatives in the validation. To avoid these problems, you must understand the probe construction.

The logic analyzer probe has a high input impedance. The probe-tip circuitry consists of a tip resistor on the order of 20 kΩ. At low frequencies, the probe impedance will look like this resistance. As the frequency rises, parasitic capacitance in the probe will start to lower its impedance. The impedance will roll off following a standard RC response. This could present problems for the target system; as the probe impedance begins to approach the system impedance, the voltage divider formed with the probe becomes substantial. A low impedance will absorb the majority of the signal and cause system failure.

Capacitance in the probe is mainly caused by the construction of the interconnect. For example, if there's a significantly large connector between the target signal and the tip resistor in the probe, this connector will add a large capacitance to the probe load. Using a smaller connector will decrease capacitance.

Connectorless probes provide lower electrical loading. As we mentioned earlier, when you use a connectorless probe, you put landing pads on the target system. The logic analyzer probe features a compression interconnect that makes electrical contact to the target. By removing the physical connector from the electrical path, you achieve a very low capacitance (see Table 1).

Figure 2 shows the effect of the equivalent lumped capacitance for a variety of probing form factors on a load terminated transmission line. This waveform shows how the capacitive reflection from the probe arrives at the receiver sometime after the initial wave front.

Probe	Probe Style	Equivalent Capacitance
E5380A	Mictor Connector	3.0 pF
E5378A	Samtec Connector	1.5 pF
E5381A	Flying Lead (solder down)	0.9 pF
E5390A	Soft touch Connectorless	0.7 pF

Table 1.

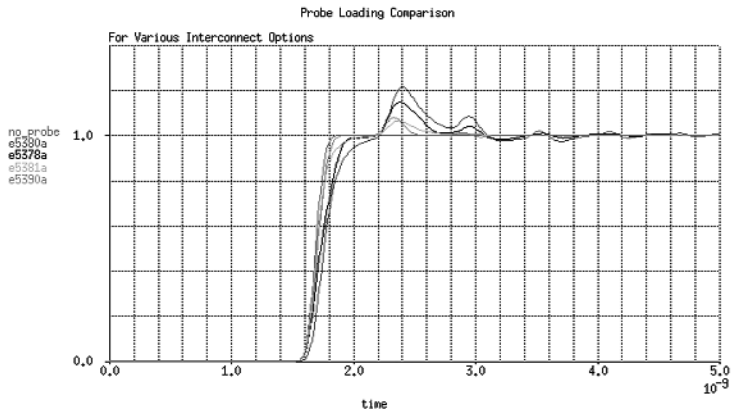


Figure 2. Waveforms are a good way to compare probe loading for various interconnect options. As the connector size is reduced (or removed), the loading decreases. The original rise time in this system is 150 ps.

Tip 3 Signal quality at the probe tip

As we stated earlier, poor signal quality at the probe tip can cause false negatives in the logic analyzer. False negatives are a source of much frustration for validation teams, because they spend their time debugging problems that don't exist. To avoid this problem, you must pay attention to the signal quality at the probe tip.

In addition to watching for simple capacitive loading of the probe, you must pay attention to the probe location. This is particularly important when you probe various termination schemes. For certain termination schemes, the signal observed by the receiver may have sufficient signal quality, while the signal observed at any other point on the line may be unacceptable.

To illustrate this point, consider a series-terminated transmission line. The theory of a series termination is that the induced waveform instantaneously divides between the source termination resistor and the characteristic impedance of the line. The half-amplitude wave travels down the line to the receiver. Upon arriving at the receiver, it experiences a 100% positive reflection, which doubles the half-amplitude signal, thus yielding the original waveform's amplitude. The reflection travels in the reverse direction down the line until it's absorbed into the source termination resistor, thus ending the transient response.

While such a scheme presents a nice waveform to the receiver, the waveform has a stair-step shape at any point on the line. But a stair-stepped waveform simply doesn't suit a logic analyzer because during the period when the waveform remains at half amplitude, the logic analyzer can't detect whether it's a logic "1" or logic "0". Figure 3 shows the waveforms for this situation. Note that the waveform at the receiver has high signal quality, while the observed waveform at the probe tip is unacceptable. As signal speeds increase, the signal quality at the probe tip becomes important to the success of the measurement.

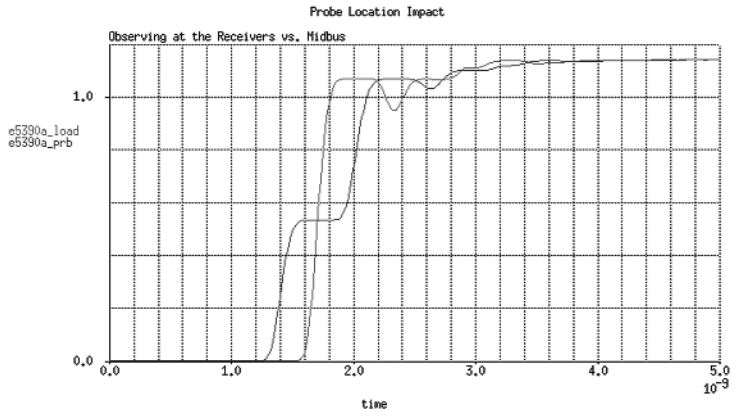


Figure 3. For a series-terminated system, the waveforms are observed at the receiver and the probe tip. Notice the stair-step shape of the wave when observed in the middle of the line. This shows the forward-traveling, half-amplitude wave that's moving toward the receiver. The waveform reaches its final value when the reverse traveling reflection is super-imposed upon the forward-traveling wave.

Tip 4 Grounding issues

You also need to watch out for insufficient grounding when you are using your logic analyzer. The ground signal for the probe supplies the reference that's in relationship to the observed signal. For current to flow and a signal to develop, an electrical signal must always have a return current path. The return path is most always considered to be an ideal conductor with zero resistance. When this isn't the case, voltage will develop across the impedance in the ground-return path. Such voltage will detract from the signal amplitude seen by the logic analyzer. When you ground a device, your goal is to supply a return path (or ground connection) that has the lowest-possible impedance. This step allows the analyzer to observe the original signal amplitude.

A ground lead that is too long is a common cause of problems. The long ground lead will have series resistance that can cause a voltage to develop across it. To prevent this problem, your ground lead should not be significantly longer than your signal lead. Making the leads approximately the same length will match up the parasitic resistance in both the signal and ground path.

Another common probing problem is self-inductance of the ground loop. When a loop is formed by the ground and signal leads, self-inductance will form in the ground path that's proportional to the loop area. This inductance will degrade the system bandwidth due to the inductor's frequency-dependent impedance. At high frequencies, the inductance will prevent charge from traveling through the ground lead, thus reducing bandwidth.

To reduce the problem, try to keep your ground loops as small as possible. Ground loop size is usually predefined when you use a connector-based or connectorless probe. However, with flying-lead probes, there are instances where normal wires will be used to connect the probe to the system. In this case, large ground loops can be formed. To avoid these loops, twist the ground and signal wires together to form a twisted pair. Most flying-lead probes come with connection accessories that assist in solving this problem.

Using an insufficient number of grounds also can cause probing problems. In some probing configurations (such as the flying-lead probe), the user sets the number of grounds. To understand this problem, consider a flying-lead set with 16 signals using only one ground connection. In this situation, the return current for all 16 signals must travel through the single ground connection. The self-inductance of the ground lead is low enough to prevent development of a voltage across it when one or two signals return. But with 16 signals, the current becomes large enough to make the developed voltage noticeable.

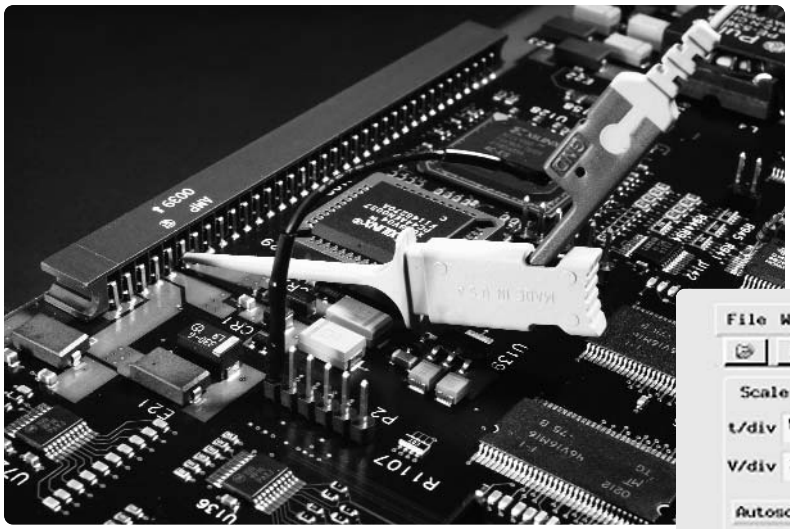
Solving this problem requires increasing the number of grounds. Ideally, there will be one ground for each signal. The number of grounds needed is proportional to frequency. We recommend you don't use more than two signals for one ground. If you experience problems capturing correct data with a logic analyzer, this would be one of the first things to check.

Tip 5 Probing at the wrong location on the line

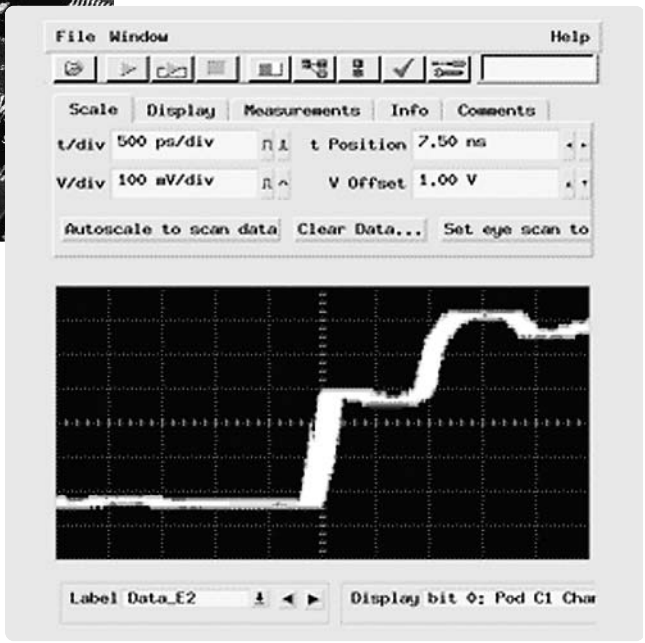
Common Mistakes

With all of the probing options available today, it's sometimes hard deciding on the connection scheme that will ensure success. In some cases, it's even hard to know which solutions are available. The following cases show two common pitfalls you may run into when you use a probing solution that is not suited for the application.

Consider the series-terminated system described earlier. The system is implemented with a driver IC on a backplane card and a receiver located in a BGA package. The user chooses to probe the system at the pin's backplane connector due to its perceived convenience. However, as already demonstrated, probing a series-terminated system at the driver will produce a stair-stepped waveform at the probe tip of the logic analyzer. Figure 4a shows the connection scheme and Figure 4b shows the resultant waveform observed by the logic analyzer.



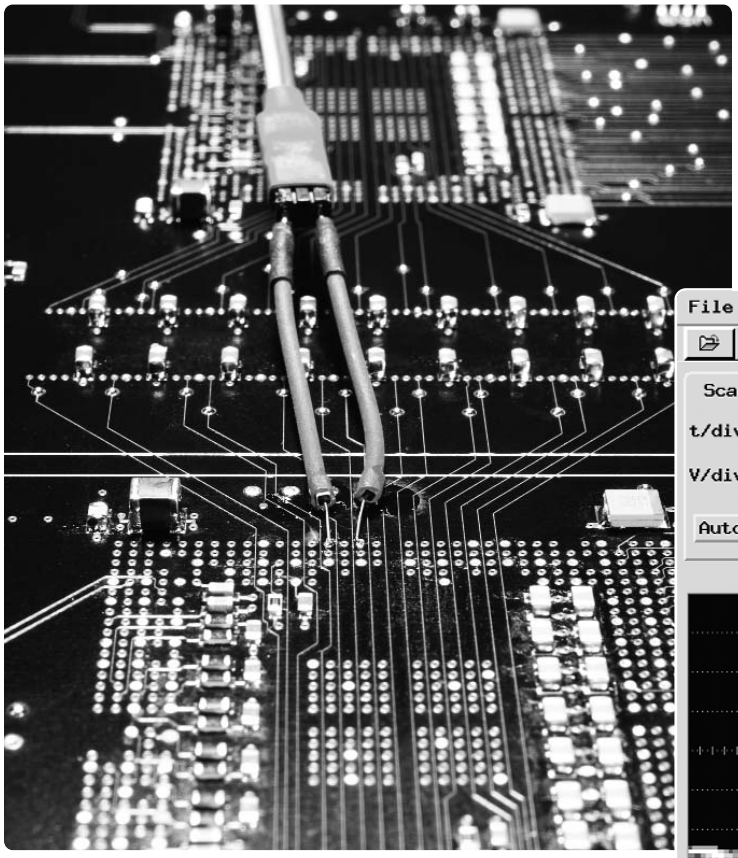
(a)



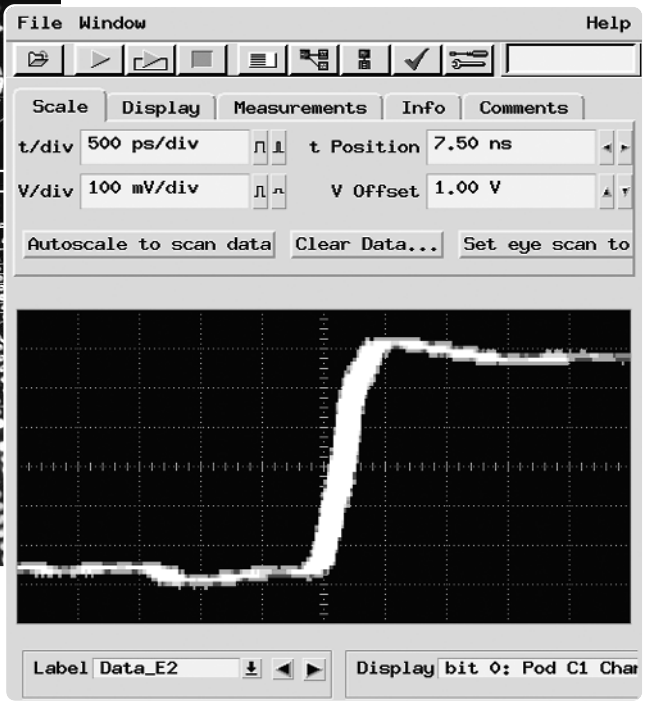
(b)

Figure 4. The probe used here is the Agilent E5382A single-ended flying lead. The connection is completed using a "grabber" accessory that can connect to the leads of a connector (a). The waveform shown is observed by the probe tip. It's displayed using an Agilent-exclusive logic analyzer feature called "eye scan," which allows a logic analyzer to produce the analog version of the signal (b).

This waveform is clearly unacceptable. The solution is to probe directly at the receiver. The closest physical probing point to the BGA package will be the breakout via pads on the bottom side of the PC board. Figure 5a illustrates a new connection scheme that solders the flying lead directly to the breakout vias of the BGA. The resultant signal quality is shown in Figure 5b.



(a)



(b)

Figure 5. Here, the probe is the E5381A differential flying lead. The connection is completed using a "damped wire solder-down" accessory that can solder to extremely small features (a). Again, the observed waveform is displayed using eye scan (b). Notice that the signal quality now is suitable for logic analysis.

Tip 6 Using the wrong interconnect option

Consider a system in which a logic analyzer observes signals that run between two parts on a PC board. The signals run on the outer layer of the PC board and can't withstand more than a 3.5-pF load before system failure. The designer decides to use a Mictor connector-based probe (Agilent E5380A) to observe the signals. Due to the pinout and construction of the connector, signals can't be routed directly through it. This forces the designer to place the connector to the side of the traces and add vias to each signal. The connection to the connector is then accomplished using another PC-board layer that runs traces perpendicular to the original signals. Figure 6 shows the routing diagram for such a connection.

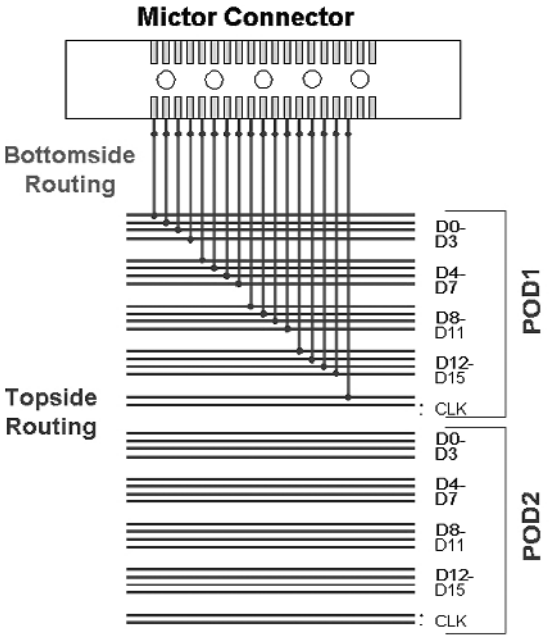


Figure 6. This connection scheme uses a Mictor connector-based probe to observe bus signals. Notice the additional trace length needed to connect to the Mictor. This trace capacitance is added to the connector (3 pF). The net capacitance of this connection is greater than 3.5 pF, resulting in system failure.

Now consider an alternative solution using the Agilent E5390A soft touch connectorless probe. In this case, you can route the signals directly through the landing pads of the probe points (Figure 7). Using this method, no additional trace capacitance is added to the system. The probe's net capacitance is 0.7 pF. By using this type of connection scheme, you can add logic analysis without causing system failure.

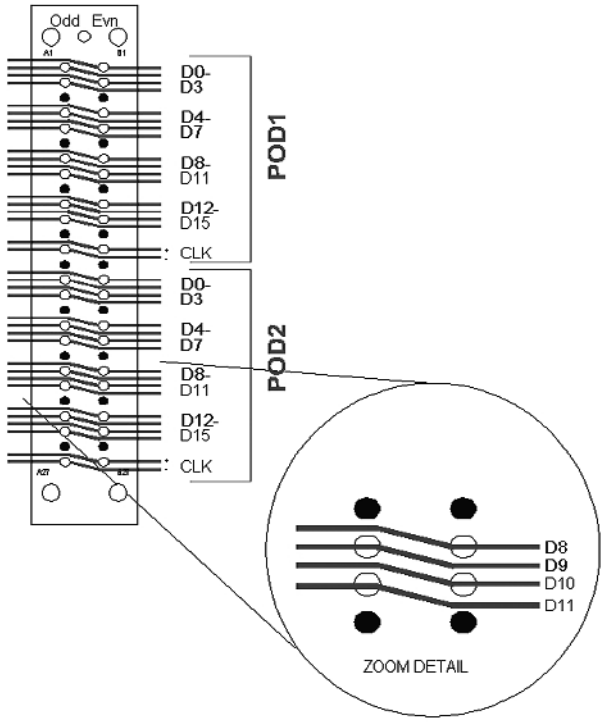


Figure 7. Here, a soft touch connectorless probe observes the bus signals. The reduced probe loading and the ability to route directly through the landing pattern makes for an acceptable logic analyzer connection.

Conclusion

A probe acts as a physical connection between a logic analyzer and your system under test. In some cases, the probe can be a performance bottleneck. If the signals received by your logic analyzer are degraded, then your logic analyzer's powerful triggering and analysis tools are useless. Choosing the right probe form factor and taking steps to minimize probe loading and ensure signal quality at the probe tip can minimize signal degradation. Paying attention to grounding issues can also make a big difference.

This application note is based on an article written by Brock J. LaMeres and Kenneth Johnson of Agilent Technologies. The article, "Taking Logic-Analyzer Probing For Granted Can Spell Trouble," appeared in ED Online in August 2004.

Related Literature

Publication Title	Publication Type	Publication Number
Soft Touch Connectorless Logic Analyzer Probes	Photo Card	5988-8128EN
Probing Solutions for Logic Analyzers	Catalog	5968-4632E
Logic Analyzer Probing Techniques for High-Speed Digital Systems	Application Note 1450	5988-9125EN
FPGA Dynamic Probe	Data Sheet	5989-0423EN
16900 Series Logic Analysis Systems	Brochure	5989-0420EN
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