N4906B Serial BERT

Data Sheet

Version 3.0

New: Enhanced measurement suite

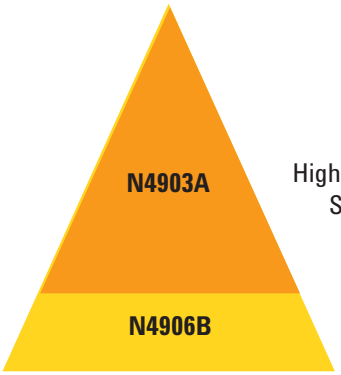
Agilent Technologies

Agilent Technologies N4900 Series

The Agilent N4900 serial BERT series provides industry-leading parametric test capabilities for design verification, characterization and manufacturing of semiconductor and communication devices up to 12.5 Gb/s.

The N4906B serial BERT addresses the need for cost-effective bit error ratio (BER) testing, which is especially important in manufacturing environments but also for budget-sensitive telecom device testing.

The J-BERT N4903A high-performance serial BERT is the right choice for R&D applications and characterization needs. It is equipped with calibrated and built-in jitter injection for quick and accurate receiver characterization and compliance testing.



Key benefits of the serial BERT platform:

- Excellent precision and sensitivity
- User-selectable choice of feature set and frequency classes to tailor to dedicated test needs
- Pass / fail testing
- State-of-the-art user interface with color touch screen
- LAN, USB and GPIB interfaces

The serial BERT N4906B offers cost-effective manufacturing and telecom device testing:

- N4906B option 003: 150 Mb/s to 3.6 Gb/s; differential analysis
- N4906B option 012: 9.5 Gb/s to 12.5 Gb/s
- N4906B option 101: differential analysis, fast eye mask and enhanced measurement suite
- N4906B option 102: extension to full frequency range 150 Mb/s - 12.5 Gb/s & clock data recovery

The J-BERT N903A high-performance serial BERT is the ideal choice for characterization and R&D

- 7 and 12.5 Gb/s data rates max
- Jitter injection and anlysis options

Serial BERT selection guide

Device under test	Typical requirements	Recommended Agilent BERT	
		For R&D and characterization	For manufacturing
Optical transceivers, i.e.: SONET, SDH, 10GbE, XFP Fibre Channel 8 G /10 G	PRBS Signal precision Eye masks Datarates 10 Gb/s ± margin	N4903A	N4906B opt. 012
High-speed serial computer buses, i.e. PCI Express 1.x, 2.0 SATA II and III, SAS Infiniband-DDR, Fibre Channel 2 G/4 G, etc	Test pattern sequences CDR Differential inputs Datarates < 6 Gb/s	N4903A*	N4906B opt. 012/101/102
0.6 - 2.5 Gb/s transceiver, i.e. E-PON / G-PON OLTs, Gigabit Ethernet	Fast bit synchronisation Datarates < 3.5 Gb/s Burst mode Recirculation loop testing	N4906B opt. 003*	N5980A

* Or ParBERT for multiple channels

The N4906B Serial BERT

General

The N4906B serial BERT is a general-purpose bit error ratio tester designed for testing high-speed digital communication components and systems. It is ideal for cost-effective manufacturing and telecom device testing.
It offers a 3.6 Gb/s or 12.5 Gb/s pattern generator and error detector with excellent price/performance ratio.
The 12.5 Gb/s error detector can be configured with CDR (option 102) to test clockless interfaces and with true differential inputs to test LVDS and other differential interfaces.
The 3.6 Gb/s error detector is equipped with true differential inputs.
The compact size of the N4906B saves rack space and LAN, USB and GPIB interfaces allow smooth integration into automated test environments.
For bench users the N4906B serial BERT offers an intuitive user interface with a state-of-the-art Windows® XP based color touch-screen.

Available configurations for N4906B up to 3.6 Gb/s:

- N4906B option 003: 150 Mb/s to 3.6 Gb/s; differential analysis

Available configurations for N4906B up to 12.5 Gb/s:

- N4906B option 012: 9.5 Gb/ to 12.5 Gb/s
- N4906B option 101: differential analysis, fast eye mask and enhanced measurement suite
- N4906B option 102: extension to full frequency range 150 Mb/s to 12.5 Gb/s & clock data recovery

Key values & benefits

- 150 Mb/s to 3.6 Gb/s (option 003) or
- 9.5 Gb/s to 12.5 Gb/s (option 012) pattern generator and error detector (option 102: 150 Mb/s - 12.5 Gb/s)
- Fast eye mask measurement for pass/fail testing (option 101)
- < 50 mV_{pp} input sensitivity
- Fast bit synchronization on bursted pattern
- Intuitive user interface, state-of-the-art Windows XP color touch screen
- Small form factor to save bench and rack space
- Compatibility with existing remote commands, e.g. Agilent 71612, 86130A series and N4900 series

Key characteristics:

- Excellent price/performance ratio
- Data rate up to 3.6 Gb/s or 12.5 Gb/s
- <50 mV_{pp} input sensitivity
- Enhanced measurement suite (option 101)
- Small form factor
- LAN, GPIB and USB for remote control
- Color touch screen, Windows XP

Pattern generator

- Pattern generation for PRBS or memory based patterns
- Pre-defined for sonet/SDH frames and patterns for 10 GbE
- Flexible levels addressing a broad range of technologies, e.g. ECL, PECL (3.3 V), LVDS, CML
- < 25 ps (10%-90%) transition times for option 012
- < 50 ps (10%-90%) transition times for option 003 using N4915A-001 transition time converter

Error detector

- BER measurements
- Automatic threshold alignment
- Automatic sampling point alignment
- Automatic data polarity alignment
- G. 821 measurement

Measurement features

- Bit error ratio (BER)
- Fast eye mask measurement including pass/fail (option 101)
- BERT scan (option 101)
- Fast total jitter (option 101)
- Spectral jitter decomposition (option 101)
- Eye contour (option 101)
- Output level (option 101)
- Error location capture (option 101)

User Interface/Remote Control

The time needed to set up a measurement is minimized based on intuitive and easy-to-learn interfaces.

By utilizing network capabilities, the N4906B serial BERT is remote controllable via LAN, GPIB and USB interface. Test executives can control the system by using Agilent TestExec or Vee, Microsoft® Excel or Visual Basic and National Instruments' LabVIEW.

The serial BERT N4906B user interface is easily fitted to manufacturing testing applications. In addition, the fast eye mask measurement (option 101) guarantees an immediate return on investment.

The user interface provides the following functions:

- Pattern generator setup
- Error analyzer/ dectector setup
- Pattern editor
- BER result, G. 821 result
- Enhanced measurement suite (option 101)

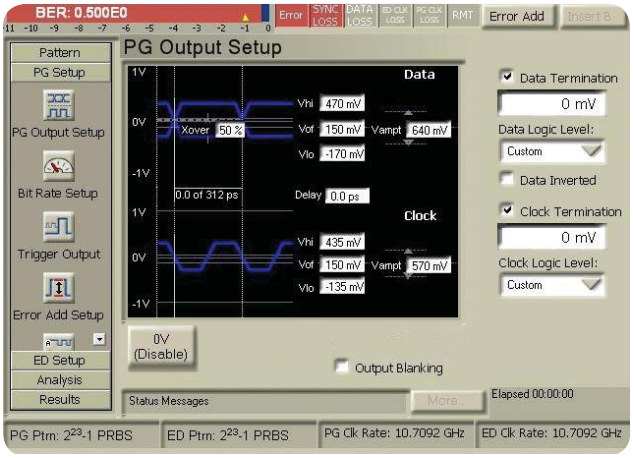


Figure 1: Pattern generator setup

The pattern generator screen allows simple access to timing & level parameters, as seen above.

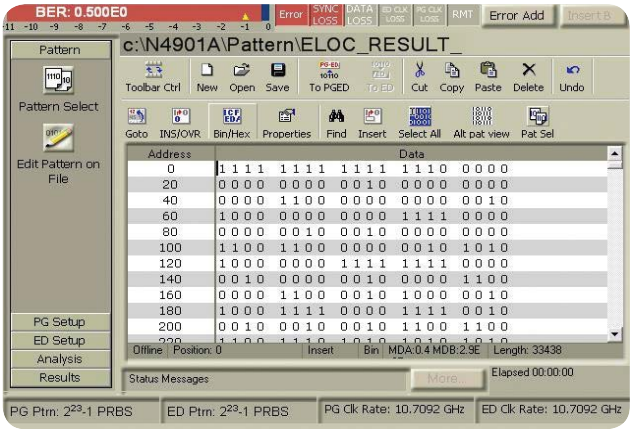


Figure 2: Pattern editor

The pattern editor allows to enter user-specific data or select pre-defined test or PRBS patterns.

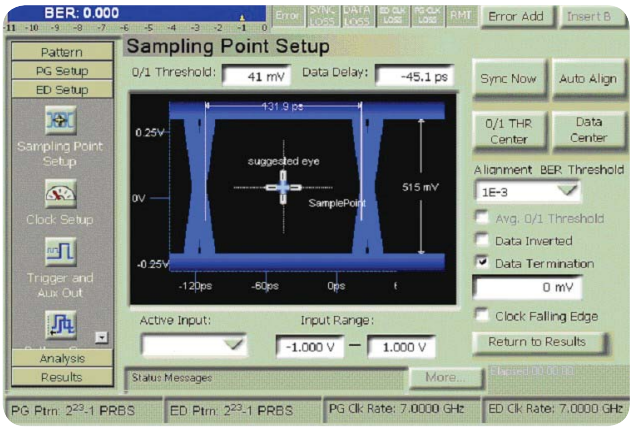


Figure 3: Error detector setup

The sampling point setup allows simple access to sampling point position dependent on timing and voltage threshold.

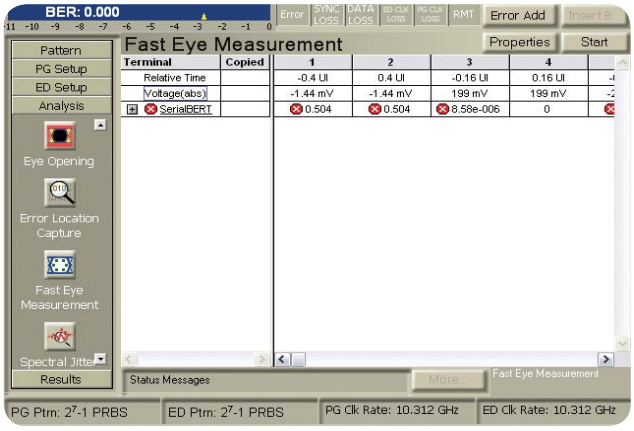


Figure 4: Fast eye mask measurement

The fast eye mask measurement screen shows the results for up to 32 pre-defined test points. This measurement is ideal for fast pass/fail testing in manufacturing. (option 101 only).

Enhanced Measurement Suite
(option 101)

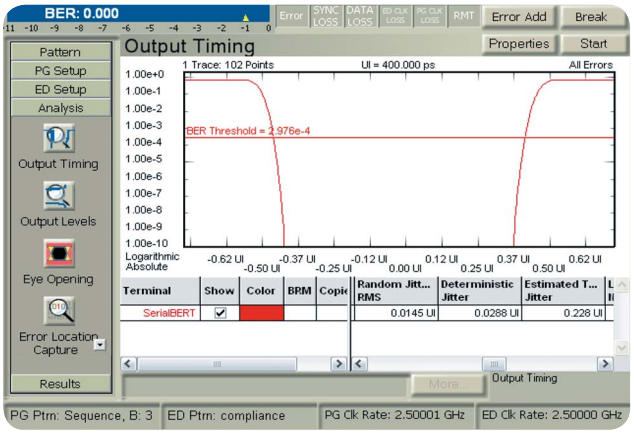


Figure 5: BERT scan including RJ/DJ speparation and total jitter

The BERT scan is used to measure the timing and jitter behavior of the output signal of a device under test (DUT). It measures the bit error ratio (BER) versus the sampling point delay. The result can be displayed as a so-called"bathtub" curve or as a histogram. A table shows the measured total jitter and the separation into random jitter and deterministic jitter components. The measurement method is equivalent to the IEEE 802.3ae method.

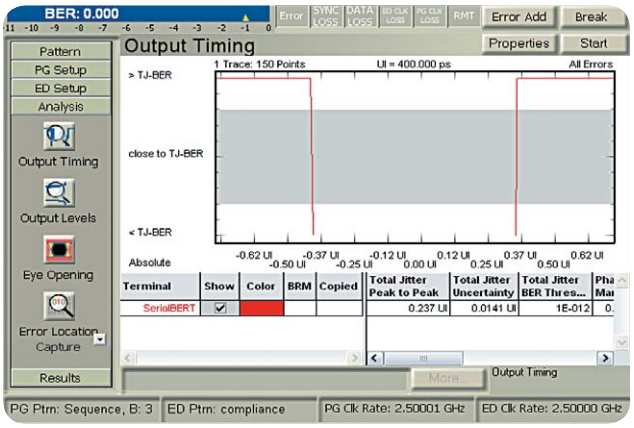


Figure 6: Fast total jitter measurement for quick and accurate total jitter measurements

The fast total jitter measurement method provides fast and feasible total jitter measurements, around 40 times faster than a common BERT scan but with comparable confidence level. Instead of comparing bits until the BER reaches a defined number of bits or a defined number of errors, it only compares bits until it can decide with a 95% confidence level whether the actual BER is above or below the desired BER.

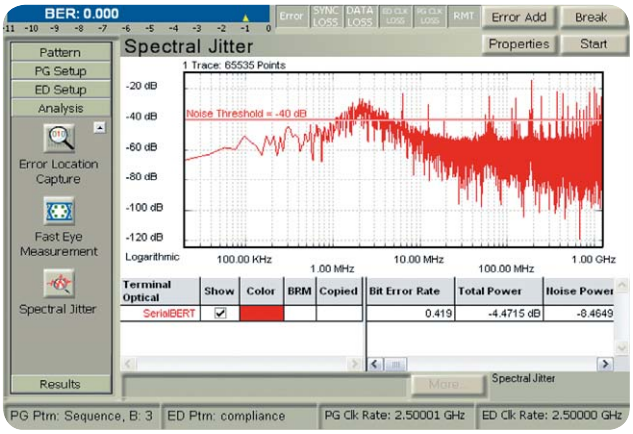


Figure 7: Spectral jitter decomposition for debugging the jitter sources in a design

The spectral jitter measurement provides a method for investigating the spectrum of the jitter in terms of its power distribution over frequency. Deterministic jitter can be caused by repetitive data patterns. It can also be caused by internal or external periodic effects. The spectral jitter measurement detects even small periodic components that may be hidden in a high level of random noise. It shows the frequencies of such components and measures their contribution to the total jitter. This helps to identify jitter sources and to reduce or eliminate their influence.

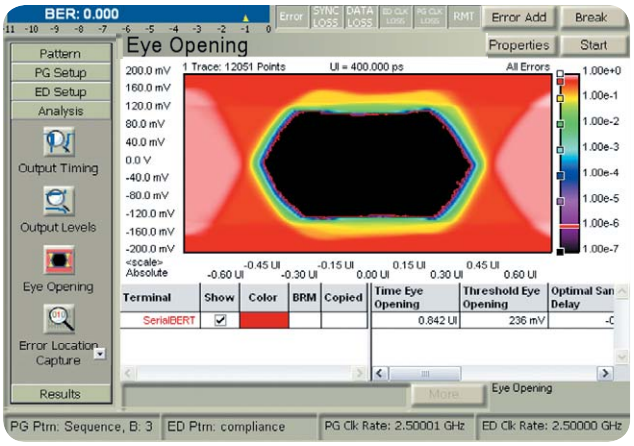


Figure 8: Eye contour with colors indicating the BER level

The eye contour measurement generates a three-dimensional bit error rate (BER) diagram as a function of the sample delay and the sample threshold. With this measurement, the complete eye of the DUT output signal is measured. The results comprise the voltage and timing of the eye opening and the BER level. Different result views are available: eye contour, pseudo colors and equal BER plots.

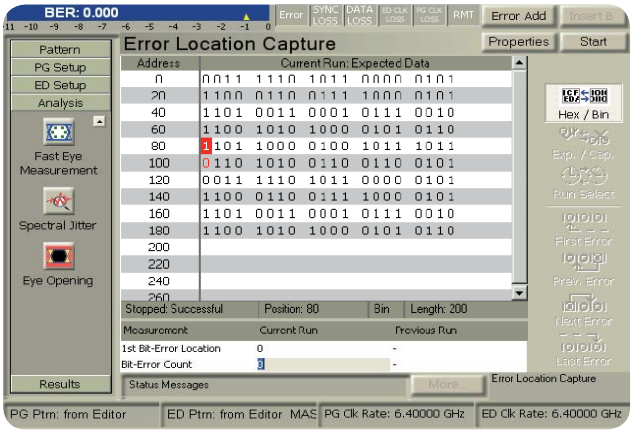


Figure 9: Error location capture indicates the position of errored bits

The error location capture measurement allows capturing the actual position of errored bits in a memory-based pattern. The instrument searches for the first bit errored in the incoming bit stream and marks it in the pattern. The address of the errored bits can be displayed after the error is located. This feature can be used to find rare or random errors. A DUT could have problems handling long series of zeroes. Error location capture can be used to locate the bit errors in such cases.

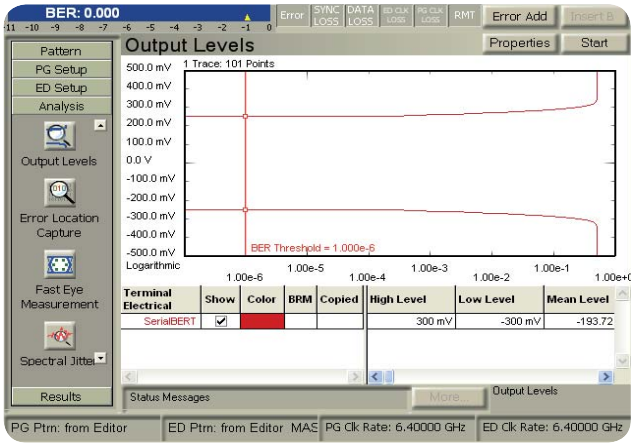


Figure 10: Output level measurement

The output level measurement allows to characterize the behavior of the output levels of a device under test (DUT). The sampling delay is fixed. The error detector's decision threshold is automatically swept within a user-defined range. A direct result is the determination of the optimum decision threshold level for receiving data from the DUT with maximum confidence. Three result views are available: Q-factor, BER vs. threshold, and dB histogram vs. threshold.

Pattern Generator

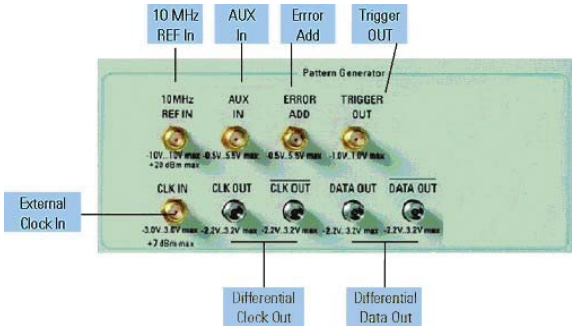


Figure 11: Front view of pattern generator

The pattern generator generates hardware-based PRBS up to 2^{31}-1 and user defined patterns. It provides a memory depth of 32 Mbit. Pattern format is compatible within the N4900 series. Therefore user defined patterns can be transferred across the N4900 serial BERT series.

Features:

- Differential outputs
- Adjustable output
- Amplitude and levels
- Clock/data relative delay adjustment
- Adjustable crossing point
- Output blanking (burst mode)
- Error insertion
- Trigger output
- Alternating pattern

Waveform example for differential data output

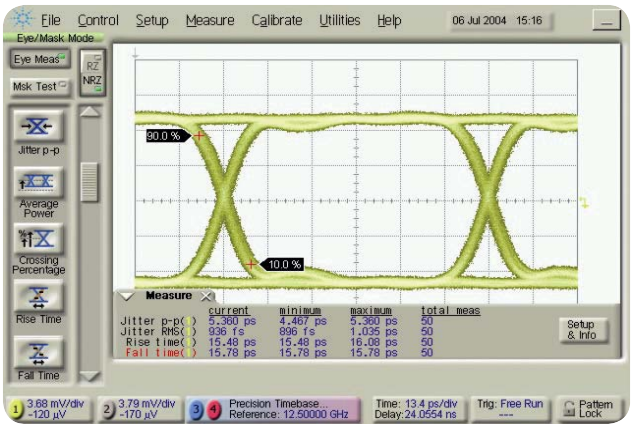


Figure 12: Output signal at 50% crossing point and 12.5 Gb/s (option 012)

Data Output

Table 1: Parameters for N4906B serial BERT generator. All timing parameters are measured at ECL levels.

Range of operation	
Option 003	150 Mb/s[1] to 3.6 Gb/s
Option 012	9.5 Gb/s to 12.5 Gb/s
Option 102[2]	150 Mb/s[3] to 12.5 Gb/s
Format	NRZ, normal or inverted
Amplitude/resolution	0.1 V to 1.8 V/ 5 mV steps
Output voltage window	-2.0 V to +3.0 V
Predefined levels	ECL, PECL (3.3 V), LVDS, CML
Data interface[4]	Differential or single-ended DC coupled, 50 Ω
Transition times	
20% to 80%	< 20 ps typ.
10% to 90%	< 25 ps[5]
With N4915A-001 transition time converter	< 50 ps typ.[6]
Jitter	9 ps pp typ.
Clock/data delay range	±0.75 ns
Resolution	100 fs
External termination voltage[7]	-2 V to +3 V
Crossing point	20%.....80% typ. adjustable
Single error inject	Adds single errors on demand
Fixed error inject	Fixed error ratios of 1 error in 10^n bits, n = 3, 4, 5, 6, 7, 8, 9
Connector	2.4 mm female 2.4 mm to 3.5 mm adapters are included

1) 150 MHz to 3.6 GHz external clock, 620 Mb/s to 3.6 Gb/s internal clock.
2) Only in combination with option 012.
3) 150 MHz to 12.5 GHz external clock, 620 Mb/s to 12.5 Gb/s internal clock.
4) Unused outputs must be terminated with 50 Ω to GND.
5) Only option 012 at 10 Gb/s.
6) Recommended for option 003.
7) For positive termination voltage or termination to GND, external termination voltage must be less than 3 V below VOH. For negative termination voltage, external termination voltage must be less than 2 V below VOH. External termination voltage must be less than 3 V above VOL.

Generator Clock

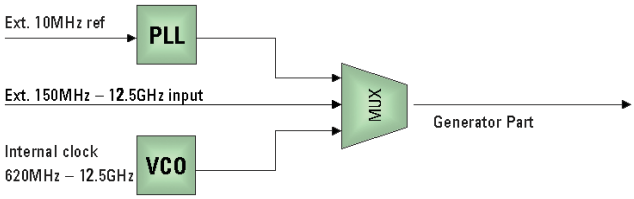


Figure 13: Block diagram for the clock section

The clock of the N4906B provides three different operation modes:

- Internal clock
- External clock signal to CLK IN.
- 10 MHz reference signal to 10 MHz REF IN: in this mode the internal clock is derived from the applied 10 MHz reference signal.

Clock frequency range

Table 2: Clock frequency range

Frequency range	
Option 003	150 MHz[1] to 3.6 GHz
Option 012	9.5 GHz to 12.5 GHz
Option 102[2]	150 MHz[3] to 12.5 GHz

Clock output

Table 3: Parameters for N4906B serial BERT clock output. All timing parameters are measured at ECL levels.

Impedance	50 Ω typ.
Amplitude/resolution	0.1 V_{pp} to 1.8 V_{pp}/ 5 mV steps
Output voltage window	-2.00 to +2.8 V
Short circuit current	72 mA max.
Clock interface[4]	Differential or single-ended, DC coupled, 50 W
Transition times	
20% to 80%	< 20 ps typ.
10% to 90%	< 25 ps[5]
with N4915A-001 transition time converter	< 50 ps typ.[8]
Addressable technologies	LVDS, CML, PECL, ECL (terminated to 1.3 V / 0 V / -2 V) low voltage CMOS
External termination voltage[6]	-2 V to +3 V
Jitter	1 ps rms typ.
SSB phase noise[7]	< -75 dBc with internal clock source
Connector	2.4 mm female 2.4 mm to 3.5 mm adaptors included

Clock input and 10 MHz reference input

Table 4: Specifications for clock input and 10 MHz reference input

Interface	AC coupled, 50 Ω nominal
Amplitude	200 mV to 2 V
Connector	SMA female

Trigger output

It operates in two modes: pattern trigger and divided clock trigger. This provides an electrical trigger synchronous with the pattern for use with an oscilloscope or other test equipment. Typically there is a delay of 32 ns between trigger and data output when using datarates ≥ 620 Mb/s.

Pattern trigger mode

For PRBS patterns the pulse is synchronized with a user specified trigger pattern. The repetition rate is 1 pulse for every 4th pattern.
For memory-based patterns the trigger signal is synchronized to a certain bit position in the pattern.

Divided clock mode

In divided clock mode the trigger is a square wave at the clock rate divided by 2, 4, 8, 10, 16, 20, 32, 40, 64, 128.

Table 5: Specification for trigger output

Pulse width	Square wave
Levels	High: +0.5 V; Low -0.5 V typ.
Transition times	35 ps typ.
Interface	DC coupled, 50 Ω nominal
Connector	SMA female

1) 150 MHz to 3.6 GHz external clock, 620 MHz to 3.6 GHz internal clock.
2) Only in combination with option 012.
3) 150 MHz to 12.5 GHz external clock, 620 Mb/s to 12.5 Gb/s internal clock.
4) Unused outputs must be terminated with 50 Ω to GND.
5) Only option 012 at 10 Gb/s.
6) For positive termination voltage or termination to GND, external termination voltage must be less than 3 V below VOH. For negative termination volt-age, external termination voltage must be less than 2 V below VOH. External termination voltage must be less than 3 V above VOL.
7) 10 GHz @ 10 kHz offset, 1Hz bandwidth.
8) Recommended for option 003.

Auxiliary Input

When the alternate pattern mode is activated the memory will be split into two parts. The user can define a pattern for each part. Depending on the operational mode of the auxiliary input the user can switch in real-time the active pattern by applying a pulse (mode 1), or by a logical state (mode 2), to the auxiliary input.
If the alternate pattern mode is not activated the user can suppress the data on the data output by applying a logical high to the auxiliary input (mode 3).

Mode 1: one-shot edge sensitive alternating pattern

A rising edge on the auxiliary input inserts a single version of pattern B into repetitions of pattern A. The applied pulse must be 512 bit long.

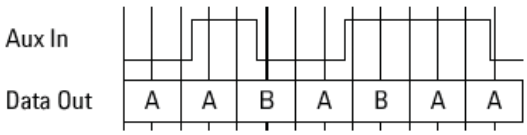


Figure 14: Edge sensitive

Mode 2: level sensitive alternate pattern (continuous)

The logic state of the signal at the auxiliary input determines which pattern is output. An active (TTL high) signal will output pattern B.

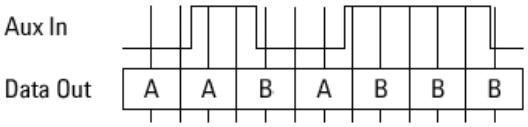


Figure 15: Level sensitive

Mode 3: output blanking

If alternate pattern mode is not selected, an active (TTL high) signal at the auxiliary input port forces (gates) the data to a logic zero at the next 32-bit boundary in the pattern. The minimum length of the signal is 100 ns.

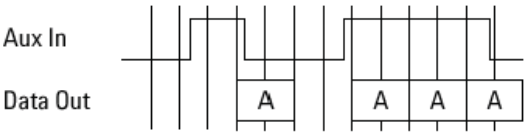


Figure 16: Output blanking

Table 6: specifications for auxiliary input

Interface	DC coupled, 50 Ω nominal
Levels	TTL compatible
Connector	SMA female

External error inject input

The external “error inject input” adds a single error to the data output for each rising edge at the input.

Table 7: Specifications for error inject input

Interface	DC coupled, 50 Ω nominal
Levels	TTL compatible
Connector	SMA female

Patterns

Patterns are used as stimulus data on the generator as well as expected data on the error detector. These patterns can be setup commonly for the generator and error detector or independently.

User-programmable test patterns

User defined patterns are available with variable length from 1 bit to 33,554,432 bits (32 Mbit).

Alternate test pattern

Switch between two equal length user programmable patterns, each up to 16,777,216 bits (16 Mbit). Switching is possible by using a front panel key, GPIB or the auxiliary input port. Changeover is synchronous with the end of the pattern. The length of the alternating patterns should be a multiple of 512 bits. Two methods of controlling pattern changeover are available: one-shot and alternate.

PRBS (HW generated)

- 2^{31} - 1 Polynomial: $x^{31} + x^{28} + 1 = 0$ (inverted)
- 2^{23} - 1 Polynomial: $x^{23} + x^{18} + 1 = 0$ (inverted) (ITU-T O.151)
- 2^{15} - 1 Polynomial: $x^{15} + x^{14} + 1 = 0$ (inverted) (ITU-T O.151)
- 2^{11} - 1 Polynomial: $x^{11} + x^{9} + 1 = 0$ (inverted) (ITU-T O.152)
- 2^{10} - 1 Polynomial: $x^{10} + x^{7} + 1 = 0$ (inverted)
- 2^{7} - 1 Polynomial: $x^{7} + x^{6} + 1 = 0$ (inverted) (ITU-T V.29)

Zero substitution

Zeros can be substituted for data to extend the longest run of zeros in the patterns below. The longest run can be extended to the pattern length -1. The bit following the substituted zeros is set to 1.

Variable mark density

The ratio of ones to total bits in the patterns below can be set to 1/8, 1/4, 1/2, 3/4, or 7/8.

Available test patterns for zero and variables:
- 8388608 bits based on 2^{23} PRBS
- 32768 bits based on 2^{15} PRBS
- 8192 bits based on 2^{13} PRBS
- 2048 bits based on 2^{11} PRBS
- 1024 bits based on 2^{10} PRBS
- 128 bits based on 2^{7} PRBS

Error Detector

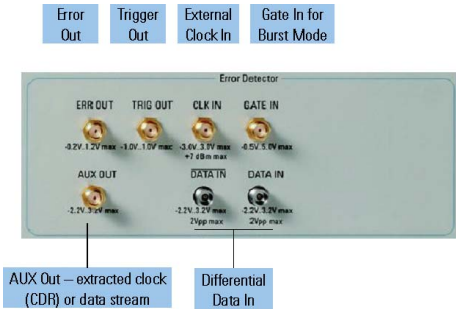


Figure 17: Front view error detector

The error detector compares each individual bit against the expected data (deterministic data or data pattern) in real time. The incoming bits must be periodic.

Features:
- Data input: normal / inverted
- Differential data inputs (option 101 or 103)
- Variable clock / data sampling delay
- Clock / data auto-alignment
- 0/1 decision threshold auto-alignment
- Clock data recovery (CDR) for selected
- Frequency ranges or ext. clock (option 102)

Data input

Table 8: Parameters for N4906B error detector

Range of operation	
Option 003	150 Mb/s to 3.6 Gb/s
Option 012	9.5 Gb/s to 12.5 Gb/s
Option 102[1)]	150 Mb/s to 12.5 Gb/s
Inputs [3)7)] normal/inverted	Single-ended: 50 Ω, typ. Differential[4)]: 100 Ω typ.
Format	NRZ
Max input amplitude	2.0 V
Termination voltage [3)]	-2 V to +3V or off (true differential mode[4)])
Sensitivity[5)]	< 50 mV_{pp}
Decision threshold range	-2 V to +3 V in 0.1 mV steps
Max levels	-2.2 V to +3.2 V
Phase margin[6)]	1 UI - 12 ps typ.
Clock/data sampling delay	±0.75 ns in 100 fs steps
Connector	2.4 mm female 2.4 mm to 3.5 mm adapters included

Clock input

The error detector needs either an external clock signal or a recovered clock signal (option 102 CDR).

Table 9: Specification clock input

Frequency range	
Option 003	150 MHz to 12.5 GHz
Option 012	9.5 GHz to 12.5 GHz
Option 102[1)]	150 MHz to 12.5 GHz
Interface	AC coupled, 50 Ω nominal
Amplitude	100 mV to 1.2 V
Sampling	Positive or negative clock edge
Connector	SMA female
CDR output jitter[2)]	0.01 UI rms typ.
Clock data recovery[2)] (CDR)	**Loop bandwidth (typ.)**
9.9 Gb/s to 10.9 Gb/s	8 MHz
4.23 Gb/s to 6.40 Gb/s	4 MHz
2.115 Gb/s to 3.20 Gb/s	2 MHz
1.058 Gb/s to 1.6 Gb/s	1 MHz

The CDR works with specified PRBS patterns up to 2^{31}-1. The CDR expects a DC balanced pattern. The CDR expects a transition density of one transition for every second bit.

Trigger out

Pattern trigger mode

This provides an electrical trigger synchronous with the selected error detector reference pattern. In pattern mode the pulse is synchronized to repetitions of the output pattern. For PRBS patterns the repetition rate is 1 pulse for every 4th pattern repetition

Divided clock mode

In divided clock mode the trigger signal is a square wave.

Table 10: Specifications for trigger output

Clock divider	4, 8, 16 up to 11 Gb/s 32, 40, 64, 128 up to 12.5 Gb/s
Interface	DC coupled, 50 Ω nominal
Levels	High: + 0.5 V; Low: - 0.5 V
Minimum pulse width	Pattern length x clock period/2 e.g. 10 Gb/s with 1000 bits = 50 ns
Connector	SMA female

1) Only in combination with option 012.
2) Only with option 102.
3) User has to define a 2 V operating voltage window, which is in the range between -2.0 V to +3.0 V. Data signals, termination voltage and decision threshold have to be within this voltage window.
4) If option 101 or option 003 is installed.
5) @ 10 Gb/s, BER 10-12, PRBS 2^{31} -1.
6) Based on internal clock.
7) Unused inputs should be terminated with 50 Ω to GND.

Errors Output

This provides an electrical signal to indicate received errors. The output is the logical 'OR' of errors in a 128-bit segment of the data.

Table 11: Specifications for error output

Interface format	RZ, active high
Interface	DC coupled, 50 Ω nominal
Levels	High: 1 V nominal; Low: 0 V nominal
Pulse width	128 clock periods
Connector	SMA female

Gating input

If a logical high is applied to the gate input the analyzer will ignore incoming bits during a BER measurement. The ignored bit sequence is a multiple of 512 bits.

Table 12: Specification for gating input

Interface levels	DC coupled, 50 Ω nominal
Levels	TTL compatible
Connector	SMA female
Pulse width	256 clock periods

For measuring data in bursts of bits, rather than one continuous stream of bits, a special operating mode is used. This is the burst sync mode. In this case, the signal at the gating input controls the timing of synchronization and error counting for each burst. This is an important feature for recirculation loop measurements.

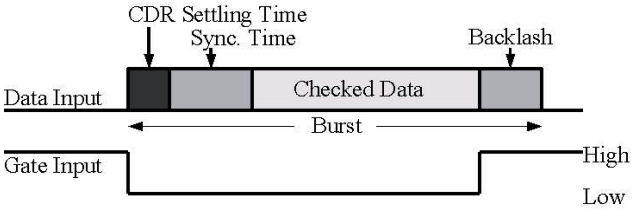


Figure 18: Burst mode

If the clock data recovery (CDR) is used to recover the clock out of the burst data, the CDR needs the first bits of the burst data to settle. The number of bits the systems needs to synchronize itself during a burst depends on wether the pattern consists of hardware based PRBS data or memory based data. To run properly in burst mode the system requires a backlash of data after the gate input returned to high. During each burst the gate input has to remain passive for a certain time.

Table 13: Burst

	Non CDR mode	CDR mode
CDR setting time	-	2 µs
Synchronisation time		
Hardware based PRBS	1536 bits	
Memory based pattern	15 kbit[1)]	
Backlash	1536 bits	1.5 µs
Gate passive time	2560 bits	2560 bits or 1.5 µs[2)]

1) Depends on when and how often the unique word for synchronistation occurs.
2) Whichever takes longer.

AUX output

This output can be used to provide either clock or data signals:
CLOCK: clock signals from the input or recovered clock signals in CDR mode (option 102)
DATA: data after being compared with the threshold.

Table 14: Specifications of AUX output

Interface	AC coupled, 50 Ω nominal
Amplitude	600 mV nominal
Connector	SMA female

Automatic Alignment

The serial BERT N4906B is able to align the sampling point's voltage threshold and time offset. It is possible to automatically align the threshold and offset together or each separately.

Automatic center (auto align)

The error detector sets the 0/1 threshold midway between the top and bottom of the eye, where the bit error ratio is equal to a selectable threshold. The eye height is calculated and displayed. It is limited to a 2 V window selected by the user. Also it recognizes a pattern inversion.

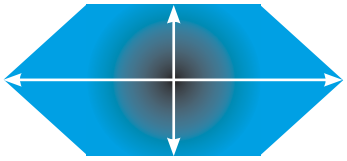


Figure 19: Automatic center

Automatic clock to data alignment (data center)

An important feature of the serial BERT N4906B error detector is the ability to automatically align the clock and data inputs. The sampling point will be positioned in the middle of the eye (time axis).

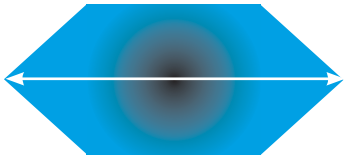


Figure 20: Clock-data sampling point search

Automatic threshold (0/1 threshold center)

The error detector centers the 0/1 threshold level automatically. If singled ended measurements are done, the error detector is able to continuously track the mean DC level of the input signal and adjust the threshold accordingly. The adjustment interval is 100 ms. The tracking is limited to a 2 V window selected by the user.

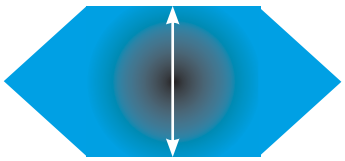


Figure 21: Automatic 0/1 threshold center search

Mainframe Characteristics

Table 15: General mainframe characteristics

Operating temperature	5 °C to 40 °C
Storage temperature	-40 °C to +70 °C
Humidity	5 - 40 °C, 95% rel.humidity
Power requirements 47 - 63 Hz, 350 VA	100 - 240 VA, ± 10%,
Physical dimensions	Width: 424.5 mm Height: 221.5 mm Depth: 580.0 mm
Weight (net)	24.5 kg
Weight (shipping)	36.0 kg max

Display
8” color LCD touchscreen

Data entry
Color touch-screen display, numeric keypad with up/down arrows, dial-knob control or external keyboard and mouse via USB interface

Hard disk
For local storage of user patterns and data. External disk via USB interface also available.

Removable storage
Floppy disk drive 1.44 MB

Interfaces
GPIB (IEEE 488), LAN, parallel printer port, VGA output, 4 x USB 2.0, 1 x USB 1.1 ports

Online help
For comprehensive software support

I/O libraries
I/O libraries to control the N4906B via LAN, USB and GPIB are included.

Specification assumptions
The specifications in this brochure describe the instrument’s warranted performance. Non-warranted values are stated as typical.
All specifications are valid in a range from 5°C to 40°C ambient temperature after a 30 minute warm-up phase. If not otherwise stated, all inputs and outputs need to be terminated with 50 Ohms to ground. All specifications, if not otherwise stated, are valid using the recommended N4910A cable set (24 mm, 24” matched pair).

Order Instructions

N4906B-003	Serial BERT 3.6 Gb/s; pattern generator & error detector with differential analysis; 4 x 50 Ω terminations; 6x 2.4 mm to 3.5 mm APC adapter; no cables included
N4906B-012	Serial BERT 12.5 Gb/s; pattern generator & error detector; 4 x 50 Ω terminations; 6x 2.4 mm to 3.5 mm APC adapter; no cables included
N4906B-101	Differential analysis, fast eye mask and enhanced measurement suite (only applicable with N4906B-012, no retrofit)
N4906B-102	Extension to full frequency range 150 Mb/s - 12.5 Gb/s + clock data recovery (only applicable with N4906B-012, no retrofit)

Calibration/test data:

N4901B-UK6	Commercial calibration with test data

Accessories:

N4910A	Cable kit: 2.4mm matched cable pair
N4911A-002	Adapter 3.5mm female to 2.4 mm male
N4912A	2.4mm, 50 Ω termination, male
N4915A-001	47 ps transition time converter 7.49 GHz; recommended for N4916B-003 (single-ended measurements: 2x N4915A-001, differential measurements: 4x N4915A-001)
N4914A-FG	Rack mount kit

Warranty:

R1280A	1 year Return-to-Agilent is included with every serial BERT N4906B.

Calibration:

R1282A	Calibration plans are available to order for 3 years; calibration interval 12 month.

Productivity Assistance:

R1380-N49XX	Remote productivity assistance or on-site productivity assistance.

Related Agilent Literature	Pub.No.
J-BERT N4903A Data sheet	**5989-2899EN**
86100 Inifniium DCA-J Data sheet	**5989-0278EN**
Agilent Physical Layer Test Brochure	**5988-9514EN**
ParBERT 81250 Product Overview	**5968-9188E**
Fast Total Jitter Solution, Application Note	**5989-3151EN**
3.125 Gb/s Serial BERT Data Sheet	**5989-4752EN**

For more information, please visit us at
www.agilent.com/find/N4900_series

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