

Keysight E9524A
MicroBlaze Trace Toolset

Data Sheet

Easily Trace Microblaze Software Execution with Keysight Microblaze Trace Core and Inverse Assembler

Keysight Technologies, Inc. and Xilinx have developed a logic analysis trace solution for Xilinx's MicroBlaze embedded processor that overcomes the traditional difficulties of tracing software execution using a logic analyzer. Combining the capabilities of a MicroBlaze inverse assembler with a specialized trace core simplifies measurement setup and reduces the number of pins required. In addition, the trace core overcomes the lack of visibility you encounter when you employ cache and pipelining, and unlocks the power of the logic analyzer to make accurate measurements. You get easy access to the insight you need to increase the quality of your design and ensure its timely completion.

MicroBlaze Inverse Assembly

For PC board layout, you enable the inverse assembler by first choosing the level of visibility you need and then routing the corresponding MicroBlaze signals to pins. The MicroBlaze inverse assembler allows a choice of instruction-side and/or data-side decoding, and can accommodate variations of bus widths and different combinations of the signals to allow maximum flexibility. For example, instruction-side decoding would require routing at least the MicroBlaze program counter signals (PC_Ex) and the valid cycle signal (Valid_Instr) to pins. Routing these signals to a specified layout allows for fast connection to a logic analyzer via mictor, Samtec, or soft touch probing. Or, you can connect the logic analyzer to these signals with individual flying leads attached to a berg strip or header.

Because FPGAs with MicroBlaze cores are reprogrammable, they can be traced late in the development cycle. As long as you have reserved a sufficient number of pins for debug, you can route trace required MicroBlaze signals to a specified pinout without PC board changes.

The Keysight inverse assembler for MicroBlaze reconstructs program flow by capturing the address of each executed instruction and looking up the associated opcode in the OMF (object module format) file. It then decodes the opcode into a MicroBlaze instruction, as shown in Figure 1.

Keysight logic analyzers also come standard with a source correlation window so you can setup a measurement at the assembly or source level.

Sample Number	Address	MicroBlaze Inverse Assembly	Cycle Type
13	0000 02B4	Read Data 0x3	Read Data
19	0000 01C4	addik r18,r0,0x0009	Instruction Other
20		Register r18 = 0x9	Write Register
24	0000 01C8	cmp r18,r3,r18	Instruction Other
25		Register r18 = 0x6	Write Register
28	0000 01CC	bti r18,0x000001ec	Instruction Branch
32	0000 01D0	lwi r3,r19,0x0020	Instruction Load/Store
33	0000 02B8	Read Data 0x3	Read Data
39	0000 01D4	addik r3,r3,0x0001	Instruction Other
40		Register r3 = 0x4	Write Register
44	0000 01D8	swi r3,r19,0x0020	Instruction Load/Store
45	0000 02B8	Write Data 0x4	Write Data
50	0000 01DC	lwi r3,r19,0x001C	Instruction Load/Store
51	0000 02B4	Read Data 0x3	Read Data
58	0000 01E0	addik r3,r3,0x0001	Instruction Other
59		Register r3 = 0x4	Write Register
63	0000 01E4	swi r3,r19,0x001C	Instruction Load/Store
64	0000 02B4	Write Data 0x4	Write Data
69	0000 01E8	bri 0x000001e0	Instruction Branch
78	0000 01C0	lwi r3,r19,0x001C	Instruction Load/Store
79	0000 02B4	Read Data 0x4	Read Data

Figure 1. Keysight's MicroBlaze inverse assembler reconstructs program flow. Results may be displayed in waveform or listing displays.

Debug Using Fewer Pins

Pins available for debug are often scarce, so the inverse assembler includes a capability that reduces the number of required pins. Although the MicroBlaze architecture has 32 PC_Ex signals, the number of external signals needed for capturing a logic analysis trace is typically significantly less than 32.

This reduction is accomplished using two different techniques. First, any upper address bits that are static do not need to be traced, so one pin can be eliminated for each static upper address bit in the program counter. You can specify this information via the logic analysis user interface. Second, the lower two address bits also do not need to be traced, since all instructions start on 4-byte boundaries. Using these techniques, tracing software execution of a 1-Mbyte program requires only 18 pins (plus 1 clock pin and 1 control pin). Keysight's MicroBlaze trace core provides further pin reduction by using a 2:1 time-domain-multiplexing capability in conjunction with the Keysight logic analyzer. This enables an additional 50% reduction in pins required for trace.

Correlate Assembly Mnemonics with High-Level Source Code, Even with Cache Enabled

MicroBlaze execution can be tracked deterministically, even when cache is enabled, since captured signals are routed from the execution stage of the MicroBlaze pipeline. This also makes the trace impervious to unused prefetches.

Keysight logic analyzers come standard with a source correlation window. By reading a symbol file (.elf format), the logic analyzer can associate captured addresses with the high-level software mapped to that address. When you step through assembly instructions, the equivalent line in the source code for this instruction is also highlighted. Or, step through high-level source code while the logic analyzer simultaneously displays the associated instruction mnemonics in the lower window. Right click in the source code to quickly set up the logic analysis trigger (trace specification) for the next acquisition, as shown in Figure 2.

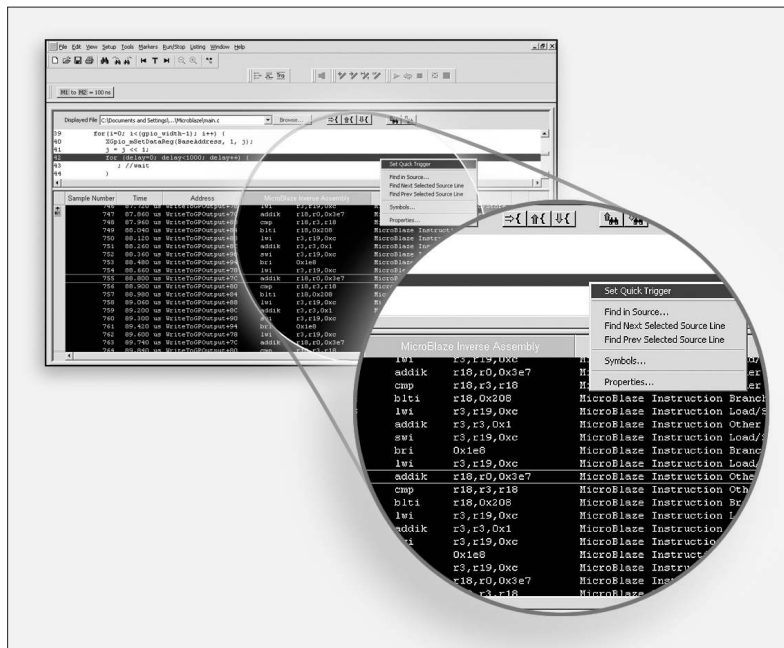


Figure 2. Keysight logic analyzers come standard with a source correlation window that provides correlation between assembly mnemonics and high-level source code. One-click trigger specification simplifies triggering on a specific line in the source code.

MicroBlaze Trace Core

The MicroBlaze trace core (MTC) reduces setup time and the number of pins required to trace a MicroBlaze processor instance. The MTC core, co-developed by Keysight and Xilinx, works exclusively with the Xilinx Platform Studio, which is included with the Xilinx embedded development kit (EDK) design flow. It allows you to graphically add an MTC core to your design. Core parameters include data values, status signals, pin compression using time division multiplexing, pin location, and I/O standard.

The MTC core works together with Keysight's FPGA dynamic probe logic analyzer software to provide four key benefits:

1. The MTC core connects required MicroBlaze signals to FPGA pins (pre-synthesis).
2. The core can be configured to reduce the number of pins required by a factor of two. Two MicroBlaze signals are time-division-multiplexed onto a single pin with data valid on the rising edge of the clock for signal one and data valid on the falling edge of the clock for signal two. A demux clocking mode in the logic analyzer decompresses the information and splits it into two separate logic analysis channels.
3. The MTC core includes auto pin-mapping that reduces initial setup time from hours to seconds and eliminates manual errors that can happen during the PC board layout. Tracing MicroBlaze can be done late in product development, as the MTC core eliminates the need to layout a PC board with a specific MicroBlaze signal pattern (see Figure 4).
4. Via JTAG, the logic analyzer sends an auto setup message to the MTC core. The core outputs a training pattern on a specific MTC pin. The logic analyzer looks for this training pattern across its channels and discovers which channel is connected to the MTC pin. By repeating this process for each MTC output pin, the logic analyzer learns how each MTC core input is routed through the core to pins and through connectors and/or probes to the logic analyzer.

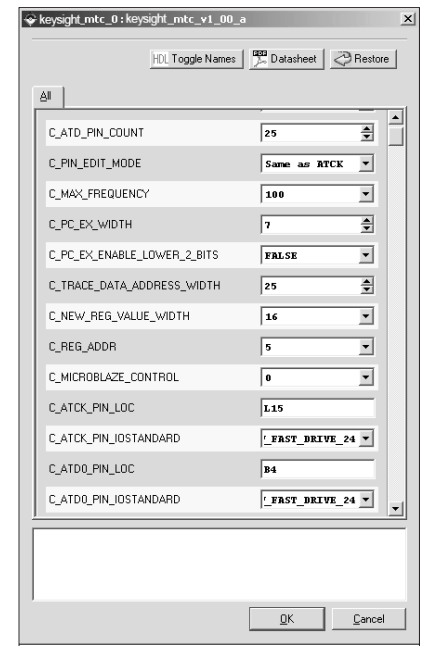


Figure 3. Keysight's MicroBlaze trace core (MTC) is inserted in your design using the tools supplied in Xilinx's EDK. When you select the MTC core to insert it, you can specify all of the relevant parameters of the core graphically to make it specific to your design.

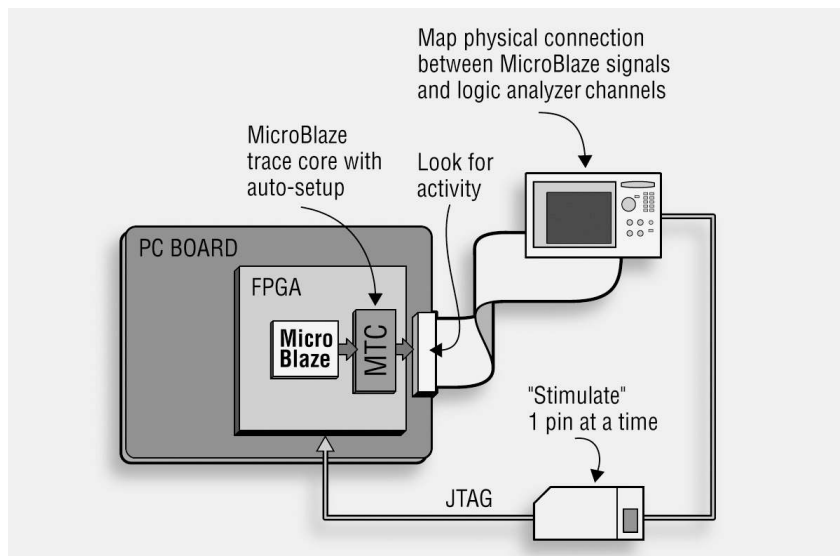


Figure 4. Keysight's MTC reduces the setup time for an initial trace measurement. You can literally connect a logic analyzer to a connector with MTC core outputs routed to it, and within seconds, the logic analyzer becomes ready to take a MicroBlaze trace measurement. In addition, the MTC core's pin compression technology reduces the number of required pins for tracing MicroBlaze processors by 50%.

5. The MTC core, constructed entirely of flops and LUTs, uses a multi-stage pipeline (typically four stages), as shown in Figure 5, to minimize the core's impact on the timing of your design. MTC cores are designed to be very small in terms of device resource consumption. An MTC core in a XC2V3000 device consumes roughly 1% of the LUTs and flops.

Keysight logic analyzers are equipped with precise time resolution, allowing them to correlate MicroBlaze execution history with other software or hardware events acquired simultaneously. This allows you to quickly isolate problems associated with hardware and software interaction. Keysight's royalty-free MTC core, distributed as part of the Xilinx EDK, minimizes the time to setup the measurement and eliminates the need for a specific PC board layout.

For more information visit www.keysight.com/find/microblaze.

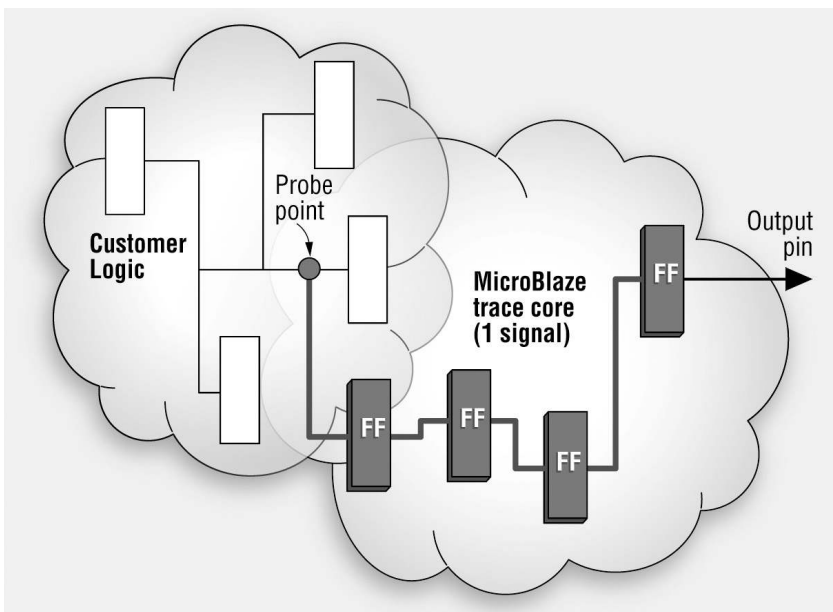


Figure 5. The thick lines show the flops and routes added by the MTC core. Since there is a flop in the fabric in addition to one at the I/O buffer, the router can use timing solely within the MTC core to move a signal across the chip, thereby minimizing the impact of the MTC core on the design's timing.

Quick Tour of the Application

Design step 1:

Create and instantiate an MTC core

Use Xilinx Platform Studio to select the MTC core and specify the parameters that best match your design needs. Parameters include data compression, status signals, and location.

Design step 2:

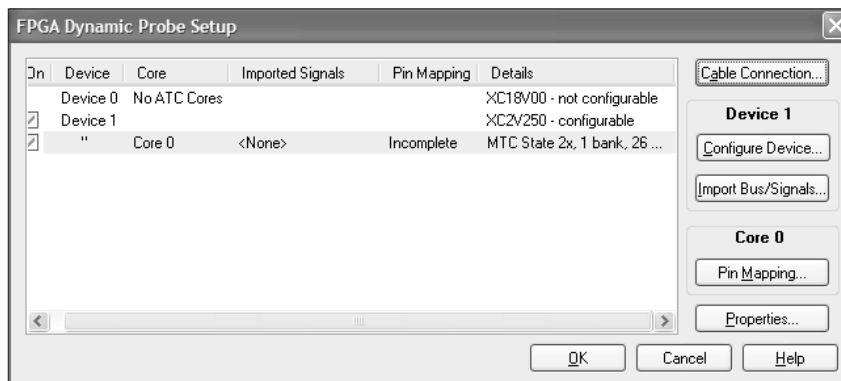
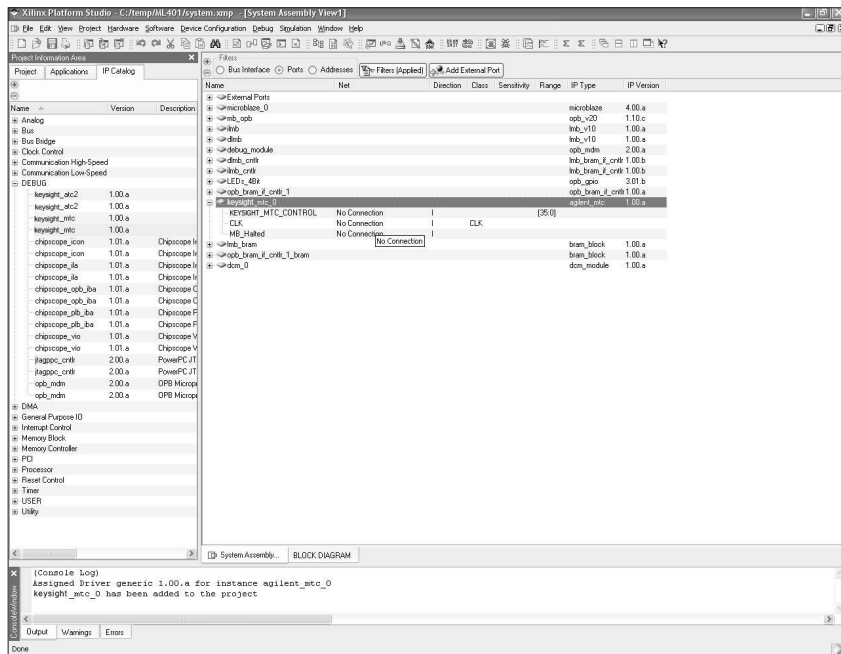
Implement your Xilinx FPGA design with MicroBlaze and MTC cores in place

Once the design is ready for prototyping in the FPGA, use the Xilinx tools to implement the design (generate the bitstream) including the MicroBlaze and MTC cores. You're then ready to set up the logic analyzer for measurement.

Measurement setup step 1

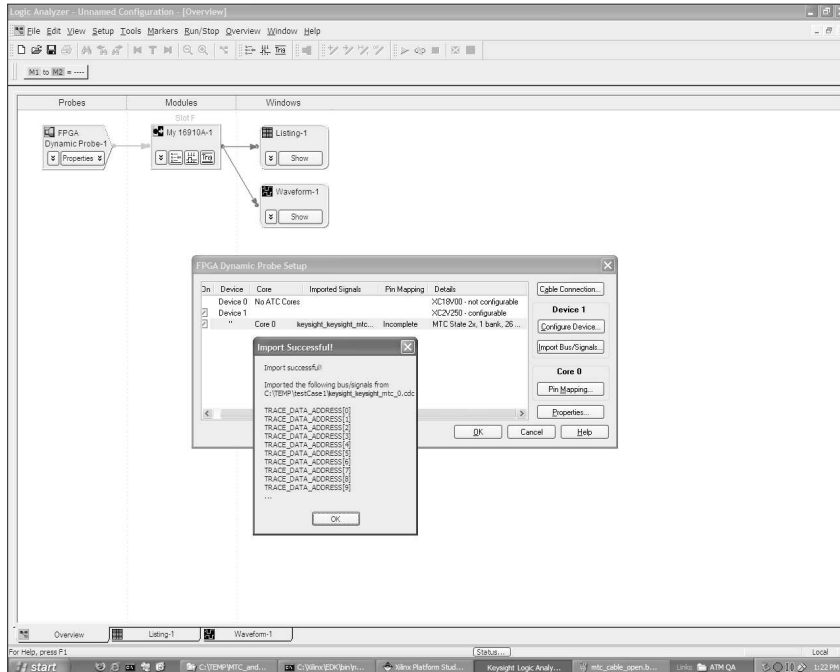
Activate FPGA probe: Identify MTC core

The FPGA dynamic probe application allows you to query the MTC core (via JTAG) and quickly set up the logic analyzer for a MicroBlaze measurement. It establishes a connection between the logic analyzer and a Xilinx cable, and shows what devices are present on the JTAG scan chain. You can define core and device names.



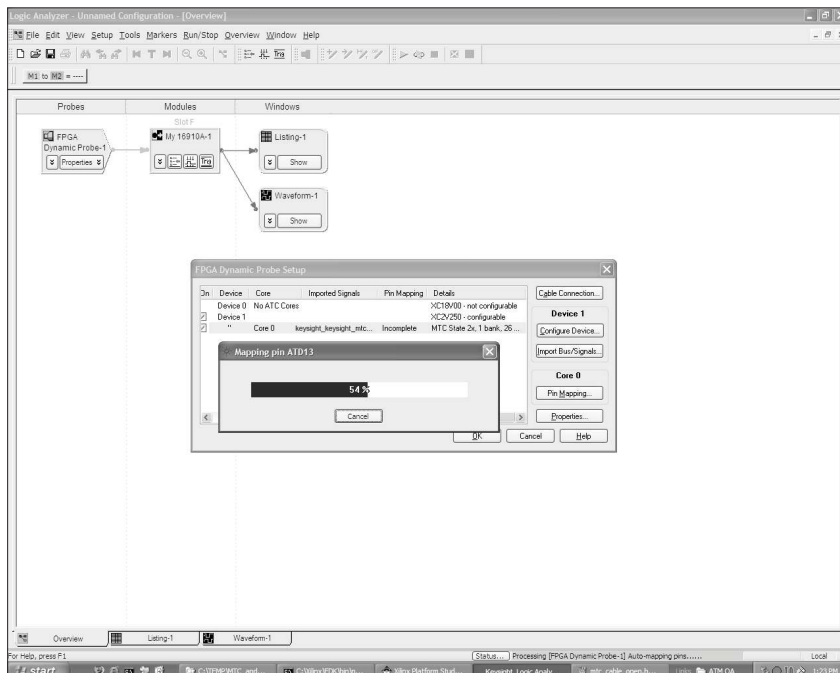
Measurement setup step 2: Import signal names

The FPGA dynamic probe application reads a .cdc file produced by the Xilinx EDK. The names of your MicroBlaze signals will now automatically show on your logic analyzer listing and waveform windows.



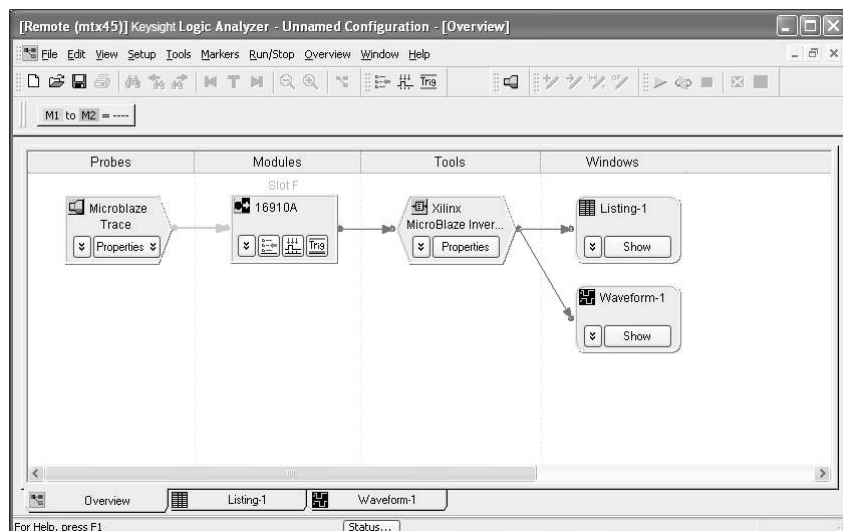
Measurement setup step 3: Map pins automatically in seconds!

Mapping the signals from the pins of the device to the proper logic analyzer channels is often a time-consuming and error-prone task. The MicroBlaze trace core includes an automatic pin mapping feature that reduces this tedious task to a few seconds and automates the entire process to eliminate errors.



Measurement setup step 4: Load the MicroBlaze inverse assembler:

Load the MicroBlaze configuration file and inverse assembler from the logic analyzer application software.



Setup complete: Make measurements!:

You're now ready to make trace measurements on your MicroBlaze embedded processor.

E9524A Specifications and Characteristics

Supported logic analyzers	
Standalone logic analyzers	1680 Series, 1690 Series, 16800 Series
Modular logic analysis systems	16900A, 16902A, 16903A with one or more state/timing modules: A single node-locked license will enable all modules within a 16900 Series system
Triggering capabilities	Determined by logic analyzer
Supported Xilinx FPGA families	Virtex-4, Virtex-II Pro series, Virtex-II series, Spartan-3 series
Supported Xilinx cables (required)	Parallel 3 and 4, Platform Cable USB
Supported probing mechanisms	Soft touch (34-channel and 17-channel), Mictor, Samtec, Flying lead

FPGA dynamic probe software application	
Maximum number of devices supported on a JTAG scan chain	256
Maximum number of ATC2 and MTC cores supported per FPGA device	15

MicroBlaze trace core characteristics	
Number of output signals	User definable: Clock line plus 4 to 128 signals in 1 signal increments
Inputs	User definable: Program Counter, Trace Data Address, Control Signals
Compression	Optional 2X pin compression via time division multiplexing. Logic analyzer decompresses the data stream
FPGA Resource consumption	Consumes no BUFs, DCM or Block RAM resources. See resource calculator at www.keysight.com/find/MicroBlaze

Compatible design tools		
EDK (Embedded Development Kit)	1680, 1690, 16800, 16900 Series SW Version	Primary New Features
8.2i	3.5 or higher	Support for MTC core using EDK flow

Additional information available via the Internet (www.keysight.com/find/FPGA) and www.keysight.com/find/fpga_FAQ.

Ordering Information

The Keysight E9524A MicroBlaze trace toolset includes:

Option 10:

- Entitlement certificate for perpetual node locked license
- CD with application software

Option 20:

- Entitlement certificate for perpetual floating license
- CD with application software

Related Literature

Publication Title	Publication Type	Publication Number
<i>Keysight Technologies 16900 Series Logic Analysis Systems</i>	Color brochure	5989-0420EN
<i>Keysight Technologies Measurement Modules for the 16900 Series</i>	Data sheet	5989-0422EN
<i>Probing Solutions for Keysight Technologies Catalog Logic Analyzers</i>	Catalog	5968-4632E
<i>Keysight 16800 Series Logic Analyzers</i>	Data sheet	5989-5063EN
<i>Keysight 16800 Series Logic Analyzers</i>	Color Brochure	5989-5062EN
<i>Keysight 1680 and 1690 Series Logic Analyzers</i>	Data Sheet	5988-2675EN
<i>Planning Your Design for Debug: FPGA Dynamic Probe</i>	Design Guide	5989-1593EN

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