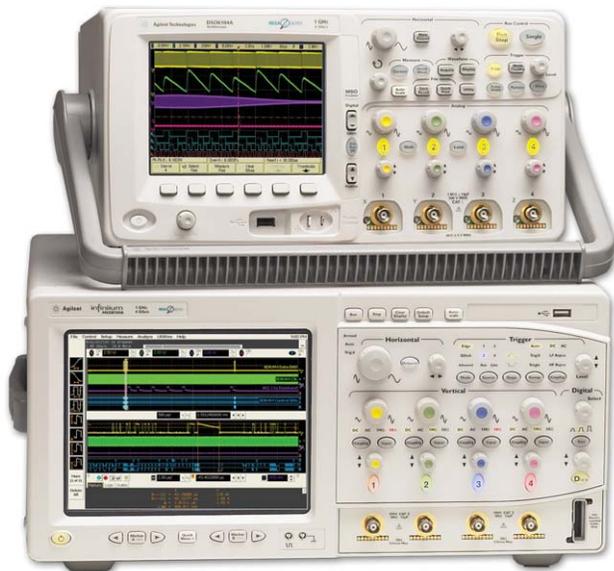


# Frequently Asked Questions N5433A and N5434A Agilent MSO FPGA Dynamic Probe for Altera

Data Sheet

## FAQ

This document addresses common MSO questions whose answers are not found in the N5433A and N5434A FPGA dynamic probe data sheets available at [www.agilent.com/find/6000-altera](http://www.agilent.com/find/6000-altera)  
[www.agilent.com/find/7000-altera](http://www.agilent.com/find/7000-altera)  
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Agilent's FPGA dynamic probe provides greater real-time measurement productivity for MSO-based validation of FPGAs and the surrounding system.

The tool features:

- Increased visibility – Traditional probing limits engineers to measuring signals at the periphery of the FPGA. With Agilent's FPGA dynamic probe, engineers are able to measure up to 256 internal FPGA signals for each external FPGA pin dedicated to debug.
- Faster probing changes – Agilent's FPGA dynamic probe enables your design team to move probe points internal to the FPGA with a mouse click – without any design changes and without any changes to the timing of your design.
- Automatic setup of the MSO – The FPGA dynamic probe maps internal signal names from your FPGA design tool to the labels on your MSO digital channels. The signal-naming capability of the Agilent FPGA probe eliminates mistakes and saves you the time it would take to manually set up signal and bus names and MSO digital channel connections, providing a significant advantage over instruments without this capability.



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## **Q1 What Altera Software is required to use Agilent's FPGA Dynamic Probe?**

You will need Altera's Quartus II FPGA Design Software, version 6.0 or higher. Quartus II includes Altera's Logic Analyzer Interface (LAI) that provides the MUX core and insertion mechanisms to enable FPGA dynamic probe.

The most typical use model with Infiniium MSOs is to run the FPGA dynamic probe application on the PC in your Infiniium MSO. You will need to also install Altera's Quartus II Programmer Software on your Infiniium MSO to provide the necessary drivers for control of the Altera JTAG cable.

For the Series 6000 MSO use model, run the FPGA dynamic probe application on your PC. The PC connects to your MSO via LAN, GPIB, or USB and passes setup information to the digital MSO channels. You will need to also install Altera's Quartus II Programmer Software on the same PC that FPGA dynamic probe application is running to provide the necessary drivers for control of the Altera JTAG cable.

## **Q2 I already put my own MUXes in my FPGA design to better utilize debug pins. How is this solution better?**

FPGA dynamic probe was designed to have minimal intrusion in both the design flow and the design itself. Here are the top areas where the FPGA dynamic probe solution will save you work and time, even if you already use your own MUXes.

1. FPGA dynamic probe does not require you to modify your HDL code. Altera's LAI Interface Editor lets you specify details of the MUX and automatically includes it in your FPGA. Teams not using FPGA dynamic probe must modify HDL code to include MUXes.
2. Control of which signals are presented for measurement is done from the FPGA dynamic probe GUI in about a second (only 2 mouse clicks). Teams not using FPGA dynamic probe must design in special capability (such as changing register values) to change which signals are presented to IO pins.

3. With FPGA dynamic probe, signal names are imported from the FPGA Design Tools and automatically updated in the MSO each time the user selects a new signal bank to measure. This saves considerable time and reduces errors over a manual process for making sure the MUX outputs are correctly reflected in the MSO.

## **Q3 When would I want to use an LAI state core (synchronous) versus a timing (asynchronous) core?**

### **State cores:**

- Are most typical as they provide synchronous measurements inherent to FPGA debug.
- Provide most-accurate measurements for functional debug in one time domain.
- Register outputs to synchronize sampling data with your system's clock.

### **Timing cores:**

- Are best for measurements across multiple time domains.
- Run at fastest-possible speed of device, no registering of MUX inputs or outputs.

## **Q4 Can I use FPGA dynamic probe with multiple MSOs?**

With option 002, a PC-locked license, the FPGA dynamic probe is licensed to the PC and not to the MSO. When the PC with the FPGA dynamic probe license connects to an MSO, the application is enabled on the connected MSO. So, a single PC with a license could be shared between multiple MSOs in a lab.

## **Q5 Who do I contact if I'm having problems?**

Altera provides the LAI Editor and core, including expertise on inserting the core into your design. Agilent's expertise is on the FPGA dynamic probe application. Agilent and Altera work together on issues that cross company boundaries.

**Q6 What if I didn't assign all of the signals of interest early when I created the LAI core?**

Altera supports incremental compilation in Quartus II with the LAI. This feature allows you to preserve the synthesis and fitting of your original design and add the LAI to your design without recompiling your original source code.

**Q7 Can I use the FPGA dynamic probe application to download configuration bits into my Altera FPGA?**

Yes.

**Q8 What Altera JTAG cables work with FPGA dynamic probe?**

Altera ByteBlaster, USB Blaster and MasterBlaster cables. The cable makes a connection between the parallel or USB port on your Infiniium MSO or PC, and the JTAG pins on the FPGA.

**Q9 Can I use a different clock on each bank or do I need a clock with each bank?**

Timing cores do not have a clock, because information is sampled asynchronously using the MSO's internal clock. For state cores, the LAI core has a master clock that is used for all banks.

**Q10 What limitations are there with signal and bus names on MSOs?**

Infiniium MSOs support up to 4 groupings of signals into buses. The application will automatically group signals into buses when appropriate. Additional signals will be displayed independently. Each signal or bus group is identified by a label of up to 16 characters.

Series MSOs support up to 2 groupings of signals into buses. The application will automatically group signals into buses when appropriate. Additional signals will be displayed independently. Each signal or bus group is identified by a label of up to 6 characters.

**Q11 How many simultaneous signals can I measure on an MSO?**

Infiniium and InfiniVision MSOs have 16 digital channels. If using LAI state cores, you will need to monitor the clock output to trigger on and view valid state measurements. This leaves 15 other digital channels available for simultaneously capturing 15 internal signals. Valid states can be found at the intersection of clock edges and signal patterns.

Infiniium MSOs have an added pseudo "state clock" feature. Specify the digital or analog channel that is connected to the LAI clock output. A post processing algorithm filters the digital channel acquisition and displays states that were valid on the clock edge exclusively. All intermediate states are filtered out to make state analysis measurements. When an analog scope channel acquires the LAI clock output, this leaves 16 simultaneous digital channels for signal capture.

**Q12 Which Altera FPGAs are supported?**

FPGA dynamic probe supports Altera Stratix, Stratix GX, Stratix II, Stratix II GX, Cyclone, Cyclone II, Max II, APEX II, Apex 20K, and Excalibur.

**Q13 What triggering resources are available with the FPGA dynamic probe?**

The full trigger resources of the Agilent MSO are available. For LAI state cores, state triggering will be specified by selecting an ANDing of the LAI clock output edge with the desired state pattern. Additionally, trigger conditions can include the MSO's analog channels.

**Q14 What special pinouts are required by FPGA dynamic probe?**

No special pinouts are required. The FPGA dynamic probe includes a graphical feature called graphical pin mapping. This feature lets you visually tell the tool how the FPGA physical pins that carry the MUX output are connected to the MSO channels. If you are using a traditional probing connection, such as a flying leads, Mictor or Samtec connector, or a soft touch probe, the graphic lets you specify the location of each LAI output.

**Q15 How do I trigger on and display valid states on an Infiniium MSO?**

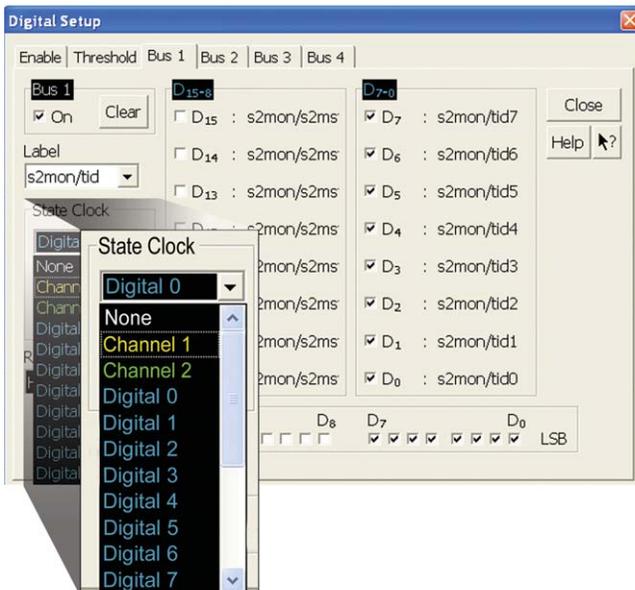
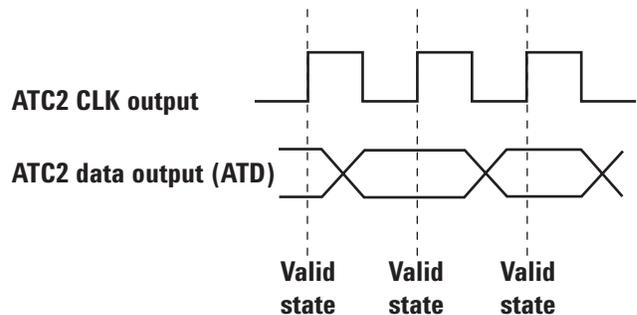
Infiniium MSOs incorporate some logic analysis state capabilities useful for making FPGA measurements. Using pattern trigger, setup a state trigger on ATC2 clock edge and desired digital pattern.

After acquiring the data, use the post-processing “State clock” feature to transform the timing waveforms into state waveforms. Valid states are shown and invalid states are filtered. Any of the 16 digital channels or any of the analog channels can be set as the state clock. Using an analog channel state clock allows you to retain all 16 digital channels for bus measurement.

**Q16 How do I trigger on and display valid states on an InfiniiVision 6000 or 7000 Series MSO?**

InfiniiVision MSOs incorporate logic state triggering for triggering on specific states. Because the ATC2 core outputs both the clock signal and bus values, triggering on the combination ensures your state trigger is valid—even though the MSO digital channels are sampling asynchronously

Set up a valid state trigger by specifying the appropriate ATC2 clock edge and the desired bus/signal pattern. Track valid states by measuring the bus value on each clock edge.



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