

Keysight 4082F Flash Memory Cell Parametric Test System

A Complete Solution for Evaluating Write/Erase
Characteristics of Flash Memory Cells

Application Note



Introduction

The production testing needs of modern high-density NAND flash memory processes and novel flash memory technologies such as multi-level cell (MLC) and charge-trapped flash memory present many new measurement challenges. The Keysight 4082F Flash Memory Cell Test System, which utilizes a new high-voltage semiconductor pulse generator unit (HV-SPGU), meets the production parametric testing needs of these advanced non-volatile memory technologies. The Keysight 4082F provides high throughput, high resolution, and high repeatability for the write/erase endurance testing of a wide variety of state-of-the-art flash memory cells.

Driven by strong growth in MP3 music players and the digital camera markets, the demand for NAND flash memory as a mass storage medium continues to grow at a rapid pace. The expected replacement of smaller hard disk drives with flash memory will only continue to accelerate this trend, as will the increased use of integrated flash memory in microcontrollers to store program code. These market forces have also accelerated the need to decrease costs and increase densities by reducing the memory cell area through such means as multi-bit cells and charge trap flash memory. For this reason, the ability to create precise voltage pulses to evaluate the write/erase characteristics of these advanced flash technologies has become very important in both process development and production. The Keysight 4082F and HV-SPGU form a complete solution to evaluate the write/erase characteristics of these types of advanced flash memory.

The key features of this solution include:

- High voltage pulsing capability The HV-SPGUs can output ± 40 V (80 V peak-to-peak) with a programmable rise/fall time from 20 ns¹ to 400 ms, which meets the needs of modern NAND flash memory cell testing.
- High resolution voltage forcing capability The output waveforms can be programmed with 0.4 mV resolution, which provides a stable and clean pulse waveform for the evaluation of multi-level flash memory cells.
- Improved switching speeds The pulse switch used to create an open drain connection during the erase cycle has been improved from 2 ms (on the Keysight 4070 Series) to 500 μ s, which reduces the total time required to complete a write/erase endurance test.
- Cost effectiveness Each HV-SPGU module has two independent channels that can each output two or three level pulses, which reduces the number of pulse generator units required versus using external, off-the-shelf pulse generator instrumentation.
- Arbitrary Linear Waveform Generator (ALWG) The ALWG feature simplifies the creation of complicated pulse waveforms of four levels or more, which makes it easy to test novel non-volatile memory cells.
- Test Instruction Set (TIS) compatibility between the 4070 and 4080 The TIS commands used to control the 4082F are structured to maintain compatibility with the TIS commands used on the 4070 Series, which make it easy to migrate from the 4070 Series to the 4082F and to maintain a mixed test floor environment. Note: The HV-SPGU is also supported on the 4070 Series².
- Fast and reliable operation The 4082F is designed to provide high-throughput with high reliability in a production wafer test environment.

High voltage pulses with programmable transition times for NAND flash memory test

As previously mentioned, two features are essential for the testing of modern NAND flash memory cells: large voltage amplitude pulses and fast rise/fall times. The 4082F and HV-SPGU meet these needs with ± 40 V (80 V peak-to-peak) pulse generation capability into a high impedance load (see Figure 1) and a programmable pulse rise/fall time from 20 nsec¹ to 400 msec. However, pulse overshoot is also a major concern when testing flash memory cells, and the 4082F solution also addresses this issue.

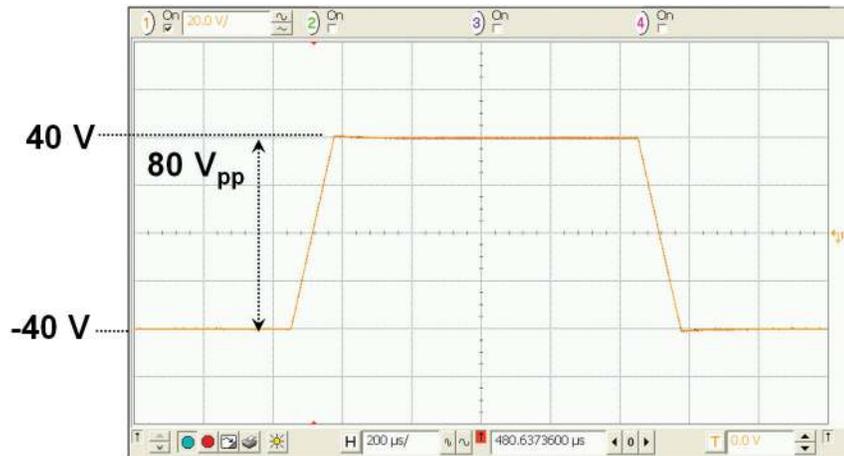


Figure 1. The HV-SPGU has ± 40 V output capability.

The write/erase characteristics of flash memory cells are strongly dependent on the applied voltage. This means that eliminating pulse overshoot is crucial to correctly evaluating flash cell performance. Since modern NAND flash technologies require up to ± 40 V voltage swings, pulse overshoot is a serious challenge. A programmable rise/fall time capability is one means to overcome this issue, since increasing the rise/fall time is the fundamental way to remove pulse overshoot and ringing.

Prior to the introduction of the HV-SPGU, the 4070 Series had to use the Keysight 8114A high power pulse generator for NAND flash memory cell test. However, the rise/fall time of the 8114A is fixed at approximately 6.5 ns, which is too fast to avoid creating an overshoot after passing the voltage pulse through the 4070 test head. To solve this issue, the 4070 Series uses a transition time converter to decrease the rise/fall time of the 8114A to 65 ns. Unfortunately, even this rise/fall time is not slow enough to prevent a pulse overshoot for certain combinations of the 4070 test head with the device under test (DUT).

Figure 2 (following page) shows a comparison of waveforms measured at the pogo-pins of the testhead through the high frequency port of the Keysight 4082F for both the 8114A and HV-SPGU (the waveform is being monitored by a passive probe with 10 M Ω equivalent loading). For the 8114A case, waveforms both with and without the transition time converter are shown. As can be seen, the 8114A pulse without the transition time converter exhibits a significant overshoot and ringing; the 8114A pulse with the transition time converter has a rise time of about 55 ns and a greatly reduced overshoot and ringing (although both are still observable). In contrast, the HV-SPGU with a programmed rise time of 55 ns shows less overshoot and ringing than the comparable case using the 8114A and transition time converter, illustrating the superior design of the HV-SPGU. For the HV-SPGU case, any remaining overshoot can be removed by increasing the rise time. Figure 3 shows how reducing the rise time decreases the pulse overshoot.

1. The minimum rise and fall times are 20 ns when $|V_{amp}| \leq 10$ V and 30 nsec when 10 V $< |V_{amp}| \leq 20$; both of these cases are for a 50 Ω load. V_{amp} = Amplitude of the pulse
2. This requires the latest version of the system software running on Linux; please confirm the required software environment.

The write/erase characteristics of NAND flash memory cells strongly depend upon the voltage pulses applied to them. This makes the control of the write/erase pulse overshoot a critical factor for process characterization and monitoring. The superior performance of the HV-SPGU versus that of the 8114A demonstrates that the HV-SPGU is almost mandatory for testing of state-of-the-art NAND flash memory cells.

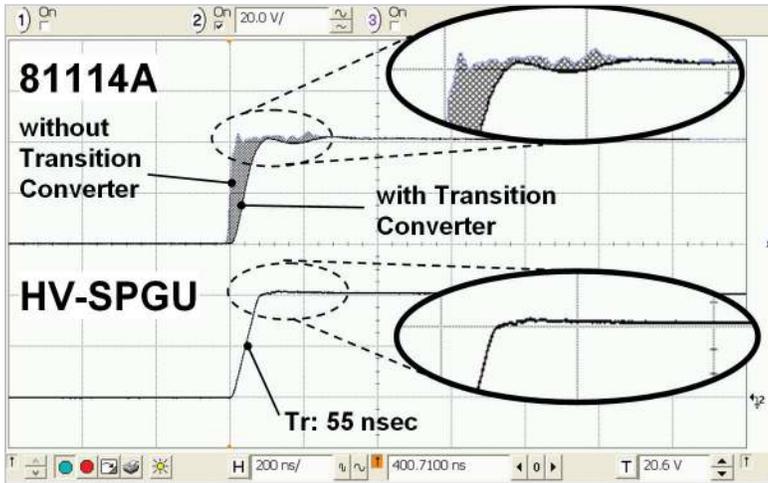


Figure 2. Overshoot comparison between the 8114A and the HV-SPGU.

Improved pulse resolution, accuracy and repeatability meet the needs of multi-level cell flash memory

More so than traditional flash memory cells, multi-level cell (MLC) flash memory require extremely accurate voltage pulses for writing and erasing to insure that the correct data bit is accessed. The 4082F addresses this need with vastly improved voltage pulse resolution.

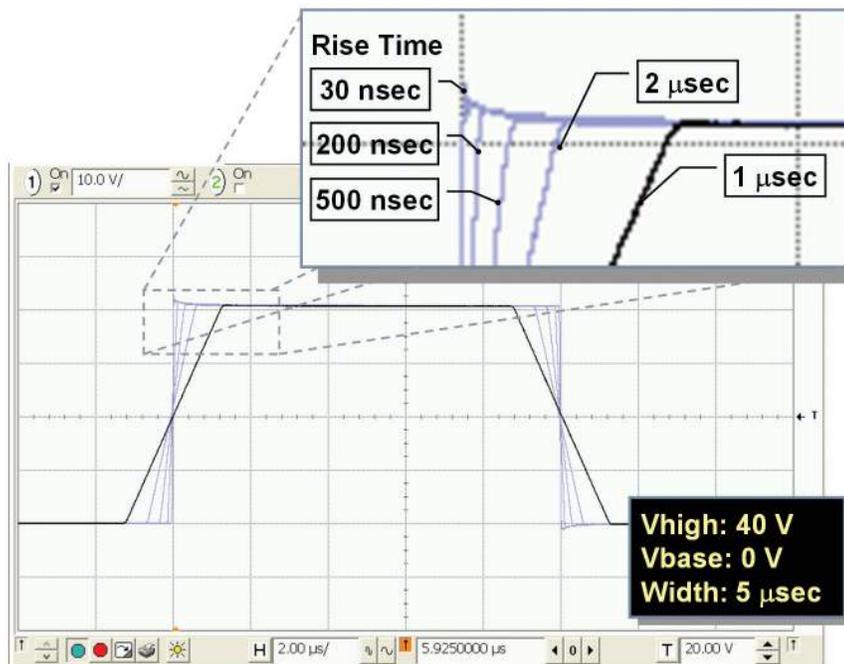


Figure 3. Reducing overshoot by increasing the rise time.

Prior to the introduction of the HV-SPGU, the most accurate pulse generator for the 4070 Series was the Keysight 81110A pulse pattern generator. The output voltage pulse force resolution of the 81110A is 100 mV. However, the output pulse force resolution of the HV-SPGU in the 4082F is 0.4 mV, which represents more than a 100x improvement in performance. Moreover, the accuracy and stability of the HV-SPGU's output voltage are also improved relative to that of the 81110A.

Figure 4 shows voltage pulses created by the HV-SPGU and the 81110A (81111A module installed) overlaid. The force pulse target value is 5 V, the pulse width is 1 ms, and the waveform is being monitored by a passive probe with 10 M Ω equivalent loading. As can be seen, the output of the 81110A exhibits a noticeable offset from the target value of 5 V, but the HV-SPGU is exactly at 5 V.

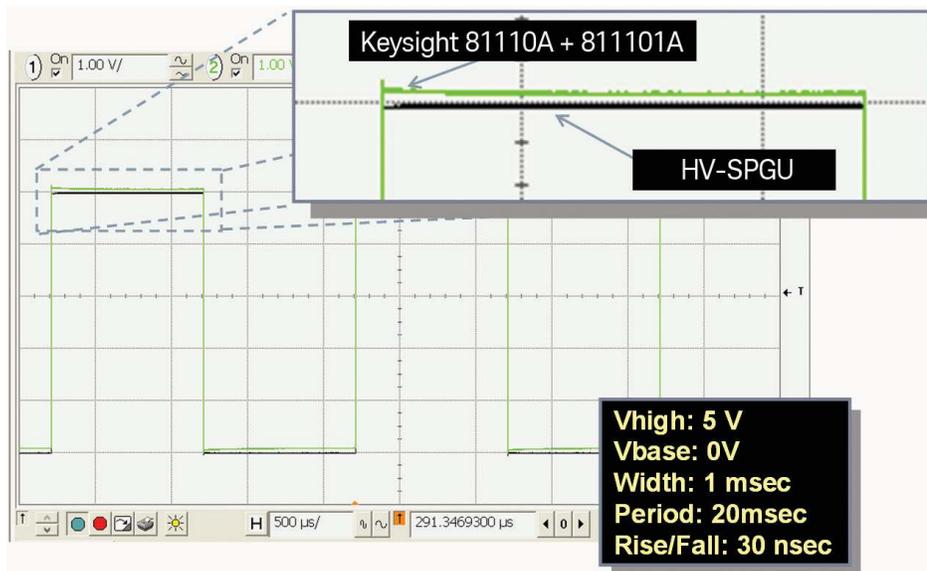


Figure 4. Accuracy level comparison between 81110A and HV-SPGU (at 5 V).

Besides having significantly better voltage resolution than the 81110A, the HV-SPGU also has an integrated calibration module. The calibration module periodically checks the HV-SPGU circuitry to make sure that its accuracy is maintained and not affected by factors such as changes in the ambient temperature. In addition, the HV-SPGU output circuitry uses a feedback loop to prevent voltage fluctuations due to circuit self-heating that would otherwise occur in an open loop design.

Figure 5 shows how the output of the HV-SPGU remains stable at higher output voltages. The pulse target value is 20 V, the pulse width is 1 ms, and the waveform is being monitored by a passive probe with 10 M Ω equivalent loading (same conditions as Figure 4). As the expanded portion of this figure shows, the HV-SPGU output remains stable for the entire pulse width whereas the 81110A pulse shows a noticeable droop.

In summary, the high resolution, high accuracy, and high stability of the HV-SPGU ensure that you can perform accurate and repeatable characterization of MLC flash memory.

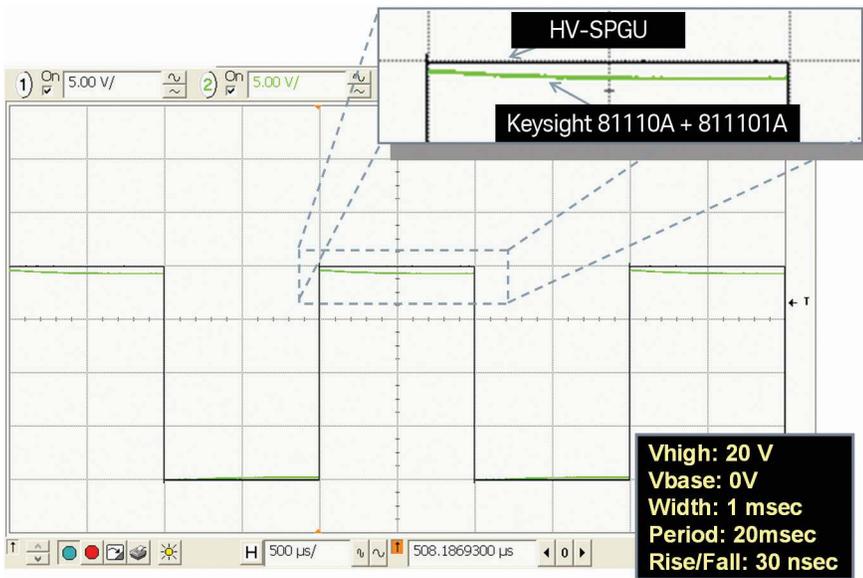


Figure 5. Pulse stability comparison between the 81110A and the HV-SPGU.

Faster hardware dramatically accelerates flash memory cell write/erase endurance testing

In addition to improving the quality of the output pulse in the 4082F flash cell testing solution, the speed with which write/erase characterization and endurance testing can be performed has also been enhanced.

A couple of new features significantly improve the operating speed of the HV-SPGU relative to that of the 81110A and 8114A. One basic improvement is simply the operating speed of the HV-SPGU, which is much faster than that of the 81110A and 8114A. Another improvement is that the HV-SPGU was designed to be an integrated component of the 4082F system. The HV-SPGU can communicate to the 4082F controller its status in real time, so there is no need to factor in added wait times to guarantee the completion of 81110A and 8114A pulsing operations.

Figure 6 shows comparative oscilloscope traces monitoring a pulse sequence for the HV-SPGU and the 81110A. The pulse widths are 1 ms and the top level of the pulse is changing from 1.0 V to 2.0 V in 0.5 V steps. The HV-SPGU and 81110A are being programmed via TIS commands using the C programming language on a Linux controller. Note that in the case of the HV-SPGU there is only about 13 ms between pulses, whereas in the case of the 81110A there is 660 ms between pulses!

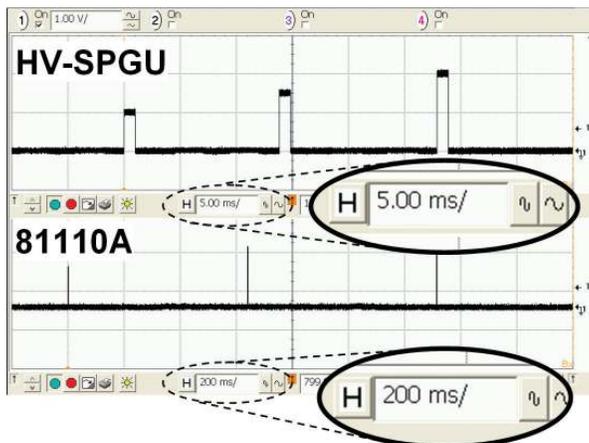


Figure 6. Pulse level switching speed comparison between the 81110A and the HV-SPGU.

This illustrates how significant the faster operation of the HV-SPGU can be, especially when characterizing MLC flash memory where the pulse width and pulse amplitude need to be changed frequently.

Besides improvements to the pulse generator, the Keysight 4082F also has a faster pulse switch unit to create an open connection to the DUT (relative to the 4070 Series). Figure 7 shows a diagram of the pulse switch unit. This unit has three multiplexers to switch the pulse source and four switches to create the open state. The pulse switch unit can be controlled by both TIS commands and by pulses synchronized with pulse streams being used to write or erase a flash memory cell. When controlled via pulsing the pulse switch unit can toggle in 500 μ sec (versus 2 ms on the 4070 Series), since the overhead associated with the controller sending out TIS commands is nonexistent. For a one million cycle write/erase endurance test, this would equate to a reduction in the switching time overhead from 2,000 seconds to 500 seconds.

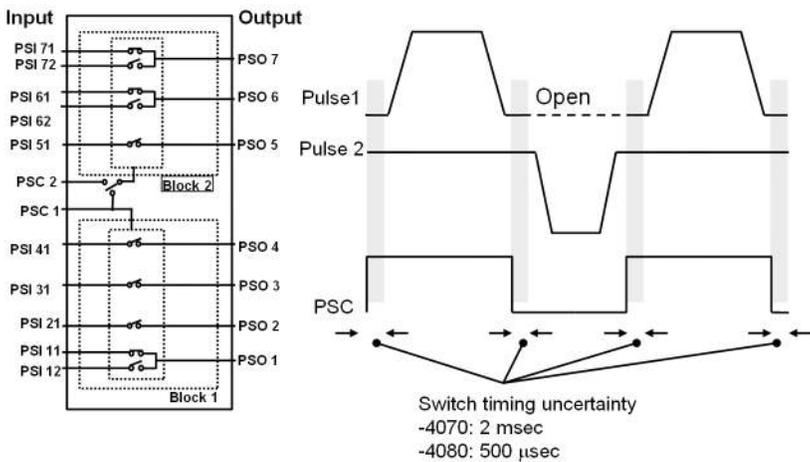


Figure 7. Pulse switch unit speed comparison between the 4070 and 4080.

Three-level pulsing capability on each channel lowers the cost of write/erase endurance testing

Creating a three-level pulse, which is simply a pulse that has two levels that are different from its base level, is required to apply alternating write and erase pulsing to flash memory cells. Unlike the 81110A and 8114A, each of the two channels on the HV-SPGU can independently generate three-level pulses. Moreover, the three levels can be selected arbitrarily anywhere from within the -40 V to +40V output range of the HV-SPGU (see Figure 8).



Figure 8. The HV-SPGU can output a three-level pulse with ± 40 V output swings.

Another important pulse generator capability is the ability to create accurate and synchronized write and erase pulse widths on multiple channels, even when the pulse widths differ by many orders of magnitude. This is due to the fact that generally the widths of write pulses are on the order of microseconds, while the widths of erase pulses are on the order of milliseconds.

Figure 9 shows an oscilloscope plot of a “typical” write and erase pulse sequence. The waveforms are generated by two different HV-SPGU channels, and consist of three-level write and erase pulses that vary from microseconds to milliseconds. The width of the first pulse on output channel one is 1 μsec and the width of the second pulse on output channel one is 1 ms. The width of the first pulse on output channel two is 800 ns and the width of the second pulse on output channel two is 800 μs . From this figure it is easy to see that the write and erase pulses are well synchronized even though the write and erase pulse widths on the two channels are vastly different.

It is worthwhile to point out that, since two 81110A channels are required in order to generate a three-level pulse, it would take two 81110As to create a pulse sequence similar to that shown in Figure 9. In contrast, as already mentioned only one HV-SPGU module is required to do this since each channel can independently output three-level pulses. This feature helps to reduce the total system cost of performing write/erase testing on flash memory cells.

Complex waveform synthesis capability for testing novel memory devices

While the 4082F and HV-SPGU flash cell test solution can provide significant cost savings and throughput improvements for process monitoring and wafer acceptance testing on the production line, it can also be used for research and development (R&D).

The new arbitrarily linear waveform generator (ALWG) function available on the HV-SPGU supports the creation of complicated pulse sequences such as those required for the characterization of novel non-volatile memory technologies like charge trap flash memory. ALWG waveforms consist of a combination of line segments, and each HV-SPGU channel can store up to 1024 points. The time between the points can be specified from 10 ns to 671.08863 ms, with 10 ns resolution. Up to 512 different waveform patterns can be stored in each channel, with one point from each ALWG waveform required as a delimiter between waveforms. The output ordering and repetition of each stored waveform can be arbitrarily specified to create the desired output sequence, and each pattern can be repeated up to 1,048,576 times.

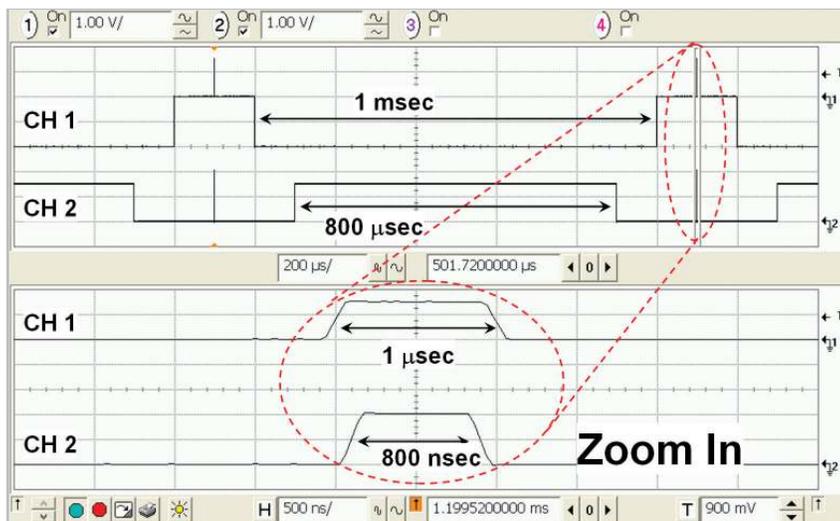


Figure 9. The HV-SPGU has excellent synchronization between the write and erase pulses.

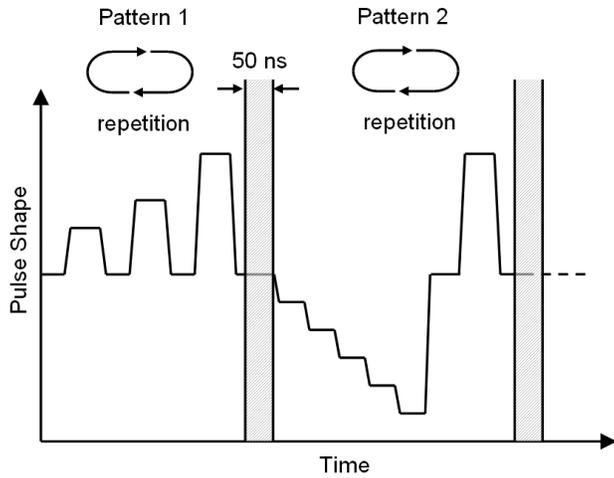


Figure 10. 50 ns is required to switch between ALWG patterns.

Figure 10 illustrates the timing between repeated waveforms when using the ALWG function. Note that although there is 50 ns of overhead time required when moving from one pattern to the next, there is no overhead time required during the repetition of the same pattern. Figure 11 shows the oscilloscope trace of an actual waveform created using the ALWG function. Pattern 1 consists of pulses at five different levels; pattern 2 consists of the combination of a negative staircase sweep and a single positive voltage pulse. Pattern 1 is repeated twice while pattern 2 is repeated once. Note that there is no overhead time associated with the repetition of pattern 1 (dotted line), while 50 ns of overhead time is needed during the transition between the two patterns (solid line).

One area where the ALWG function can be used to reduce write/erase endurance test times is MLC flash memory. MLC technology requires pulse steps with more than four levels, which can easily be done using the ALWG function with no overhead time penalties. Another application is to create small staircase pulses rather than one large pulse to prevent a sudden large current pulse that could damage a device, or to deactivate the damage caused by stress during the erase sequence on flash memory cells.

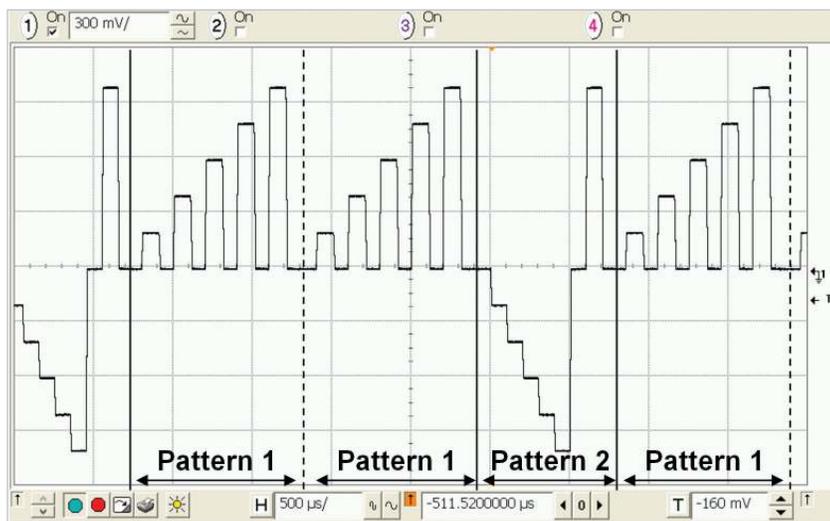


Figure 11. ALWG example showing repeated waveforms.

Standard furnished software tools facilitate flash cell test program development

The Keysight 4070 Series and 4082F testers provide tools to support test program development as part of their standard system software.

The TIS commands used to control the 4082F are structured to be compatible with the TIS commands used on the 4070 Series by maintaining basic compatibility with the Keysight 81110A and 8114A pulse generators. This feature makes it easy to migrate from the 4070 Series to the 4082F and to maintain a mixed test floor environment.

The interactive debug panel (IDP) also has features to help users design complicated write/erase pulse sequences. Using IDP, pulse parameters can be defined via a set of fill-in-the-blanks menus and the pulse waveform can be previewed in a special pulse generator preview window (see Figure 12). In the pulse generator view the waveforms of all of the output channels defined within the IDP are displayed; included in the display is the overhead associated with the pulse switch so that the user can visually confirm the timing of the pulse sequences.

IDP also has the ability to generate the equivalent program code in BASIC/UX and C for the waveforms interactively created with the IDP waveform generation tool. This program code can be executed as a standalone program or as a subroutine within the user's library, which can dramatically accelerate test program development.

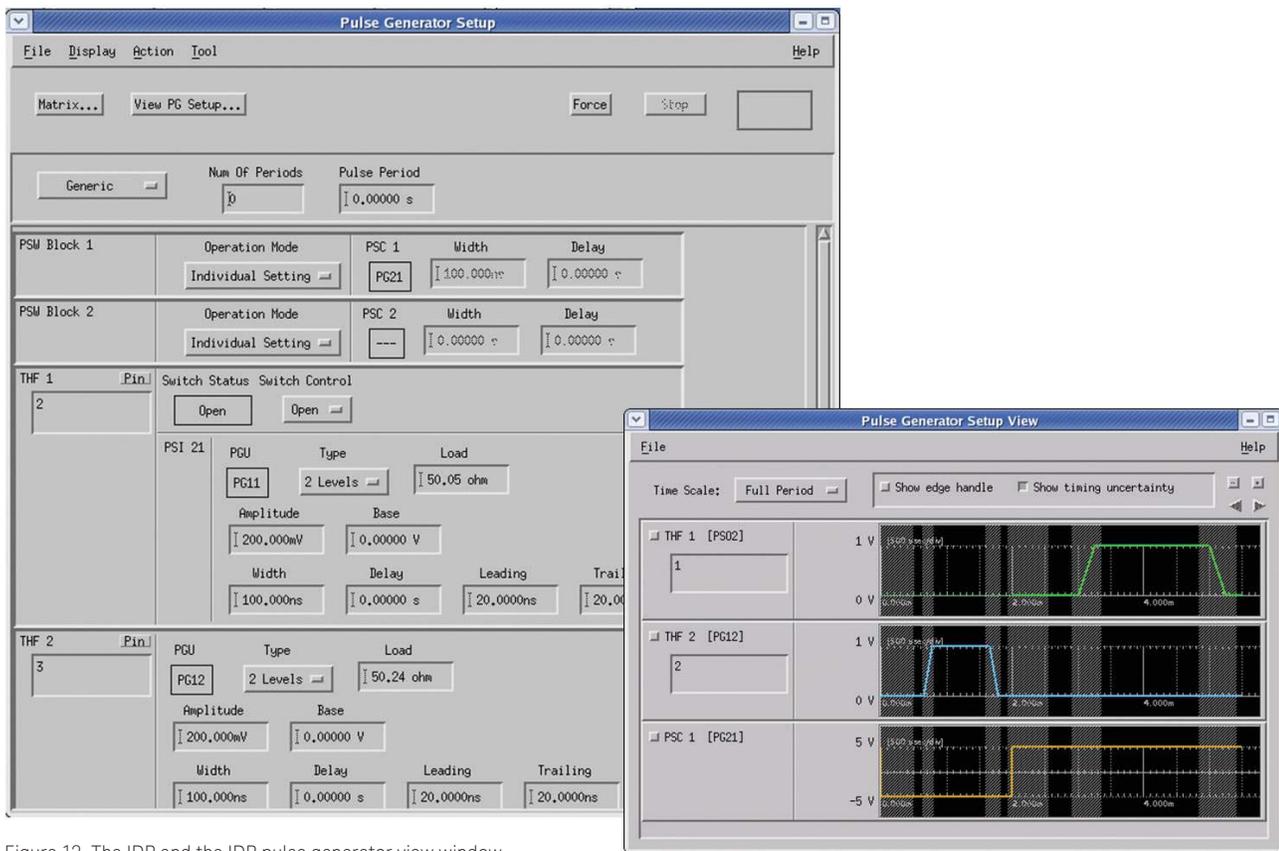


Figure 12. The IDP and the IDP pulse generator view window.

Built-in design for reliability improves MTBF

The HV-SPGU was designed to be a component of the 4082F and 4070 Series systems. As such the HV-SPGU is designed to strict reliability standards. The 81110A and 8114A are instrument products and are not designed to meet the same standards as the HV-SPGU. This means that by using the HV-SPGU in the 4082F and 4070 Series tester, the mean time between failure (MTBF) is better than that obtained using the 81110A and 8114A.

Summary

The new Keysight 4082F and HV-SPGU combine to create a complete solution for state-of-the-art flash memory cell technologies. The ± 40 V output capability of the HV-SPGUs meets the needs of modern NAND flash testing. The 0.4 mV output force resolution of the HV-SPGU permits the characterization of voltage sensitive devices such as MLC flash. The improved switching speeds reduce the time it takes to switch between write and erase cycles, thereby improving throughput. With two independent channels per HV-SPGU (each capable of outputting three-level pulses), the 4082F also provides both faster write/erase pulse streams as well as improved cost-effectiveness. The ALWG function permits the creation of complex waveforms for the characterization of novel new flash cell technologies. Compatibility between the 4082F and 4070 Series TIS commands both eases migration onto the 4082F platform and simplifies maintaining a mixed production test floor environment. Finally, the built-in reliability of the new HV-SPGU offers improved uptime relative to solutions using the 81110A and 8114A. These features ensure that you should be able to meet both known and unknown flash memory cell production test needs, and that your test investment is well-protected into the future.

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