Agilent EEsof EDA

The 2001 CAD Benchmark Rat-Race Mixer Characterisation

Eagleware Accuracy Proven in 40 GHz Benchmark

Abstract

In October 2001, Microwave Engineering Europe magazine threw down the gauntlet: a 36 GHz rat-race diode mixer complete with IF, RF, and LO filters. CAE software vendors were challenged to provide simulated results for this problem for later comparison with actual measured results. Accurate analysis required co-simulation of linear, nonlinear, and electromagnetic engines – a feature only available in Eagleware's GENESYS. These pages contain Eagleware's submitted simulations as well as the final MEE article outlining the measured results.

Read all about the benchmark inside!

The 2001 CAD Benchmark

Rat-race mixer characterisation

This document contains:

1. The original benchmark specifications submitted to CAD vendors by Microwave Engineering Europe Magazine.
2. The original simulation information submitted to Microwave Engineering Europe by Eagleware. This simulation information was sent to the magazine before publication of the benchmark specifications in the October, 2001 issue of MEE.

The 2001 CAD Benchmark

Rat-race mixer characterisation

Introduction

Mixer performance is key to the successful operation of modern communication systems and the accurate simulation of mixer characteristics is desirable in order to produce "right-first-time" designs necessary for the high-volume low-cost telecommunications market. The rat-race mixer when fabricated on microstrip offers high performance in a simple structure. It is a single-balanced mixer that is particularly convenient for microwave/mm-wave MMIC multi-chip modules as it can be fabricated on the same microstrip substrate that has the interconnecting lines for the various MMICs.

The problem

Fig. 1 shows a graphical representation of the rat-race mixer under consideration. It uses two Schottky beam-lead diodes (Agilent HSCH-9101) connected to a hybrid ring. The RF, LO and diode connections to the ring are made in such a way as to provide certain phase characteristics to the RF and LO signals to achieve cancellation of either LO or RF harmonics and also isolation between the LO and RF ports. One of the diodes has the anode grounded while the other has the cathode grounded. The DC return for the diodes is provided through a grounded via while a radial stub provides a good RF ground.

A limiting factor to the performance of the rat-race mixer is the extraction of the IF. In this topology, the IF is extracted from a port on the hybrid ring. This degrades the performance of the rat-race somewhat. A low pass high-impedance low-impedance microstrip filter is connected to the IF port, while an edge-coupled bandpass filter is connected to both the RF and the LO ports (a single section is used in the case of the LO while a 3-section filter is used in the RF path). The RF filter also employs a shield (dimensions 3 mm wide by 2mm high) that prevents interaction between the radiating filter sections and other components. The filter shield is grounded through vias that can be seen in Fig. 1. The rectangular pattern around the vias is metallised. The RF and LO connections to the test structure are made through V-series coaxial launchers on to the microstrip and the IF connection is made with an SMA connector. There is no enclosure on top of the test structure.

Given the nature of the hybrid ring and RF edge-coupled filter sections of the mixer, it would be desirable to perform EM simulation on these parts separately, however the method of importing these results into the subsequent non-linear simulations (and the need for optimisation in the design stage) is non-trivial and an interesting aspect of the outputs from the various vendors will be their strategy in this regard.

Dimensional data

The rat-race dimensions are determined by the frequency of operation (due to the spacing between the ports being various fractions of a wavelength). This mixer is designed to operate at 37GHz. Figures 2 details the dimensions of the structure. The layout file will be provided in electronic format to the CAD vendors.

Substrate

The substrate used for the fabrication of the mixer is Rodgers Duroid 5880, 0.254mm thick with an ε_r of 2.2. The metallisation is ¼ oz. Cu on both sides with 2-3 µm of Au.

Outputs

1) Schematic and test bench printouts with annotation

2) S-parameter data for the hybrid ring and filters separately

3) Following data over the frequency range 35 – 40GHz, with an LO frequency of 35GHz, as both up- and downconverter:

    i. Conversion loss for LO powers between +5 to +15 dBm in steps of 2 dB

    ii. VSWR of all ports

    iii. Port – to – port isolation

    iv. Compression test

4) Table of spurious responses for the following conditions

    i. LO 35GHz, +12 dBm,

    ii. RF 37GHz, -20 dBm

    iii. LO 35GHz, +12dBm,

    iv. RF 37GHz, 0dBm

    v. LO 35GHz, +12 dBm,

    vi. RF 37GHz, +5dBm

5) Comments on simulation strategy used i.e. whether EM simulation was used for the hybrid ring and filter simulation and how this was integrated into the non-linear simulation (it is hoped that this strategy would allow for optimisation)

6) Setup data

7) Hardware data: make/model, operating system, clock speed, RAM fitted, number of CPUs

8) Software data: name, version, elapsed run times, RAM/disk space needed, number of elements used (or cells/unknown)

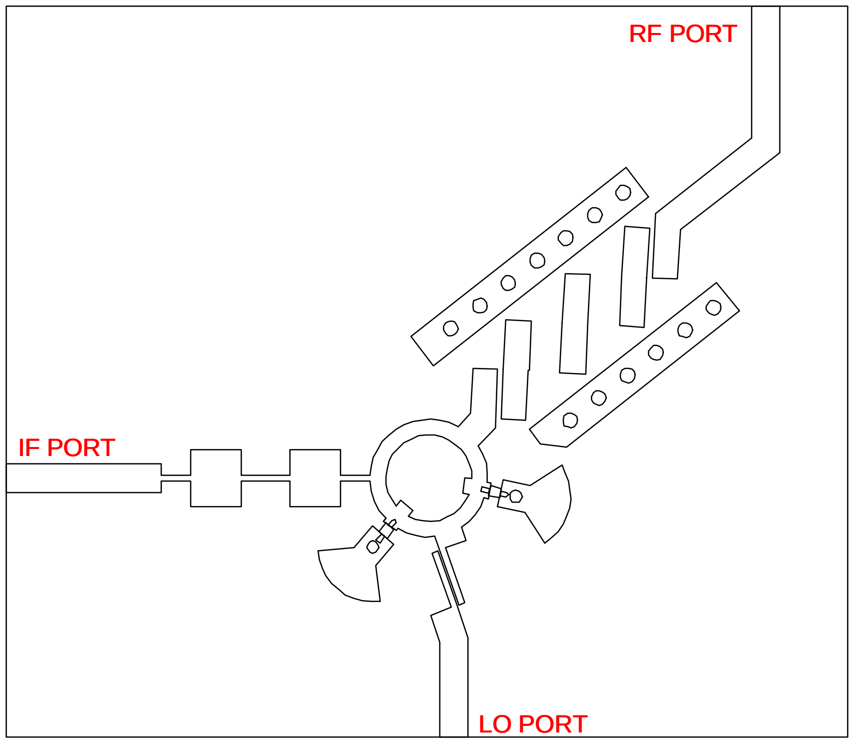

Fig. 1 Rat-race mixer

Eagleware's Submitted Results

Microwave Engineering Europe
CAD Benchmark

Simulation Strategy

Using the GENESYS suite of design software, Eagleware separated the analysis into several stages. First, circuit modeling was used for the entire design to understand the basic design intent and performance. Then the circuit was split into four sections, each being analyzed in depth using EM and circuit tools. Finally, the ring mixer, IF filter, and LO filter were combined, and EM-circuit co-simulation was used to analyze the complete design. For this final portion, the filters were modeled using already-calculated S-parameters to increase speed.

Circuit Modeling

As an initial step, the overall circuit was modeled using circuit models. The four sections of the design, the three filters and the ring mixer, were placed in separate subcircuits (see figure 1). All designs were simulated using built-in GENESYS models, including the Agilent diode model that was selected from the nonlinear device library.

Before any simulation was run, each design was laid out using the built-in layout capability. The layouts were used to verify that all dimensions were entered properly and to make sure that the input to EM simulations would match the circuit simulation exactly. The four layouts are shown in figure 2.

Each subcircuit was simulated individually. The complete circuit simulation results are shown later together with the EM simulations. At this point of the analysis, we recognized one challenge in the design: the RF filter. It has a very narrow bandwidth and performance of the overall mixer will be highly dependent upon manufacturing variations in dielectric constant and etching. Figure 8 shows the effect of a 1% variation in dielectric constant and in etching. These small variations will shift the filter sufficiently to miss the 37 GHz RF input signal. Because of these sensitivities, it was clear that EM simulation must be highly accurate to ensure that the proper bandwidth and center frequency were determined.

Once the individual pieces of the circuit had been analyzed, the overall mixer was compiled into a top-level schematic shown in figure 3. For clarity, symbols for each element were quickly created using the built-in symbol editor. S-parameters of the entire assembly were then simulated. For the initial simulation, the diodes were included in their off state. However, it was clear that the input impedance to the mixer should be affected by the LO drive. To explore this effect, the RF input impedance was calculated under large signal drive conditions. Figure 10 has three traces: 1) a 36.5-37.5 GHz frequency sweep of the small signal input impedance, 2) the large signal impedance with a +12 dBm LO drive applied, and 3) the large signal impedance at 37 GHz with the LO drive swept from -20 to 14 dBm. The traces show the dramatic improvement to RF port match when the LO drives the diodes.

EM Filter Modeling

The filters were separately modeled using EM simulation. The results are shown in figures 5-8 where the circuit models are compared to the EM results. The IF filter response, shown in figure 5 shows excellent match between circuit and EM simulation. Figure 6 shows the current density of a 10 GHz signal traveling through the filter at 10 GHz, about ½ of the lowpass bandwidth.

The LO filter response is shown in figure 7. Because of the narrow spacing of the lines relative to the metal thickness, two EM simulations were run. The first analysis assumed infinitely thin metal; the second uses the built-in thick metal analysis of the GENESYS EMPOWER simulator. While a minor effect can be seen on the filter response, particularly over 100GHz, the impact of the thickness is minor.

The RF filter was analyzed very carefully because of the sensitivities discussed above, and the results are shown in figure 8. Agreement to about 1% is seen between the circuit and EM simulator. To get high accuracy with EM analysis, it is critical to properly model the length of the resonators. EMPOWER was configured to include more cells along the length of the resonator than the width. Using Richardson extrapolation, possible with EMPOWER due to the monotonic convergence of its underlying Method of Lines approach, cell size was accurately set to make sure that a high level of accuracy was met.

Due to the narrow bandwidth of the filter, the 37 GHz signal is just in the passband of the filter predicted by EM analysis. Depending on manufacturing accuracies, the insertion loss of the filter could have a significant impact on the performance of the mixer at a 37 GHz.

EM-Nonlinear Co-Simulation of the Ring Mixer

EM-circuit co-simulation was used to model the complete mixer. Because the diodes are embedded in the circuit, with important distributed elements on both sides of the diodes, co-simulation is an ideal tool for analysis. To co-simulate, the target design for the harmonic balance simulation is the EM simulation. One key advantage of co-simulation is that the EM simulation is only run at the frequencies required by harmonic balance. Since the frequencies are unevenly spread across a wide spectrum, precise frequency selection improves the solution time. An example spectrum is shown in figure 10. Plots of conversion loss, port-to-port isolation, compression, and spectrums are also included. Worthy of note is the spectral plots where 3 RF tones are mixed, requiring a 4-tone analysis.

Optimization

As the circuit model was so close to the EM results, circuit optimization was setup, allowing orders-of-magnitude improvements in optimization times over an EM-based optimization. Alternatively, GENESYS could have been configured to optimize using

EM runs on each optimization step. While conceptually attractive, the long time required to optimize EM-nonlinear co-simulation is not practical for real-world design.

Schematics and Layouts

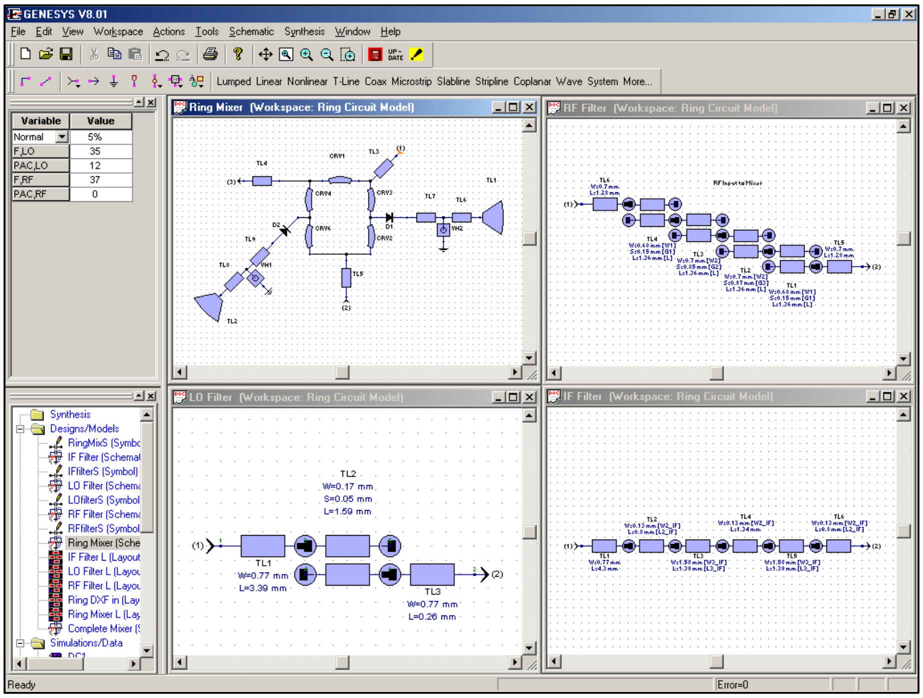

Figure 1: Schematics used in circuit simulations

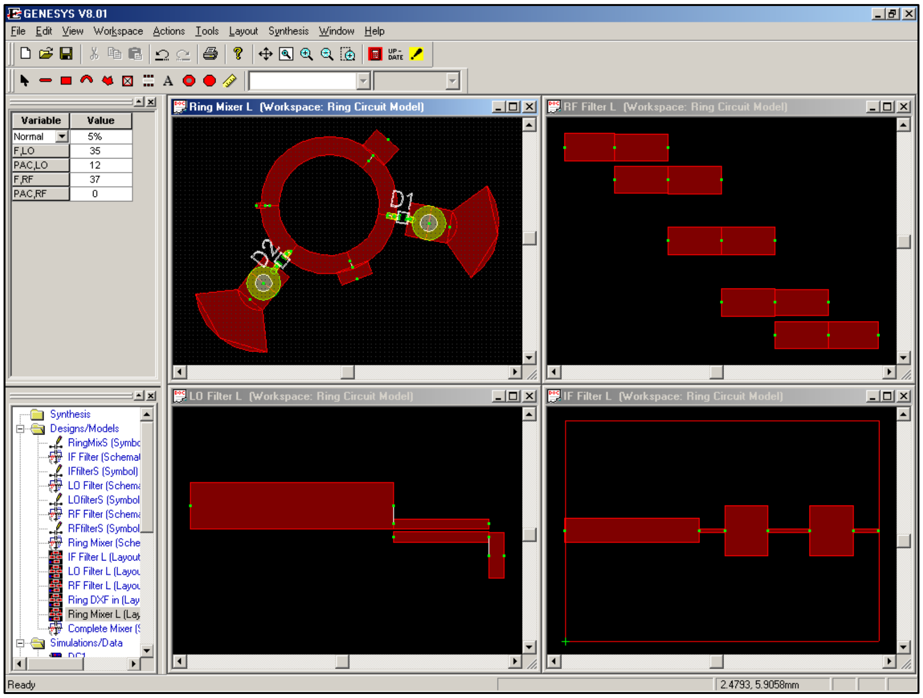

Figure 2: Layouts Generated by Circuit Simulation Models

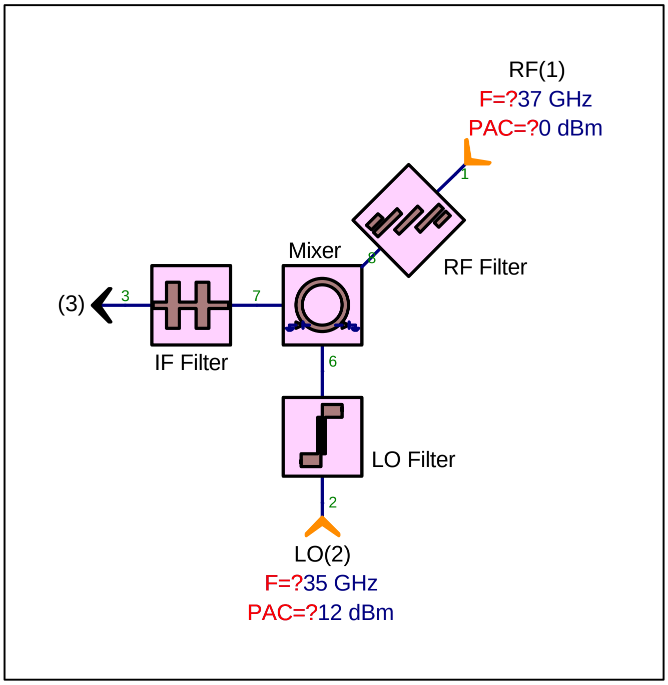

Figure 3: Schematic of Combined Subcircuits

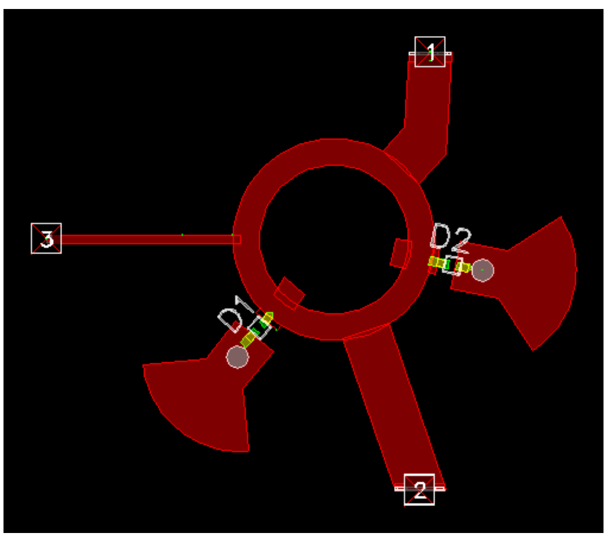

Figure 4: Layout of Hybrid Ring used in EM simulation

Simulation Results

S-Parameters

IF Filter

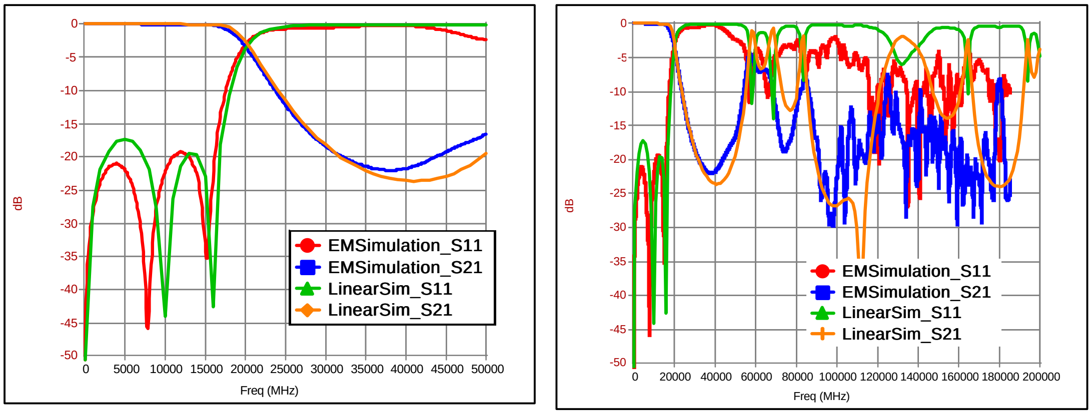

Figure 5: IF Filter Responses

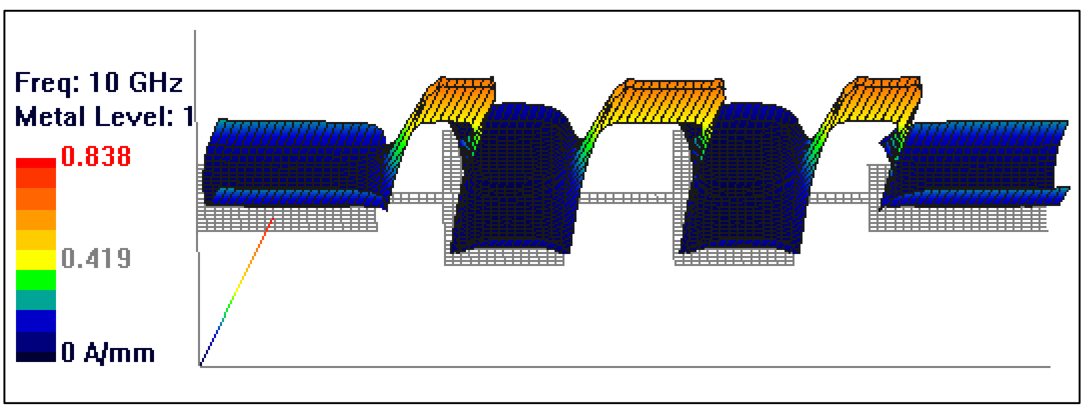

Figure 6: Current Viewer Showing Current at 10GHz through IF Filter

LO Filter

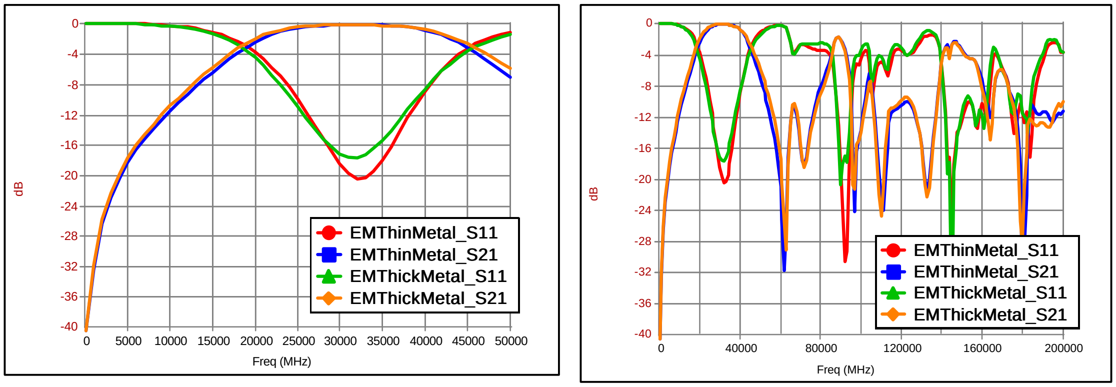

Figure 7: LO Filter Responses

RF Filter

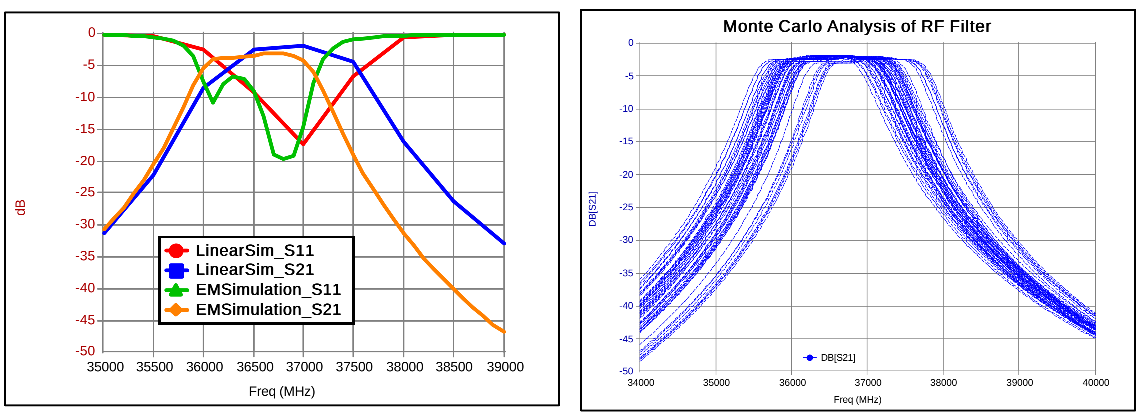

Figure 8: RF Filter Response and Monte Carlo Analysis

Hybrid Ring EM-Circuit Co-Simulation

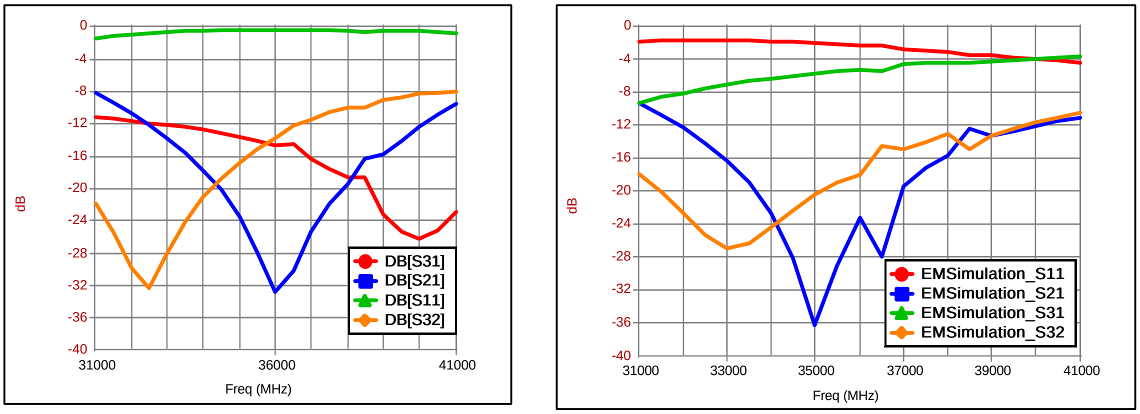

Figure 9: Hybrid Ring Response without Diodes (left) and with Diodes (right)

Composite Circuit

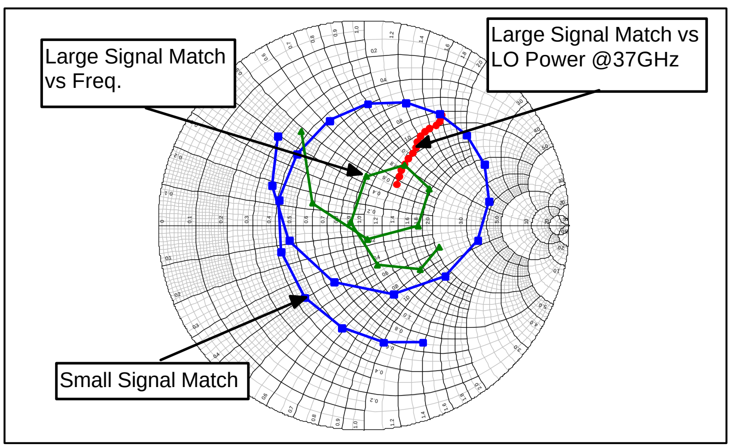

Figure 10: RF Input Impedance vs LO Drive

Conversion Loss

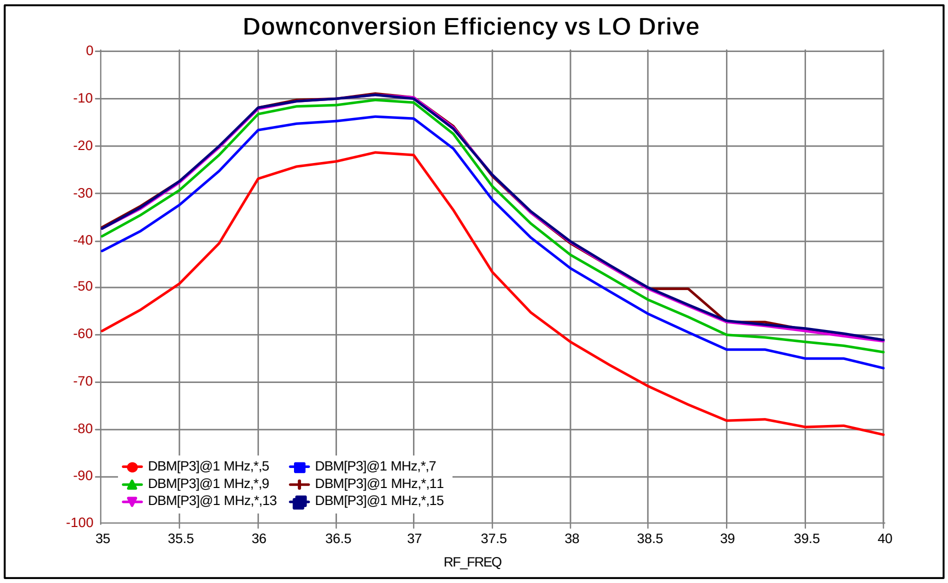

Figure 11: Downconversion vs. LO Drive Level

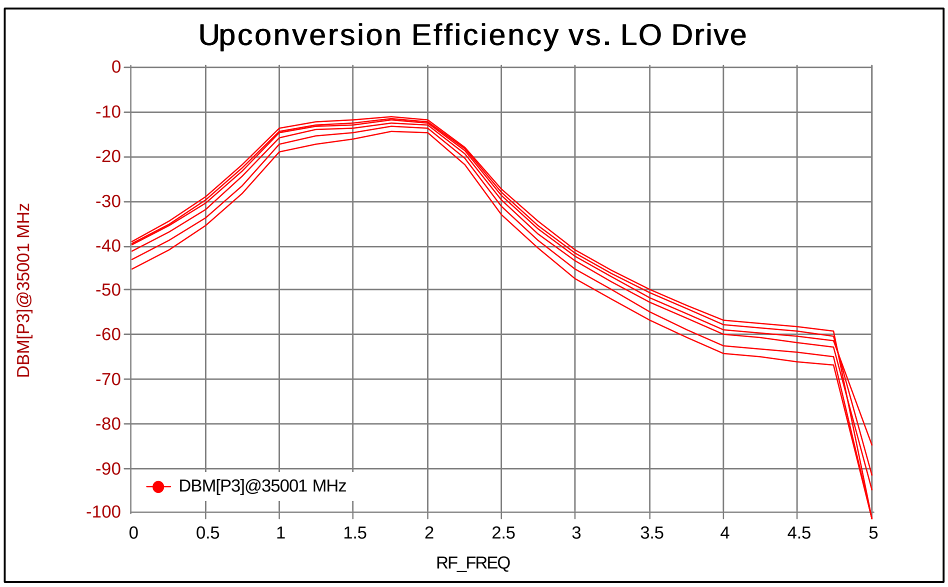

Figure 12: Upconversion Efficiency vs. LO Drive

VSWR

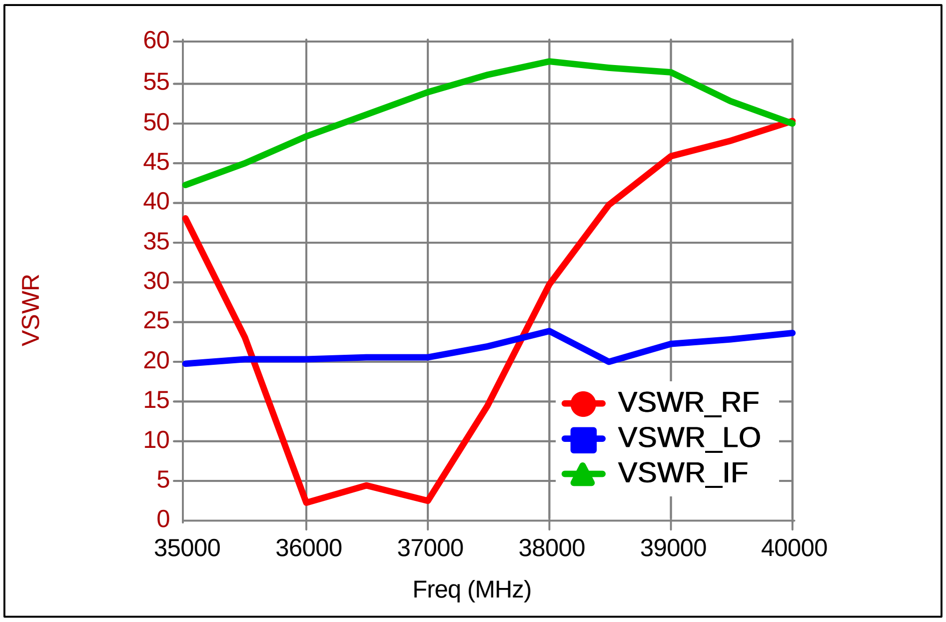

Figure 13: Small-signal VSWR of Complete Circuit

Port-to-Port Isolation

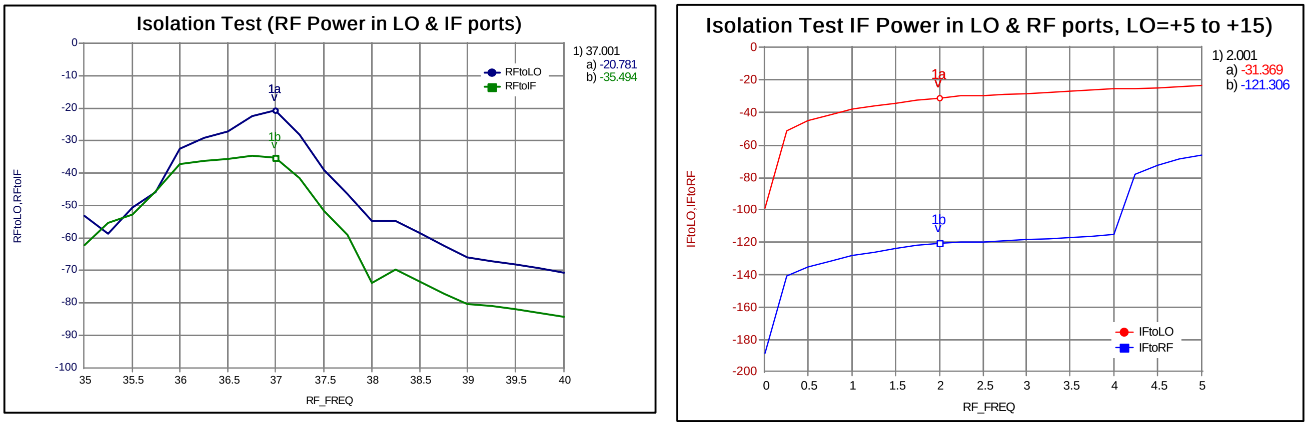

Figure 14: Downconverter Port-to-Port Isolation

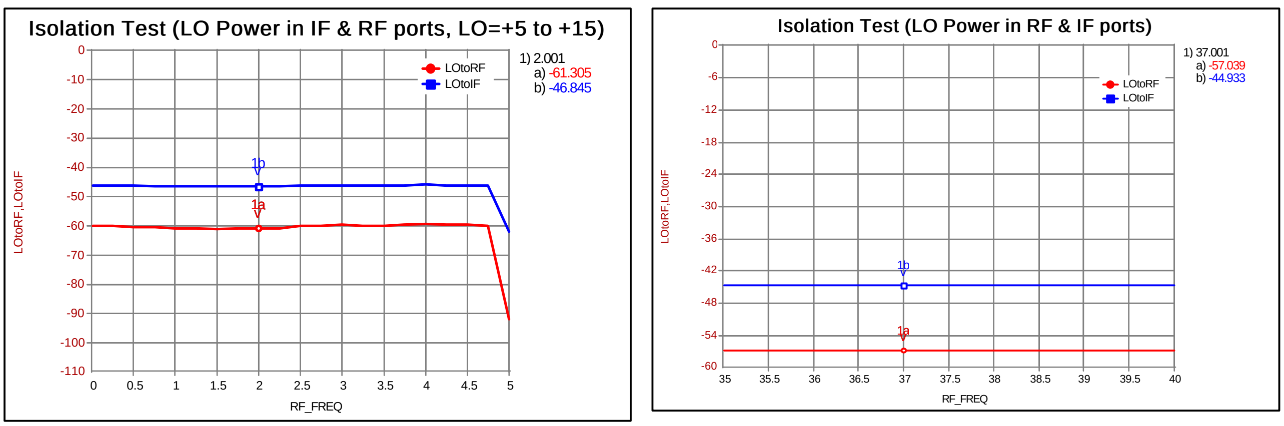

Figure 15: Upconverter Port-to-Port Isolation

Compression

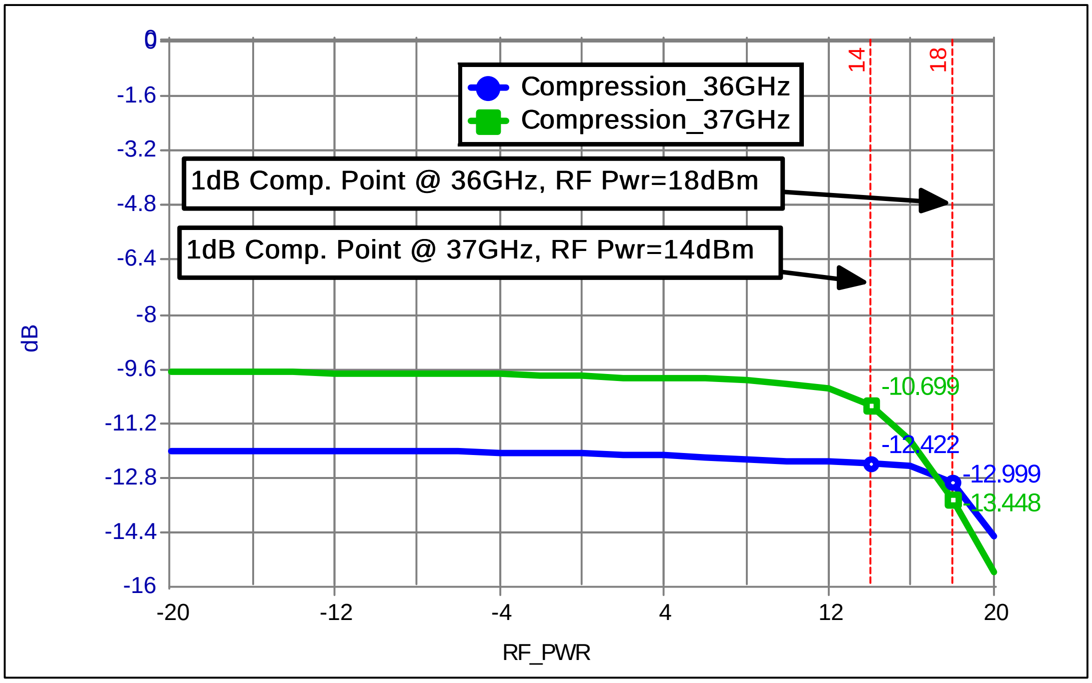

Figure 15: Downconverter Compression

Spectral Data

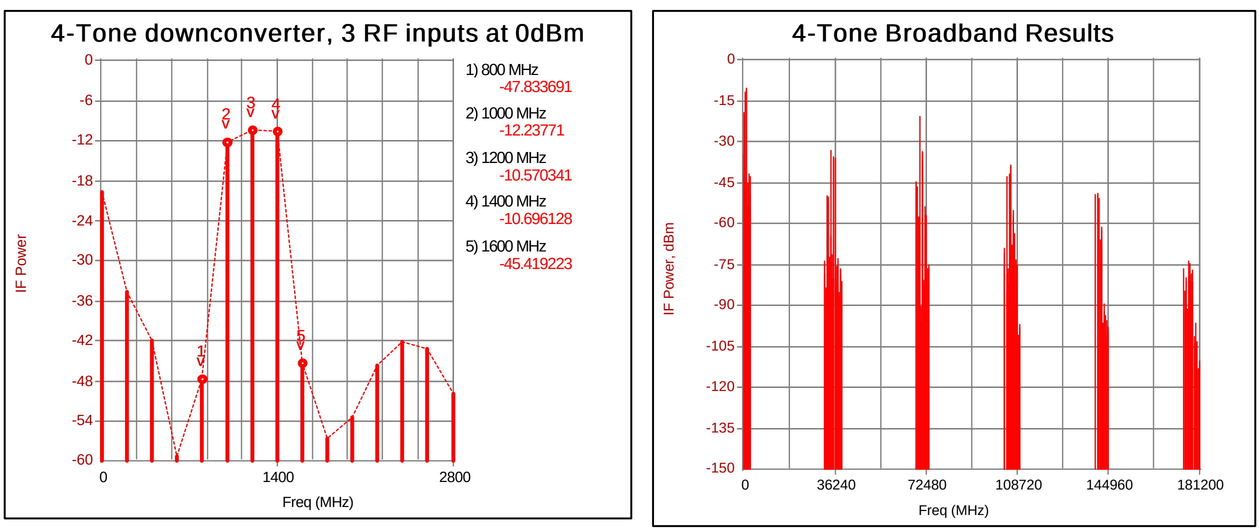

Figure 16: Multitone Spectral Outputs

Mixer Spurious Responses

Spurious responses for various power levels of the local oscillator and RF inputs were produced and are summarized by the following tables. Frequencies above 185 GHz and signals more than 100 dBc are not included. The numbers in the tables below are dBc relative to the IF of the mixer.

Frequency Table:

Harmonic LO Order (M)

RF Order Harmonic (N)

	0	1	2	3	4	5
0	0	35	70	105	140	175
1	37	[2, 72]	[33, 107]	[68, 142]	[103, 177]	[138, ----]
2	74	[39, 109]	[4, 144]	[31, 179]	[66, ----]	[101, ----]
3	111	[76, 146]	[41, 181]	[6, ----]	[29, ----]	[64, ----]
4	148	[113, 183]	[78, ----]	[43, ----]	[8, ----]	[27, ----]
5	185	[150, ----]	[115, ----]	[80, ----]	[45, ----]	[10, ----]

Table entries: [f_Δ, f_Σ] where: $f_\Delta = N * f_{RF} - M * f_{LO}$ (difference frequency)
$f_\Sigma = N * f_{RF} + M * f_{LO}$ (sum frequency)

Condition No. 1: (P_{RF} = -20 dBm)

Harmonic LO Order (M)

	0	1	2	3	4	5
0	---	3.29	(8.56)	12.8	18.7	45.3
1	25.9	0, 24.9	37.1, 26.2	32.2, 46.4	47.9, 60.2	54.6, ----
2	75.3	87.0, 78.8	53.0, 84.0	76.8, 84.2	77.0, ----	87.6, ----
3	>99	>99, >99	>99, >99	77.0, ----	>99, ----	>99, ----
4	>99	>99, >99	>99, ----	>99, ----	>99, ----	>99, ----
5	>99	>99, ----	>99, ----	>99, ----	>99, ----	>99, ----

Condition No. 2: (P_{RF} = 0 dBm)

Harmonic LO Order (M)

RF Order Harmonic (N)

	0	1	2	3	4	5
0	---	23.5	11.5	33.0	39.2	65.7
1	25.8	0, 24.7	36.8, 26.0	32.3, 46.3	48.1, 60.8	54.5
2	54.7	65.6, 58.5	31.6, 63.6	56.4, 64.4	55.0, ----	67.4, ----
3	82.3	71.1, 79.6	70.9, 83.1	38.1, ----	60.7, ----	64.4, ----
4	94.0	>99, >99	92.8, ----	>99, ----	62.5, ----	97.5, ----
5	>99	>99, ----	>99, ----	96.4, ----	91.2, ----	64.6, ----

Condition No. 3: (P_{RF} = +5 dBm)

Harmonic LO Order (M)

RF Order Harmonic (N)

	0	1	2	3	4	5
0	---	29.0	16.8	38.6	45.3	71.8
1	25.9	0, 24.8	36.7, 26.2	32.6, 46.8	48.7, 61.6	55.7, ----
2	49.8	63.7, 53.3	32.0, 59.3	54.4, 57.7	56.2, ----	63.4, ----
3	71.7	68.0, 69.4	68.8, 71.2	34.1, ----	56.4, ----	61.0, ----
4	81.4	92.4, ----	74.9, ----	76.6, ----	43.7, ----	67.6, ----
5	>99	>99, ----	96.7, ----	87.4, ----	84.2, ----	59.7, ----

Setup Information

EM Simulation

Rogers Duroid 5880 substrate was uses. Open covers were used on the IF and LO filters. The RF filter had a cover placed 2 mm above the metal layer.

Circuit	X cells	Y cells	RAM	Time/freq
IF Filter	0.10 mm	0.043 mm	28.8 MB	3 min 42 sec
LO Filter	0.10 mm	0.025 mm	0.5 MB	0 min 27 sec
RF Filter	0.06 mm	0.044 mm	182.7 MB	20 min 18 sec
Ring	0.10 mm	0.100 mm	64.4 MB	4 min 53 sec

Harmonic Balance Simulation

Harmonic balance simulations used 5 harmonics on both the LO and the RF, with a maximum mixing order of 5. Experiments were done using up to 16 harmonics with minimal changes in performance except at the highest-order products. If higher order products (above 5) are important, additional tones should be included in the simulation. Simulation times depend on previous simulations and other factors. First-run times are 5-10 seconds, sweeping or tuning is typically less than 1 second per point.

Co-Simulation

Co-simulation is automatic in GENESYS. Once the harmonic balance and EM simulations are configured, the simulation times are the sum of the two simulation times.

Hardware Information

The simulation was performed on a Pentium 4 system at 1.3GHz with 1 GB RDRAM and 1 CPU installed. The operating system was Windows 2000 Professional Edition.

Software Information

The software version used was Eagleware GENESYS V8.01. Specific modules used were GENESYS Basic (schematic capture, layout, and linear simulation), EMPOWER (planar EM simulation), and HARBEC (nonlinear circuit simulation).

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