



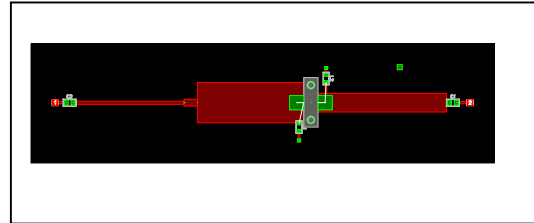
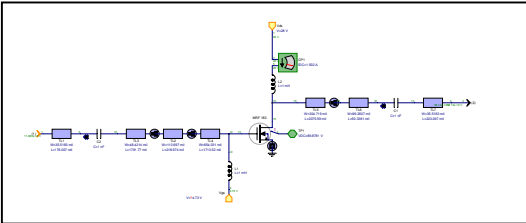
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To Design Power Amplifiers using Genesys

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Using GENESYS to Design Power Amplifiers



Abstract

The robust equation editing tools and large signal parameters available in GENESYS are illustrated in the following application where large signal S-parameters and load pull data are generated using high accuracy LDMOS models.

Introduction

In the daily world of power amplifier design the engineer is faced with the sometimes daunting task of evaluating and selecting devices for use in his project. In years past designers relied on linear data or extrapolation techniques to predict output power as well as source and load match. While it is tempting to try using large signal S-parameters for output matching the physical device's equivalent circuit is not time invariant and therefore linear analysis and all that this entails is not a valid choice for choosing the optimum match. Today more accurate methods are available in determining the optimum load given a specific bias, source impedance, and drive level. The predominate technique for determining these optimum values is "Load Pull" analysis. This method of analysis measures the output power as the load or reflection coefficient presented to the device under test (DUT) is varied. The method of varying the load often consists of a double or triple stub mechanical tuner.

Advances in recent years by several companies have established automated systems to help reduce the tedium and error in measuring the

large signal parameters. The tuners employed are often tuned under program control and have been accurately characterized for their reflection coefficient and insertion loss verses position. If accurate models are available characterizing the device for optimum performance under large signal conditions can be accomplished through simulation techniques. This note presents a step-by-step approach using the built-in functionality of GENESYS to evaluate and design a power amplifier, thus eliminating the need for costly test equipment and measurement software.

Design Procedure

We first identify a device that promises to have the gain, output power, efficiency and distortion characteristics that meet our amplifier specifications. For this application we have a stated requirement for a gain of 14db at 800 MHz and an output power of 24 watts. A device from GENESYS' supplied models is Motorola's MRF-183 LDMOS FET. The data sheet specifications for the MRF-183 indicate that it can meet our applications requirements. Having selected a suitable device, the next step is to determine it's IV characteristics so that the correct bias can be applied for the gain and power requirements.

Figure 1 illustrates a setup in SCHEMAX for generating the IV curves. Note that for this particular FET the chip temperature is available directly from a forth terminal. This is helpful for designing temperature dependant bias networks that keep the device operating in a safe zone.

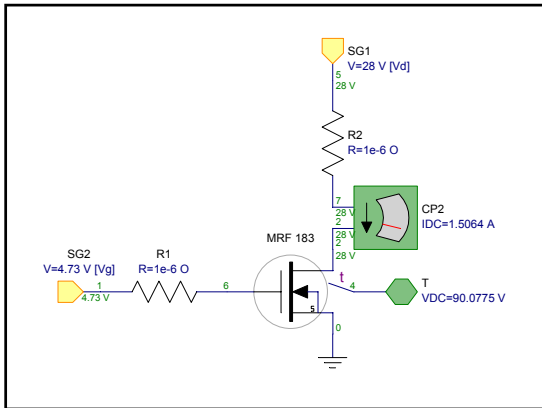


Figure 1

Using the feature in GENESYS for nested parameter sweeps, the drain to source and gate voltage is swept to generate the devices IV characteristics. Note in this example we have also presented the chip temperature as a function of bias. See Figures 2a and 2b.

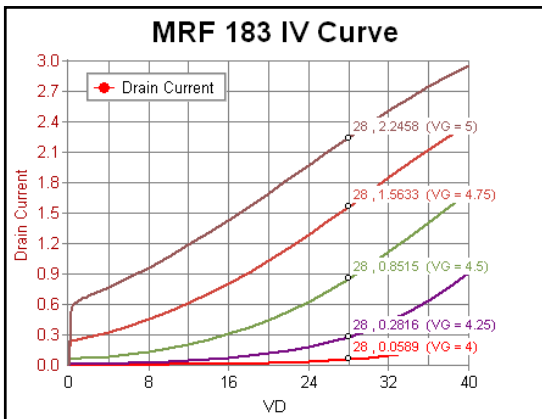


Figure 2a

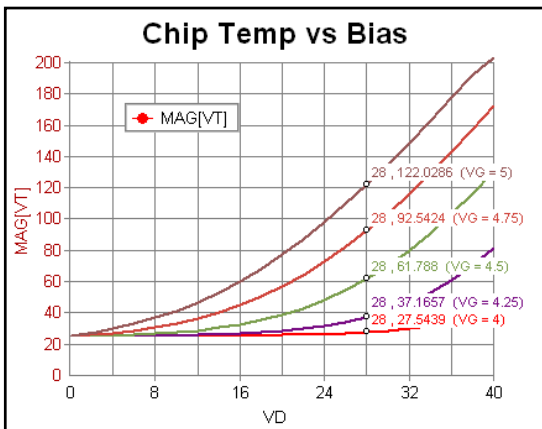


Figure 2b

We select a bias point that provides the optimum operating point to achieve the gain and output power that we desire. In our example we have chosen a VDS of 28V coupled with a drain current of approximately 1 amp. In the next step we determine the gain and input matching information when our device is driven under large signal conditions. GENESYS provides built-in functions for extracting the large signal S-parameters. These functions extract the parameters by measuring the forward and reverse signal flow at the fundamental frequencies. Having these functions built-in relieves the designer from coding additional equations to extract this data independently.

Another benefit of using simulation techniques to derive the large signal data is the ability to specify complex termination impedances at the ports. When using 50 ohm test sets the accuracy of physical measurement is linked to the difference between the devices impedance level and 50 ohms. The uncertainty and ultimate accuracy of a device of 1 ohm measured in a 50 ohm system is worst than when measured in a 5 or 10 ohm impedance system. That said, the accuracy with simulation is only as good as our model device. Figures 3, 4 and 5 illustrate the schematic setup and measurements.

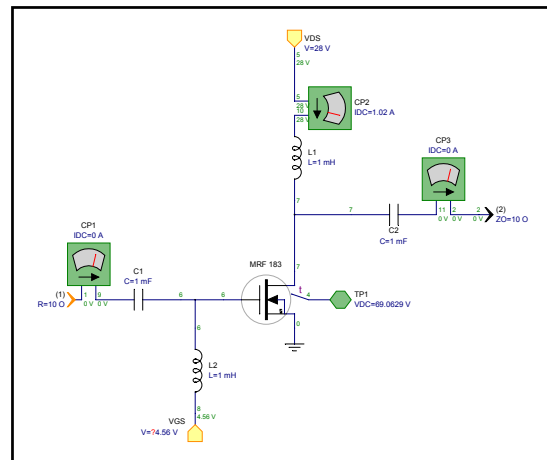


Figure 3

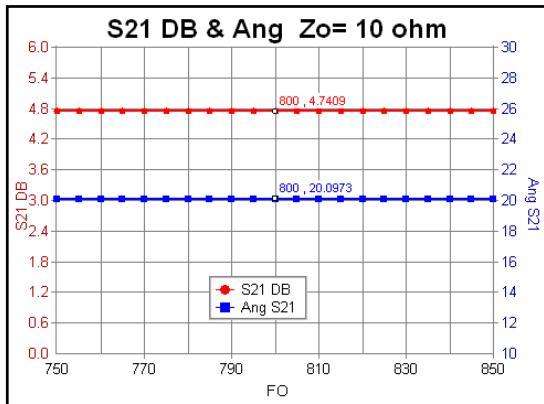


Figure 4

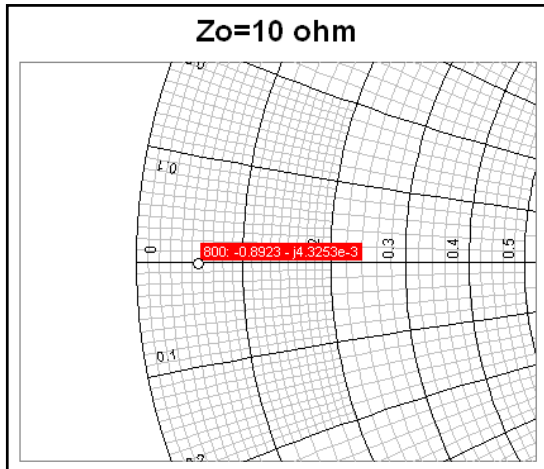


Figure 5

Having measured the large signal S11 and S21 through simulation we can now determine the optimum load presented to our device to provide us with the required output power. In our example, if we assume unilateral gain—which is most common for power amplifier design—the gain contribution from S11, S22, and S21 total approximately 13.6 db. During the process of optimizing our design we may choose to increase bias or drain voltage to bring us closer to our stated goal of 14 db.

Note that over the chosen frequency range our device shows little variation in its parameters. This also seems to be consistent with many power devices on the market.

Our final task in characterization is the dependency on output power versus load. We use the technique of load pull; however our

measurement system is the GENESYS simulator instead of a physical system of tuners, network analyzer, power supply, and measurement software. Figure 6 illustrates the schematic components used to generate a data set consisting of the power delivered to the load versus the complex load expressed as a sweep of reflection coefficient values.

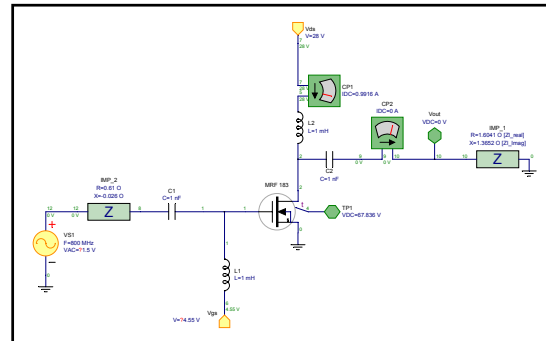


Figure 6

Note that the source impedance reflects the value determined in our evaluation of the large signal S-parameters made previously. We therefore measure the power output under the condition that the input is closely matched. We have chosen to use a special impedance element in GENESYS that allows us to specify any arbitrary value. In setting up the simulation we set the source voltage to reflect an available power of 1 watt or 30 dBm when conjugately matched to the source impedance. This can be calculated as $V_{pk} = \sqrt{P_{in} \cdot 8 \cdot \text{Re}(Z)}$. Given an input impedance whose real part is 0.6 ohms with 0.5 watt available under matched conditions, this equates to a peak voltage of 1.55 peak. Using the GENESYS capability to perform nested sweeps with multiple variables we then run a simulation that varies the load impedance over the limits specified in our parameter sweep setup. In our example we have varied the real and imaginary reflection coefficients over the range of -0.9 to +0.9. The actual formulation for setting up the measurement of power absorbed by the load and the calculation of load impedance given the swept reflection coefficient is presented in the downloadable example. Another useful function in GENESYS is the “Contour” function. This function plots 2D data on a Smith chart. This function is available to view power contours from measured data that is imported into GENESYS or as in our example to view power contours which

have been generated through simulation. In our example we have plotted power delivered to the real part of our load versus reflection coefficient. The contour function uses a “Thin Plate Spline” to generate the resulting curves. Figure 7 illustrates contours of constant power delivered to the load as a function of reflection coefficient.

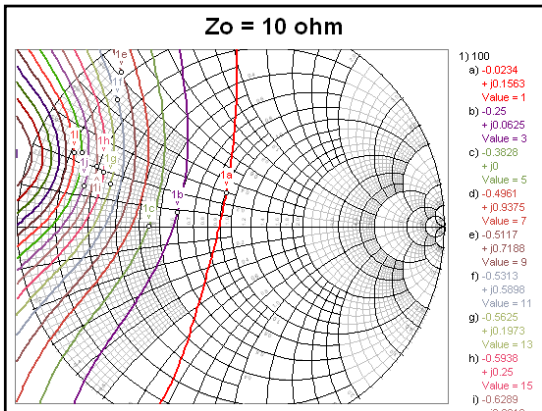


Figure 7

The contour function enables us to specify end limits for projected power as well as the step value and smoothing. The data shows that many choices for load impedance exist for each output power level. Since we have a choice of loads that will provide us with the desired output power we may choose a topology that is most convenient for minimizing production costs. Having now arrived at the point where we know what impedance or reflection coefficients will provide the desired gain and output power, we are ready to synthesize the matching structure that will convert a 50 ohm termination to the desired impedance.

GENESYS’ synthesis modules greatly reduce the effort in developing these matching structures with an embedded synthesis tool named MATCH. MATCH provides the foundation for matching between complex impedances either specified explicitly through R, L and C components, a stated impedance/admittance or from a measured data set of S, Y, or Z parameters. The resulting matching structure may be lumped, distributed or be a combination of each. In our application we used a distributed matching structure of cascaded line segments.

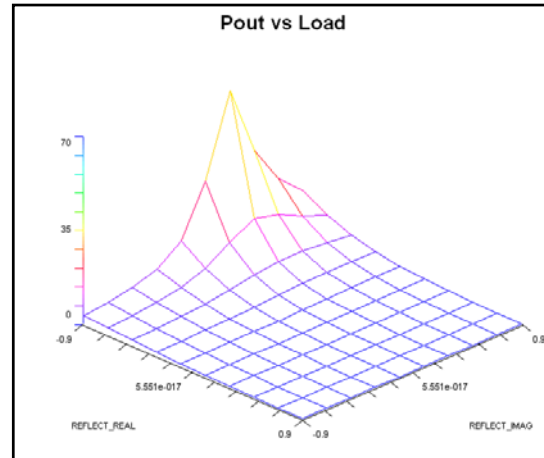


Figure 8

GENESYS offers a variety of methods to output load pull data beside the contour function. Table data can be generated as well as three-dimensional views of output power versus load see figure 8. Figure 9 shows the bi-lateral match generated and optimized with MATCH. Note that S11 is reference to 2 ohms whereas S22 is referenced to 50 ohm.

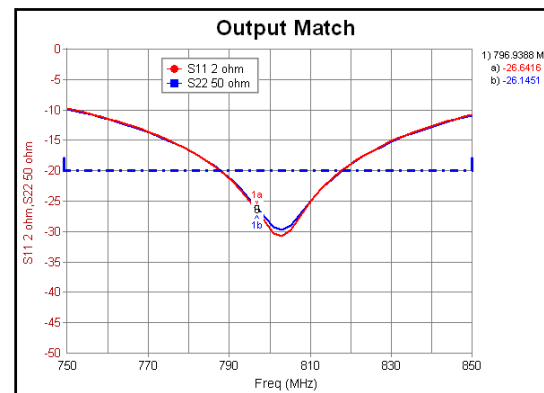


Figure 9

Figure 10 is the completed network realized in microstrip. Note also that once a topology is determined the resulting network may be realized in over 12 different physical configurations including stripline, coaxial, etc. through the use of Advanced T/LINE.

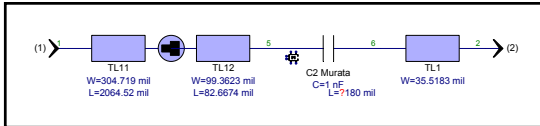


Figure 10

Using MATCH again to convert 50 ohm to approximately 0.6 ohms(real) for the input of our device we complete the design. The remaining task is to then simulate the completed amplifier and evaluate critical power amplifier parameters such as gain, power out, TOI, and compression point. The final schematic along with spectral information and output voltage information is illustrated in figures 11 through 14.

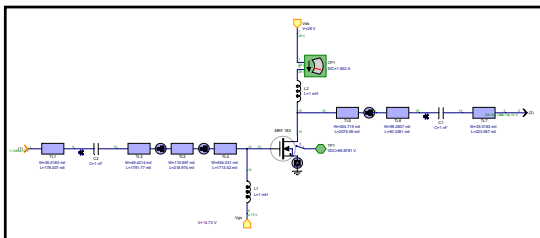


Figure 11

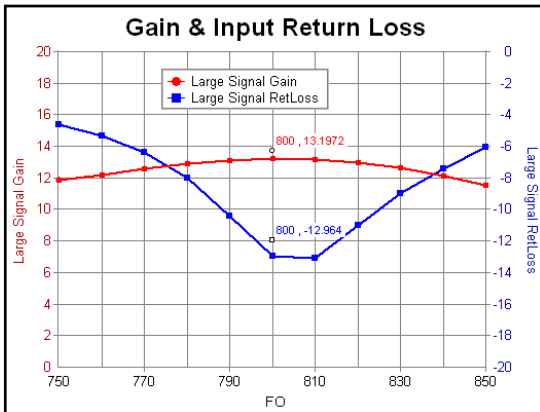


Figure 12

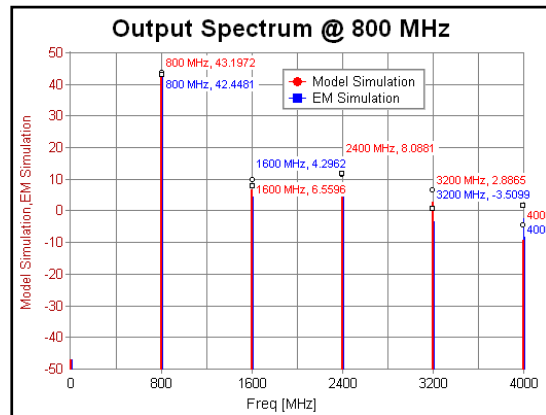


Figure 13

In figure 13 an additional analysis using GENESYS' co-simulation capability improves the accuracy of our data and enables us to view the effect of EM simulated circuit and the effects of copper losses, coupling and radiation effects.

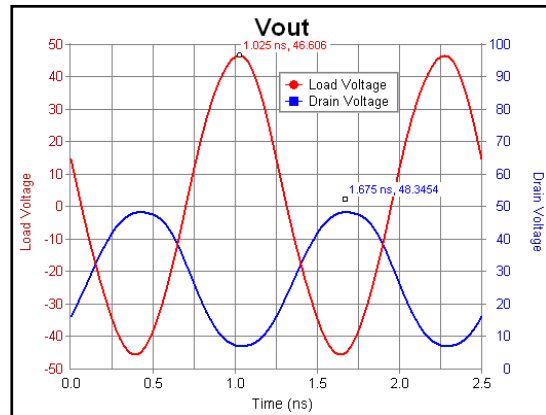


Figure 14

.In figure 15 we show the final layout, which also consists of a user define footprint of the MRF-183 LDMOS FET. The layout represents the final structure where the EM co-simulation was performed.

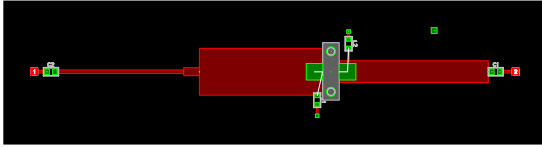


Figure 15

As noted earlier gain and output power is only two of several requirements that need to be verified before a prototype is ready to be built. Compression point and TOI are both quality measurements that are often performed on the bench with test equipment to verify overall dynamic range and linearity. GENESYS again provides the tools to verify performance prior to expending money on prototypes.

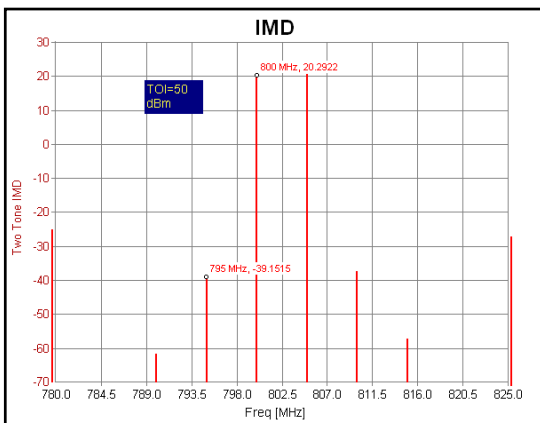


Figure 16

Two input signals of 5 dBm separated by 5 MHz are simulated via GENESYS' harmonic balance engine HARBEC to produce a third order intercept of 50 dBm.

Finally, the dynamic range of our design is presented by sweeping the input power and plotting the gain versus input power. Note that the 1db compression point occurs at approximately +26 dBm input power. Being able to accurately predict the performance of our design prior to cutting copper enables the designer to try alternate configurations, and bias scenarios, eliminating costly board turns.

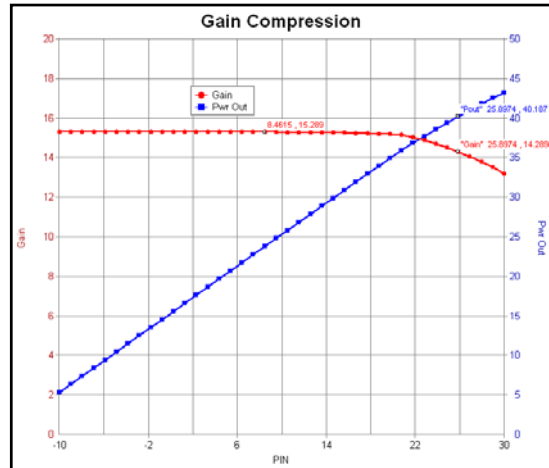


Figure 17

Conclusion

We have illustrated a systematic design flow for a medium power amplifier using the extensive capabilities available in the GENESYS suite of tools. From linear analysis, large signal S-parameters, load pull, synthesis, and EM co-simulation, Eagleware provides a platform of RF and Microwave analysis and simulation tools that reduce manufacturing and development costs.

Additional information on power amplifier design techniques can be found in RF POWER AMPLIFIERS by Mihai Albulet available through Noble publishing.

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