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RF SiP Design Verification Flow with Quadruple LO Down Converter SiP

By HeeSoo Lee and Dean Nicholson
Agilent Technologies

This article outlines the design flow used for a System-in-Package component, using multiple die integrated into a single packaged device

The wireless industry trend toward higher integration and RF component miniaturization has been driving ongoing technology innovations, especially for substrate, interconnect, and packaging technologies. RF System-in-Package (RF SiP) is one of those leading technology innovations. RF SiP is usually a sub-system unit, and it typically consists of multiple dies with or without passive components generally constructed from embedded passives (EP) and SMT technology. However some passive circuits can also be constructed from integrated passive device (IPD) technology, especially when space requirements are tight or a higher Q is needed.

From a historical perspective, RF SiP is not a totally new technology because Multi-Chip Modules (MCM) and RF modules have been on the market for years and are considered an RF SiP technology. RF SiP typically provides better integration flexibility, faster time to market, and lower product development costs than System-on-Chip (SoC) by mixing and matching existing designs (ICs) and using best-in-class technologies. Nevertheless there are still ongoing debates about the strengths and future of SiP versus SoC. It is clear, however, that there is a very strong market demand for RF SiP. It is perhaps too early to predict which technology will dominate the market in the future, but it is fair to say that SiP will be a hot technology and market over the next several years.

This article presents an RF SiP design verification flow with a quadrupled LO down converter RF SiP. Agilent Technologies' ADS (Advanced Design System) and EMDS (Electromagnetic Design System) are used to design the SiP. ADS includes circuit/system simulators and a layout package for RFICs, MMICs, RF boards, SI (Signal Integrity), RF SiP, and RF module applications. EMDS is 3-D, full-wave electromagnetic simulation software.

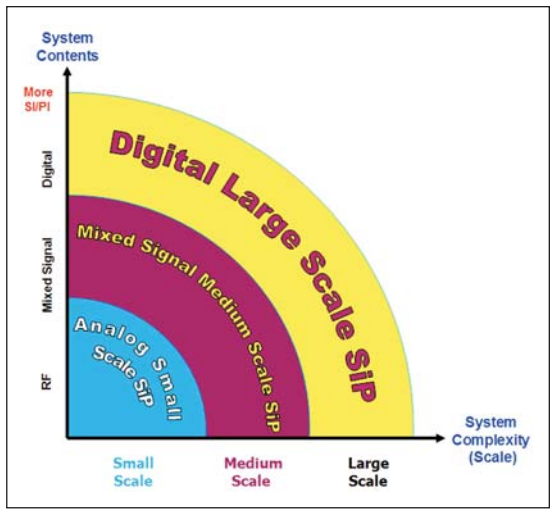

Figure 1 · SiP market segments.

SiP Market Segmentation

The SiP market can be divided into three market segments with system content and complexity (or scale), as shown in Figure 1. From the system content standpoint, there are analog, mixed signal, and digital markets, and from the scale standpoint there are small-scale, medium-scale, and finally large-scale segments. The three market segmentations of SiP are therefore analog small-scale SiP, mixed signal medium-scale SiP, and digital

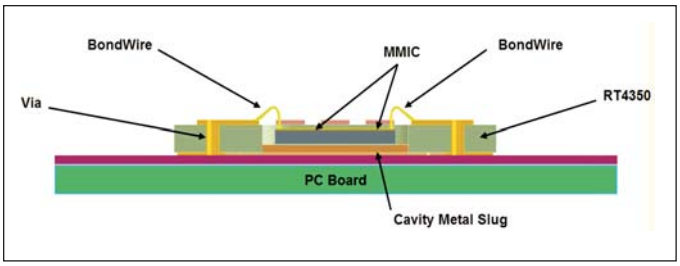

Figure 2 · Cross-sectional view of TOPS.

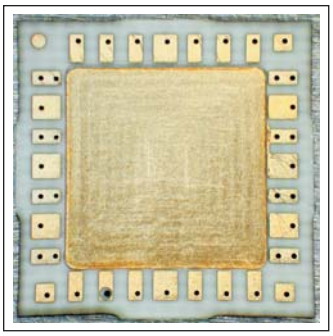

Figure 3 · Top view of TOPS.

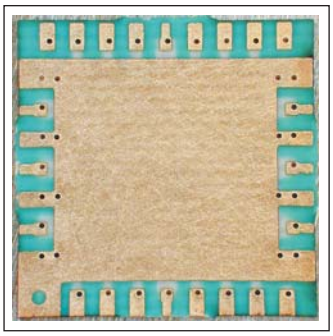

Figure 4 · Bottom view of TOPS.

large-scale SiP markets. RF SiP normally spans from analog small-scale to mixed signal medium-scale market segments. The typical products and applications for each market segment are PAM (power amplifier module), FEM (Front End Module), and ASM (Antenna Switch Module) for analog small-scale SiP; transceiver module and radio module for mixed signal medium-scale SiP; and lastly MCP (Multi Chip Packaging) type of applications for digital large-scale SiP. For the discussion in this article, we will only focus on RF SiP technology.

RF SiP Design Challenges

Although there are many design challenges in RF SiP, these challenges can be grouped under three big categories. The first one is system level design challenges, where designers must create the best performing system architecture and optimize not only the system performance but also the development and manufacturing costs. The second category is package/interconnect design challenges, where 3-D package, substrate stackup, and die-to-die/die-to-package interconnect designs must be well understood. The last category is modeling challenges, where passive/active device models, vendor component libraries, statistical models, and behavior models must be accurately developed to shorten the RF SiP design cycle. There are many commercially available design tools in the market that help designers to address these issues. Agilent Technologies offers a complete set of design tools to address these design challenges for system/circuit level designs, package/interconnect designs, and modeling solutions.

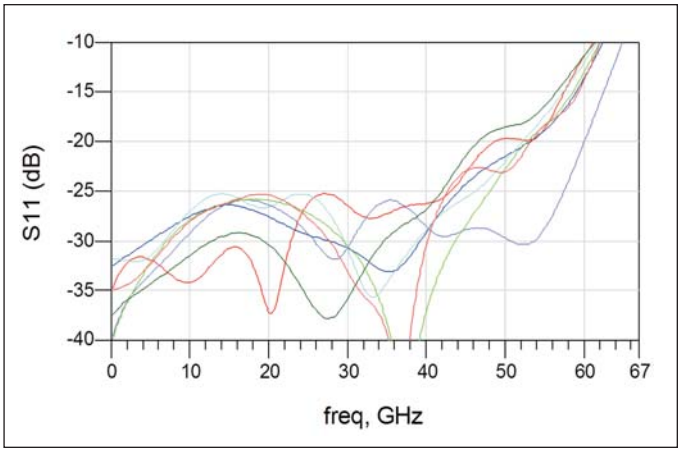

Figure 5 · Measured S_{11} performance of TOPS transition (seven samples).

TOPS Package

TOPS (The Other Packaging System) is a package designed for a surface mount technology, and is suitable for packaging a line of ICs of up to 60 GHz without the complexity of wafer probe calibrations on the mixed transmission media of GCPW on PCB and microstrip on ceramic or GaAs. The SiP design example in this article uses this TOPS package. A cross-section view of the package is shown in Figure 2. It is similar to conventional QFN packages but it has much higher frequency performance characteristic. The package has a relatively small form factor, which is about 10 × 10 mm. The lid of the package is a non-hermetic air cavity with a molded liquid crystal polymer, and the substrate material is Rogers 4350 with metal backing. Figures 3 and 4 show the top and bottom side of the package respectively. The resulting TOPS package gives the best return loss performance in the DC to 60 GHz frequency range. With the optimized bondwire interconnect [1], the transition performance of the package from PCB → package trace → bondwire → 50-ohm load demonstrates better than –20 dB return loss DC to 50 GHz, and better than –15 dB return loss DC to 60 GHz [2]. The measured data of seven transition samples is shown in Figure 5.

Quadrupled LO Down-Converter RF SiP

Figure 6 shows the photo of a quadrupled LO down-converter SiP, which is similar to the one of conventional MCM type of modules. The system is basically a down-converter that converts 22~24 GHz RF input frequency to a fixed 1950-MHz intermediate frequency. However, the LO frequency is quadrupled by two multipliers. The signal paths for RF and LO are shown in Figure 7. For active

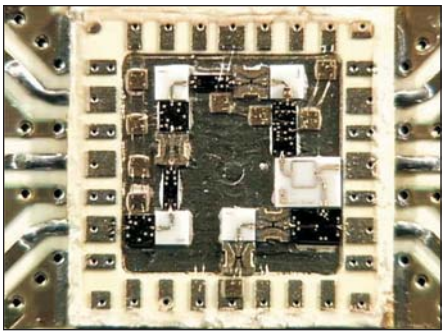

Figure 6 · Photo of the quadruple LO down converter.

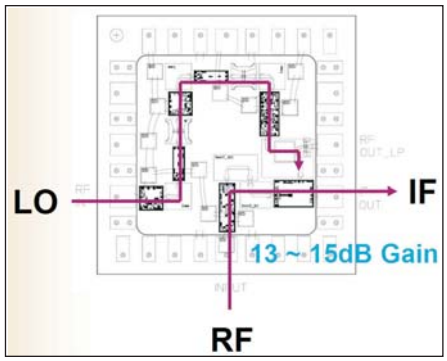

Figure 7 · Outline of signal paths within the package.

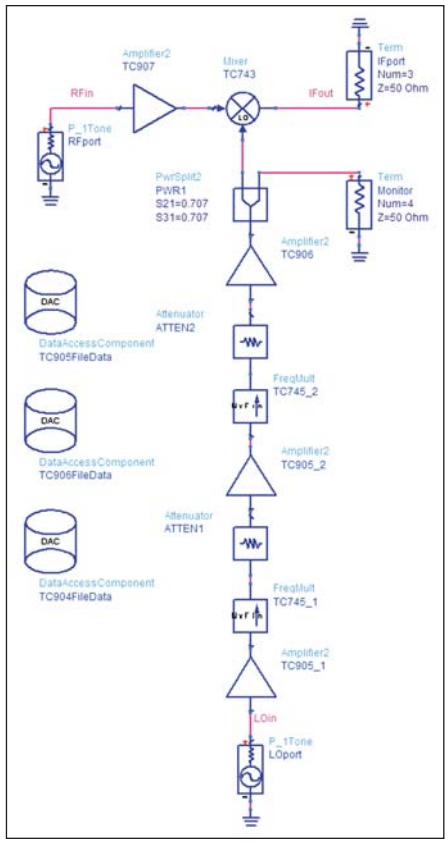

Figure 8 · ADS schematic, with DAC files.

circuits, existing MMIC chips are used, which are amplifiers, mixers, and multipliers. In addition to these active circuits, eight thin-film passive circuits on alumina substrate are specially designed to interconnect MMICs and perform necessary passive functions such as attenuation and power division. As discussed earlier, using SiP design, it was possible to design the system much faster by mixing and matching proven designs using the best-in-class technologies.

EM Simulation of Passive Structures

Most planar passive structures can be simulated effectively with Method of Moment (MoM) electromagnetic (EM) solvers. However, some passive 3-D structures require full-wave 3-D EM simulations—bondwire interconnects are perfect examples. Two popular full-wave 3-D EM simulation technologies are Finite Element Method (FEM) and Finite Difference Time Domain (FDTD). Agilent Technologies offers Momentum, a 3-D planar EM simulator for arbitrary 3-D planar passive structures. Momentum accepts arbitrary design geometries such as multi-layer structures and accurately simulates complex EM effects such as coupling and parasitics. EMDS is a 3-D FEM EM simulator used for simulating arbitrary 3-D structures based on frequency domain technique. Finally, AMDS (Antenna Modeling Design System) is a FDTD EM simulator for simulating arbitrary 3-D structures based on time-domain technique. Every passive structure in this SiP down-converter is simulated with EMDS. The resulting *S*-parameters are exported to ADS and included in the final design verification. Simulated passive structures include bondwires, 3 dB and 10 dB attenuators, microstrip bends, Wilkinson power divider, and TOPS transition.

RF SiP Design Verification Flow with Co-Design Methodology

An RF SiP design typically starts with a system design where a system architectural design is performed. Various system configurations can be evaluated and verified to achieve the best performing and optimized system against design specifications. Also the system parameters of each block in the system can be optimized not only for the performance but also manufacturing costs in this stage. Designers may use commercially available design tools or limited but simple excel spreadsheet to facilitate the system design process. ADS is used for this system's architectural design and optimization.

After the system level performance is evaluated and verified with system behavior models, each block of system behavior models can be replaced by a circuit level model if available. By including the circuit level schematic designs the entire system simulation result can get closer to real-world system behaviors, resulting in more accurate prediction of system performance. Because system blocks may not all have a schematic representation, it is necessary to mix different types of system block representations to simulate the entire system. System blocks without circuit level designs can be represented by the system behavior models. However, due to the mix of system and circuit level models, design tools must allow co-simulation of these different type of models and representations. Agilent's circuit envelope and Ptolemy simulators provide co-simulation technology with the mix of system, DSP, and circuit level designs.

Finally, the simulated results of passive circuits and 3-D interconnects can be added to the final system verification. This is a step-by-step, bottoms-up design verification flow with the co-design methodology.

Quadrupled LO Down-Converter Design Verification

System design tools can predict system behavior easily given the necessary models and design tool input data. Simulation accuracy can be enhanced by bringing real measured data into the simulation world. The system models used in the design tool are normally mathematical models and somewhat ideal in nature. However, most amplifiers have a gain roll-off or imperfect flatness over a frequency range. To overcome this limitation of the model and improve the accuracy, designers can define either frequency dependent gain or link the measured data to the model parameter. In ADS, this can be done through a special component called DAC (Data Access Component). The DAC is a general purpose file reader that accesses file data and links it to the component's model parameters. The Touchstone *S*-parameters can be read by DAC to link them to the model parameters of the gain block to show realistic amplifier behavior.

Figure 8 shows the complete system schematic representation of quadruple LO down-converter SiP based on system behavior models, where amplifier blocks use DAC components to access measured *S*-parameter data. Since the system is basically analog, Harmonic Balance (HB) simulation technology can be used to simulate conversion gain, return loss, and inter-modulation products. The total simulated system gain, RF to IF, is about 13.7 dB, which meets the design specification.

The three MMICs—20~40 GHz MMIC amplifier, 40-GHz MMIC double balanced mixer, and 10~26.5 GHz MMIC frequency doubler—have circuit level representations. The other two MMICs—6~20 GHz MMIC medium power amplifier and 21.2~26.5 GHz low noise amplifier—don't have the circuit level representations. Figure 9 shows some photos of these MMICs. The schematic design of Figure 8 can be now upgraded to a next level where some system blocks are replaced with the circuit level representations. Additionally, EM passive circuit simulation models such as attenuators and dividers can also be brought into the schematic design. Layout components that represent the symbol of subdesigns with the same look of layout with connection pins can be used here in the design to visualize the system connections easily and eliminate potential connectivity design errors. Figure 10 shows the HB 2-tone simulation result of these all combined together. As shown in the figure, the simulation result provides insights of harmonics and spurious frequency contents of the system. In this result, the gain of RF path is still 14.23 dB, which meets the system specification.

Finally, 3-D interconnects, bond-

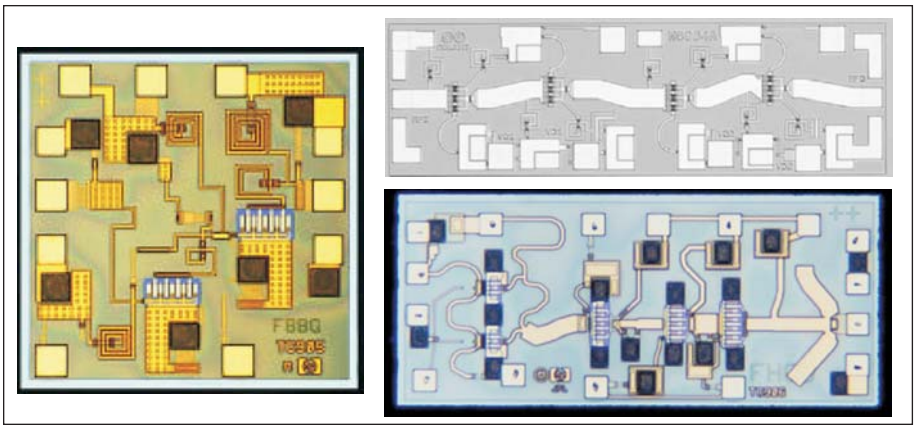

Figure 9 · Some of the MMICs used in the down converter SiP.

wires that connect MMICs, and other passive circuits can be added to the schematic for the final simulation. Although these bondwires are excellent interconnects with very low return loss obtained with compensation networks, it would be a good idea to verify the system performance by including them in the final design verification. The circuit model for the optimized bondwire and EMDS comparison data are shown in Figure 11.

The complete schematic of the quadrupled LO down-converter SiP with bondwire interconnects is shown in Figure 12. The final simulation result of RF path gain is 14.64 dB. As expected, the addition of bondwire interconnects doesn't change the simulation result much. Figure 13 shows ADS layout of the final system.

Quadrupled LO Down-Converter SiP in a Radar System Application

Figure 14 shows the top-level schematic diagram of a radar system that uses the quadrupled LO down-converter in the receiver. The radar system in this example consists of many DSP and analog functional blocks that include chirp source generator, transmitter, T/R switch, radar signal path model, receiver, chirp compressor, and compressed pulse

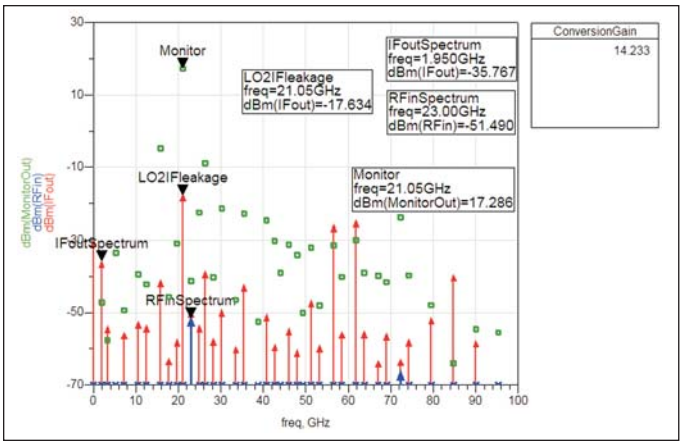

Figure 10 · Harmonic balance simulation result.

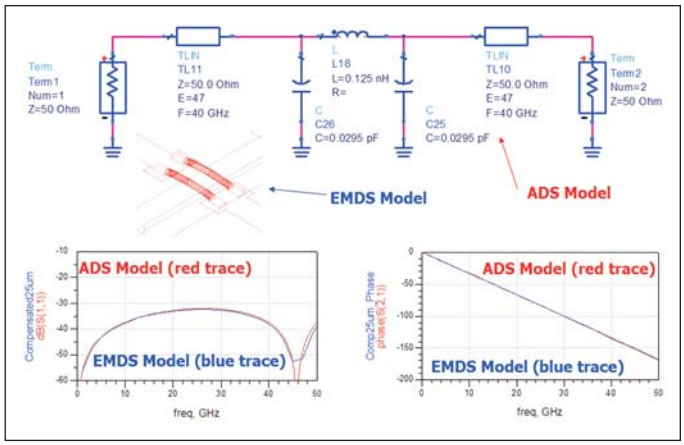

Figure 11 · Bondwire circuit model and EM comparison.

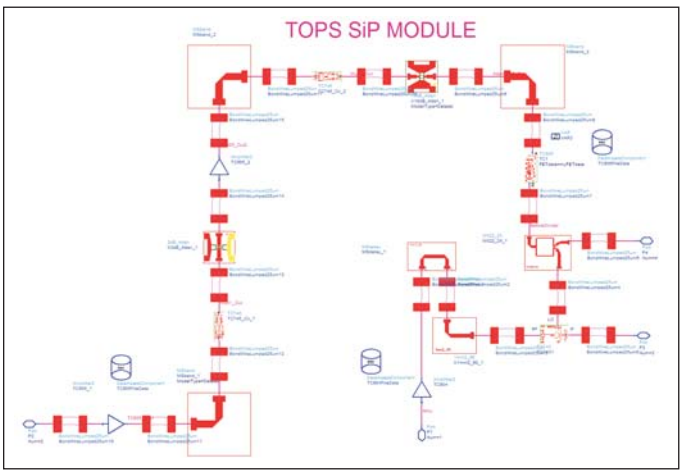

Figure 12 · Final schematic.

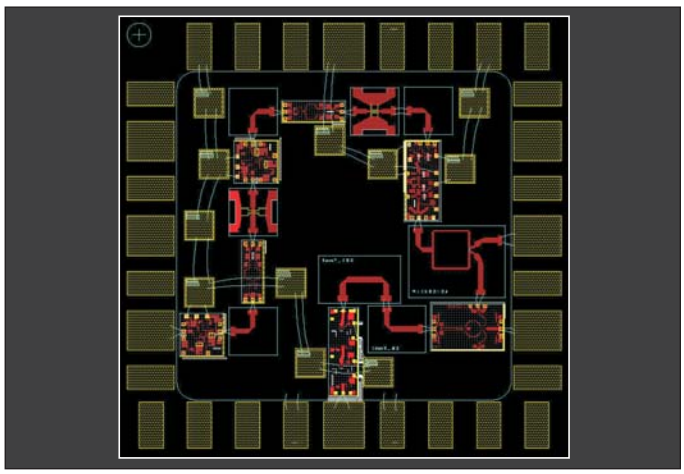

Figure 13 · ADS layout.

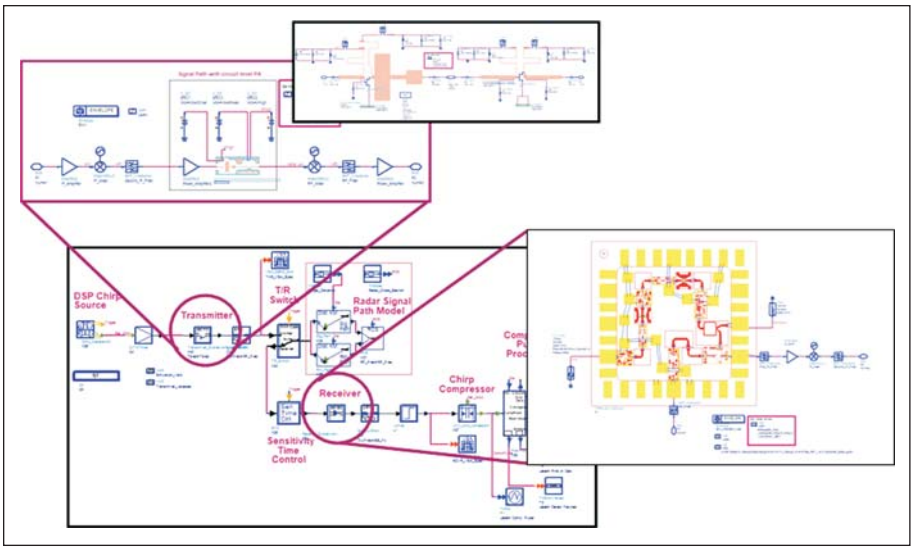

Figure 14 · SiP in a radar system.

processing unit. The front-end down conversion mechanism of the receiver is performed by the quadrupled LO down-converter SiP. This complete radar system consists of all different types of models with circuit, DSP, analog system, and EM level models and can be co-simulated with the Ptolemy simulator to predict and verify the system performance against the design specification. At the transmitter and receiver output node both time- and frequency-domain output data can be measured with a VSA (Vector Signal Analyzer) Sync element in Ptolemy. The VSA output data are shown in Figure 15, and they have the same look-and-feel as do measurement instruments.

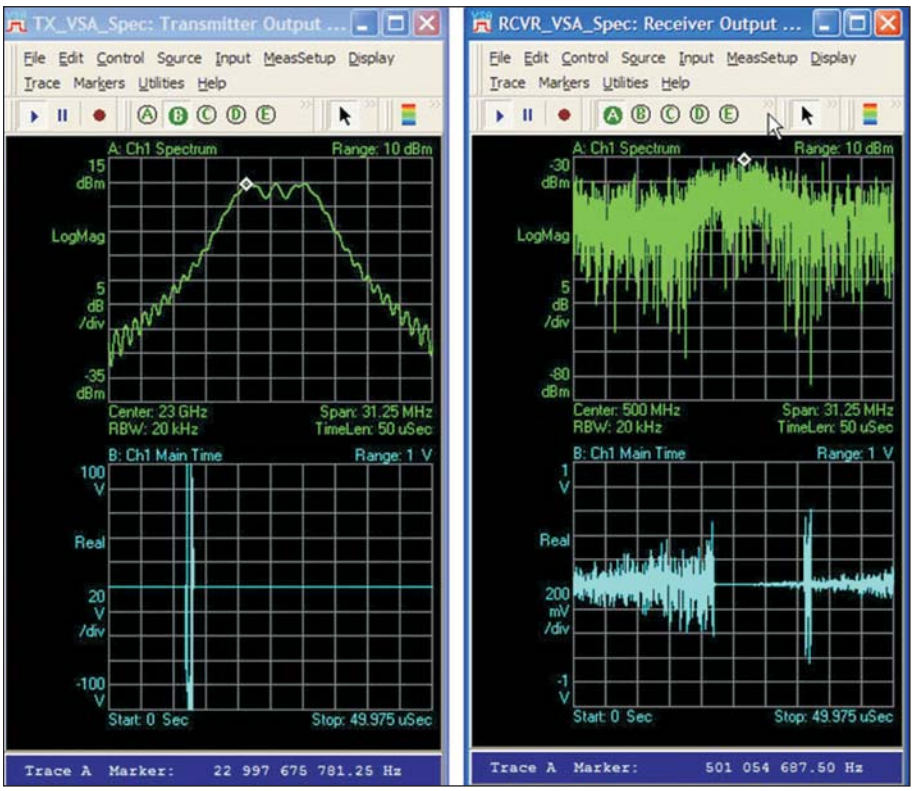

Figure 15 · Simulated TX and RX performance.

Conclusion

In this article, a bottom-up RF SiP design verification flow is demonstrated. With the technology advances of commercial design tools such as ADS, it is possible to simulate the entire system with different technologies and models in an integrated and seamless design environment. The development cycle and cost of RF SiP can be dramatically reduced by accurately predicting the system's electrical performance with the co-simulation technology and methodology.

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Author Information

HeeSoo Lee holds a BSEE degree from the Hankuk Aviation University, Korea, and is an RF SiP/Module design flow specialist in Agilent's EEsof EDA Division, where he is responsible for developing and promoting ADS/RFDE software solutions for RF SiP/Module market. He can be reached at hee-soo_lee@agilent.com

Dean Nicholson is a hardware R&D engineer at Agilent's Electronic Measurements Group, where he is responsible for the development of advanced components for use in next-generation test instruments. He has a BS degree with double major in Electrical Engineering and Material Sciences from University of California Berkeley. Dean has been active in oscillator design, microwave MCM packaging development, and development of advanced switching systems.

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