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# Signal Integrity Analysis and Simulation Tools include IBIS Models

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# Signal Integrity Analysis and Simulation Tools Include IBIS Models

By John Olah and Sanjeev Gupta, Agilent EEsof EDA, and Carlos Chavez-Dagostino, Altera Corporation

**This issue's cover highlights the introduction of Agilent Technologies' ADS2004A, which now includes greatly enhanced capabilities for signal integrity modeling in both time and frequency domains**

Signal integrity is a major concern for engineers working on high data rate designs. Effects such as crosstalk, coupling and delays in transmission lines have a big impact on signal integrity. High-speed digital board designers can now use design tools that combine time-domain IC-specific I/O Buffer Information Specification (IBIS) models with accurate transmission line models to get a better understanding of the signal distortion due to coupling and delays.

## Introduction

In terms of analog simulators, historically, there have been two main camps; time-domain SPICE simulators and frequency-domain simulators using linear S-parameters or nonlinear Harmonic Balance. Each of these simulation domains are known to have strengths and weaknesses in terms of the types of simulations they can best perform, and what circuit models they can best represent. It was difficult to find a single simulator that could handle the breadth of model types for time-domain and frequency-domain that are required for some high-speed circuits. When it comes to the simulation of a circuit for high-speed digital design, these two domains start to merge; digital waveforms that can best be described by their time-varying behavior need to interact with models that are best described by their frequency response. During the past several years, analog design software has seen the emergence of several hybrid-domain simulation techniques, where the simulator is conversant in both time and frequency domain and can combine models suitable for either domain. This article describes the types of models that need to be taken together for high-speed signal integrity analysis, and illustrates their use in a simulation of a high-speed memory circuit.

## Requirements for High-Speed Signal Integrity Simulations

In broad terms, there are three important simulation requirements for analog high-speed signal integrity characterization:

1. A hybrid-domain simulator that handles time-domain and frequency-domain models
2. Accurate transmission line structures (best described in the frequency-domain)
3. Driver and buffer models that terminate either end of the transmission structure (best described in the time-domain)

The next sections will further describe these requirements.

## Hybrid-Domain Simulation—Transient/Convolution

Convolution is one such hybrid-domain simulator to handle both time-domain and frequency-domain models. The main difference between traditional SPICE transient simulation and convolution simulation lies in how each analysis characterizes the distributed frequency-dependent elements of a circuit. A transient analysis is performed entirely in the time-domain, and so it is unable to account for the frequency-dependent behavior of distributed elements such as microstrip models,

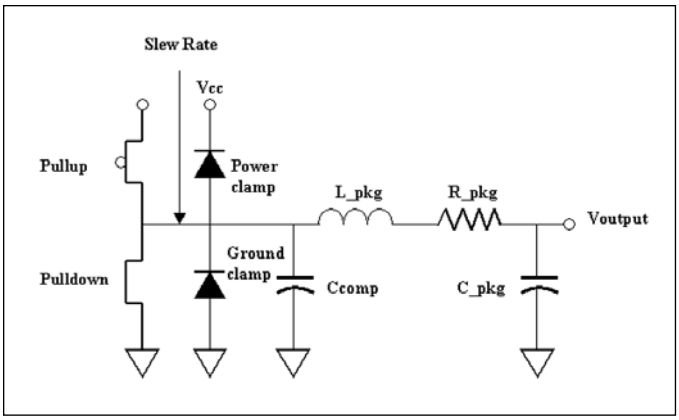


**Figure 1 · A typical output buffer equivalent circuit.**

S-parameter blocks, and so on. In a transient analysis, such elements are represented by simplified, frequency-independent models such as lumped equivalent circuits and transmission lines with constant loss and no dispersion. These assumptions and simplifications are usually sufficient at low frequencies, but are inaccurate at higher data rates.

Convolution converts the frequency-domain information from distributed elements to the time domain, effectively resulting in the impulse response of those elements. The input waveform to the element is convolved with the impulse-response of the element to produce the output signal. Components that have exact lumped equivalent models, including nonlinear elements are characterized entirely in the time domain without using impulse responses.

If the frequency domain model of an arbitrary transmission geometry is not available, an electromagnetic (EM) simulator can provide S-parameter data, or if the actual transmission line has been built then it can be measured with a network analyzer to produce S-parameter data.

The convolution simulator within the Advanced Design System (ADS) from Agilent EEsof EDA is used for the simulations.

## Accurate Transmission Line Structures

Transmission lines represent the connection path for signals between chips. In a high-speed design the signal quality and timing performance determines the inter-symbol interference of a system. The ability to accurately predict printed circuit board performance allows designers to integrate high-speed circuits into their product and improve system quality and reliability. The waveform quality and the timing margins are adversely affected by high frequency transmission line analog effects such as reflection, dispersion, cross talk, ground bounce, and propagation delay. Of particular interest to high speed designers are the multilayer interconnect library models in Advanced Design System. The multilayer transmission line models are based on method of moments and Green's function analytical methods and allow designers to handle arbitrary dielectric layers and arbitrary metal thickness. Multilayer interconnect models in ADS are implemented as the numerical Maxwell's Equations-based solution for the two-dimensional cross-section geometry that is defined by the model parameters.

S-parameters are another frequency-domain approach to describe transmission line effects, and most high-frequency design software, EM simulators and instrumentation either produce or accept S-parameter data.

## Driver and Buffer Models—IBIS Models

To produce the signals that are transmitted between chips, designers can either use transistor-level models of the entire IC, or behavioral models of the driver and buffer circuit. Simulating circuit level I/O buffers can generate a realistic stimulus signal and termination but often the circuit-level description is difficult to obtain from the IC vendor due to issues with intellectual property (IP). Encrypted driver circuits protect the IP but can suffer from long simulation times because the circuit-level netlist of the driver can be quite large, and encrypting does nothing to reduce the complexity of the circuit being simulated. To improve the simulation time while protecting IP, the concept of the IBIS behavioral model was introduced by Intel back in 1990s. The IBIS model provides tabular time-voltage pairs of data describing the rising and falling waveform at the output when triggered by the input signal. Figure 1 illustrates an electrical equivalent model of an output buffer, The devices A and B represent the pullup and pulldown devices while devices C, and D represent Powerclamp and Groundclamp diodes. "Pullup" describes the transistors when the output is high. "Pulldown" describes the transistor when the output is low. To use IBIS data in a simulation environment, the EDA tools need to have an equivalent behavioral model and need to extract SPICE equivalent parameters from IBIS data.

The 2004A release of ADS marks the first time that IBIS models are available for use with the transmission line models and convolution simulator of ADS. The IBIS model makes use of the Symbolically Defined Device (SDD) and Frequency Domain Devices (FDD) to create behavioral models by directly defining port voltage and current relationships using algebraic equations on the schematic page. Frequency Domain Devices allow the use of trigger events and clock enabled events and are used here to create the IBIS behavioral model in ADS. During the transition of logic state, the IBIS behavioral models trigger reading the $V_t$ tables and generate scaling coefficient for the pullup and pulldown devices. Figure 2

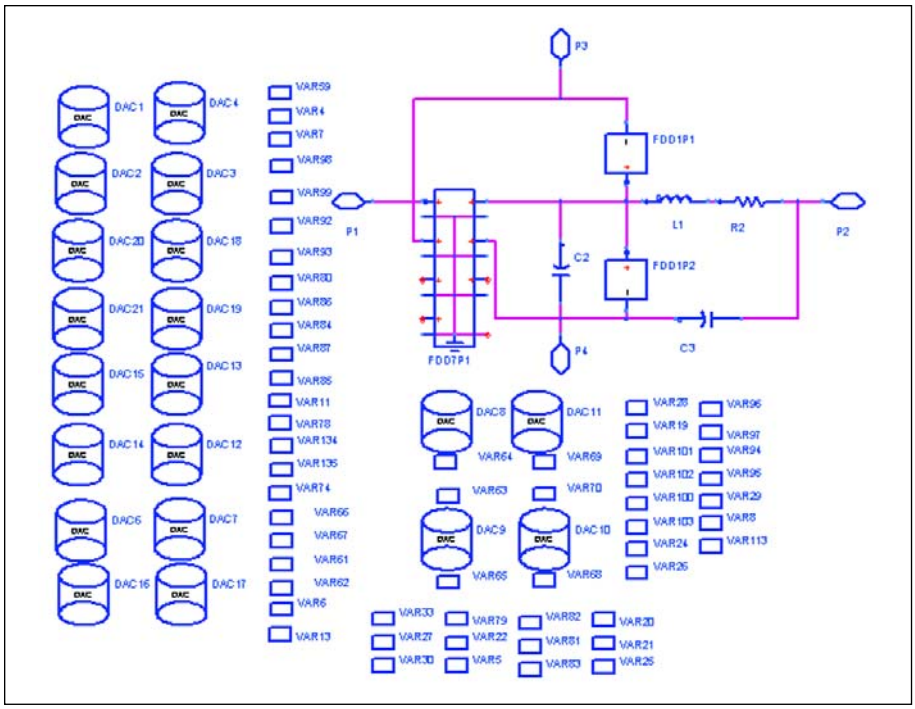


**Figure 2 · The IBIS SPICE equivalent circuit in ADS.**

shows the IBIS equivalent circuit in ADS. A five port FDD is used to define the pullup and pulldown device and all trigger events. Single port FDDs are used to create Groundclamp and Powerclamp

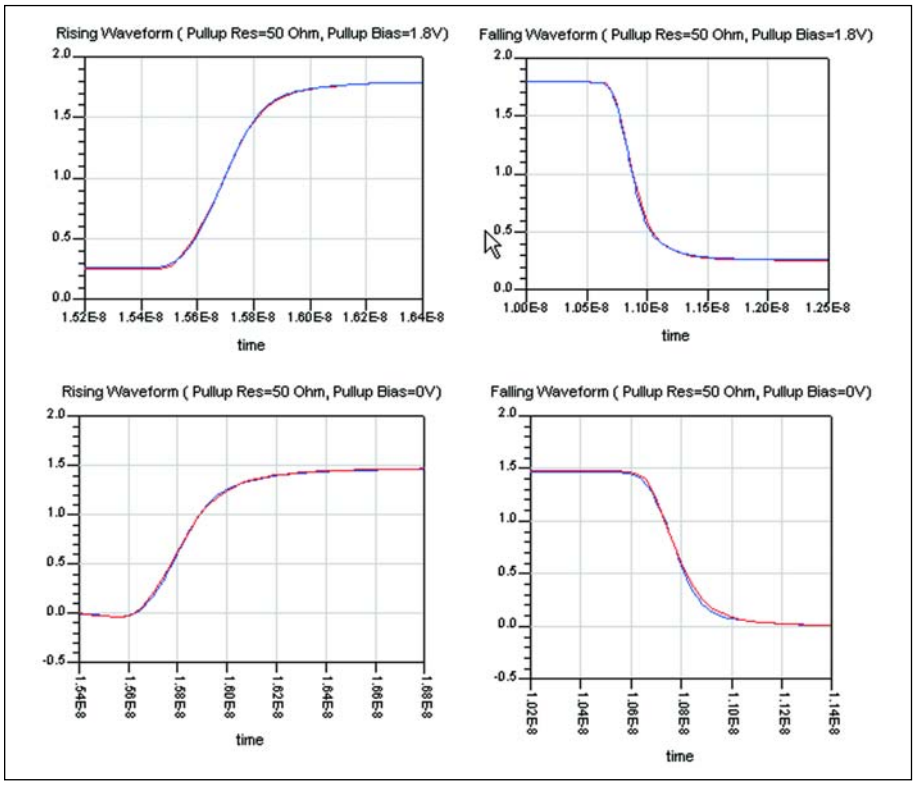


**Figure 3 · Comparison of $V_t$ table waveforms with ADS simulation results.**

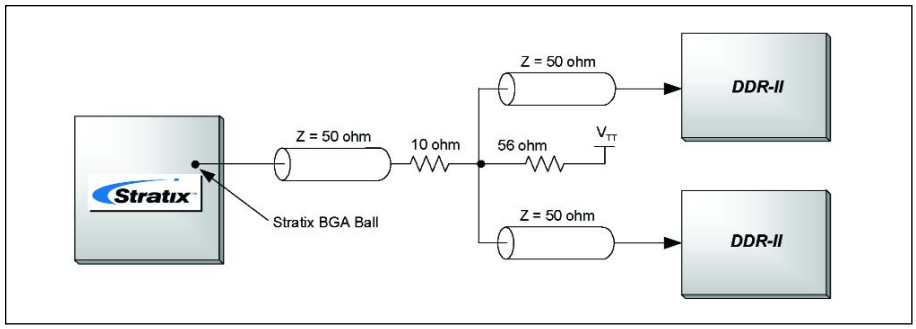


Figure 4 · The Stratix-DDR-II address interface.

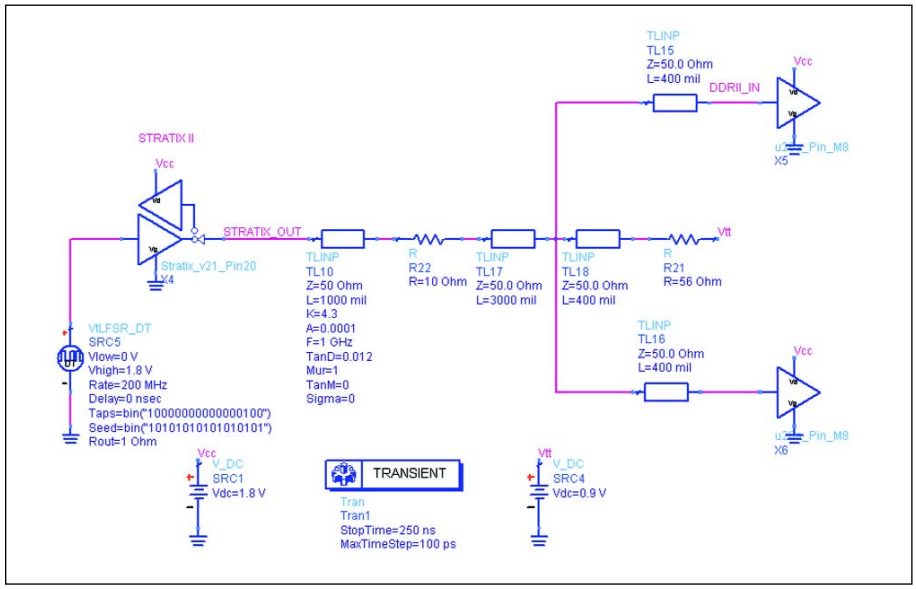


Figure 5 · The Stratix-DDR-II address interface and simulation setup.

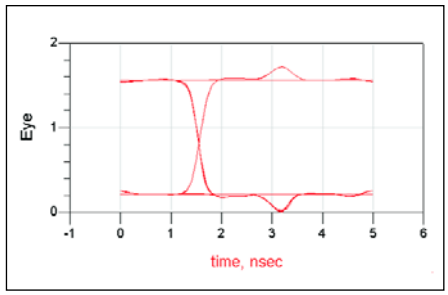


Figure 6 · The Stratix-DDR-II address interface and simulation results.

diodes. The DataAccessComponents are used to access the DC-IV data, $V_t$ data and the differential of $V_t$ data tables.

Next, we will describe an example combining IBIS models, transmission lines and convolution—a DDR-II Interface Address Interface

## Example Simulation—Overview

Simulations are performed using ADS 2004A from Agilent EEsof EDA. IBIS models are created for the Stratix device and the Micron DDR II memory devices. The memory devices used are DDR-II x16 SDRAM (part number Micron MT47H16M16FB). Simulation frequency is 200 MHz or 400 Mega Transfers per second. Simulations for the write cycle are performed for the address bus, since the bus is unidirectional. The address is a point-to-multi-point interface. This is because each address bit is serving more than one memory device.

The total routing length from the FPGA to the memory device is set to ~4.5 inches, which is a conservative estimate in the majority of systems.

Figure 3 shows the rise and fall portion of waveform generated by simulating the Stratix_v21 IBIS model using ADS. The waveforms are in good agreement.

## Pre-Layout Simulations

The pre-layout simulations are required at the earliest stages of the PCB design. In this stage the designer evaluates several topologies and selects the one that fulfills all the specifications such as space, component number and performance. In addition, the results of these simulations help to set crucial parameters for the transmission structure, such as trace width, trace spacing, maximum trace length, and critical component placement. It is important to understand that these simulations are intended for selecting the components and topologies as well as for fine tuning of the signal path. The results analysis is used to set the rules that will be incorporated into the layout.

## SSTL-II Multi-Load Address

The address bus and clocks are often shared among several DDR II devices on the board, so it is harder to achieve good signal integrity on the address bus. This section shows a typical address bit routing topology and a proposed termination scheme.

Figure 4 shows the block diagram of this address scheme. Figure 5 shows the ADS test setup, and Figure 6 shows the simulated waveform at the DDR-II memory IC interconnect balls.

## A0 Post-Layout Simulation

When the layout is complete, a post layout simulation is performed on the critical sections of the board to ensure there are no major signal integrity problems. Based on the results of the post-layout simulation,

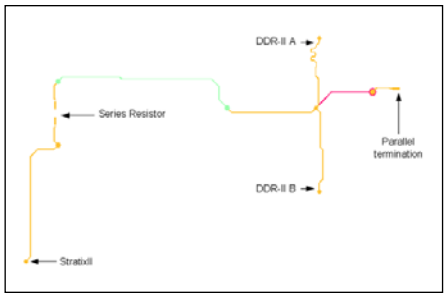


**Figure 7 · The Stratix-DDR-II A0 layout interface.**

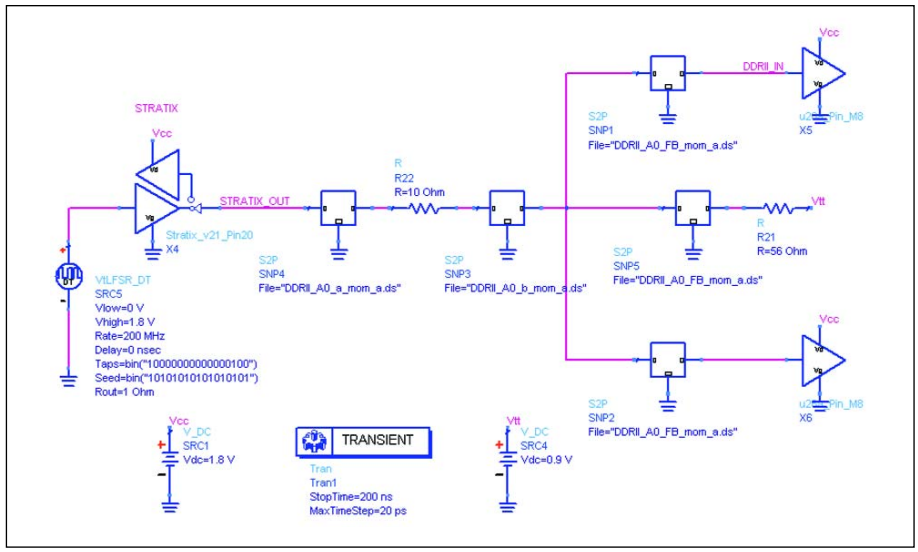


**Figure 8 · The DDR-II address post-layout simulation setup.**

any changes required are incorporated in the layout and the layout is released to the fabrication house for board manufacturing.

The post layout simulation process requires the layout of all active layers on the board as well as the physical properties of the dielectric and metal layers. The post-layout simulations use the physical properties supplied by the fabrication house that may differ from those published.

The frequency domain simulations of the signal paths were performed using ADS Momentum, the method-of-moments based planar electromagnetic simulator in ADS, from 10 MHz to 2.0 GHz and saved as S-parameters (represented as a black box in the post-layout simulations, S2P). The Stack-up used was divided into two major substrates; the external layers (TOP layer and BOTTOM Layer) and the internal dual stripline differential layers. Partitioning the stack-up reduces the computing time required by several orders of magnitude without impacting the accuracy of the results. Figures 7 through 9 show the layout, the simulation setup, and the simulation results.

## Stratix-DDR-II Address (A0) Interface Measurements

Measurements were taken using a 6 GHz oscilloscope and high impedance probes. The measured data shows good correlation with simulated data, as shown in Figure 10.

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3. "User Defined Models," Agilent ADS 2003C manual.

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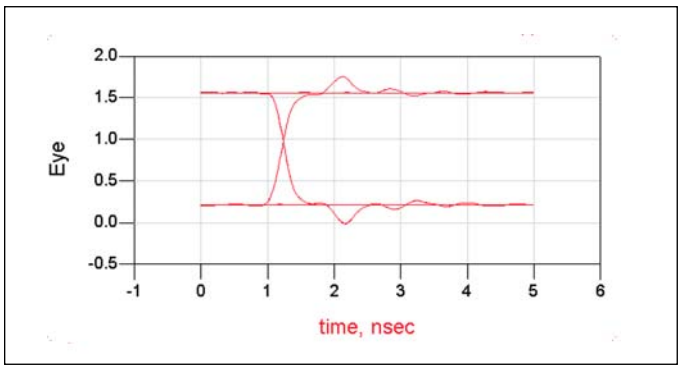


**Figure 9 · The DDR-II address post-layout simulation results.**

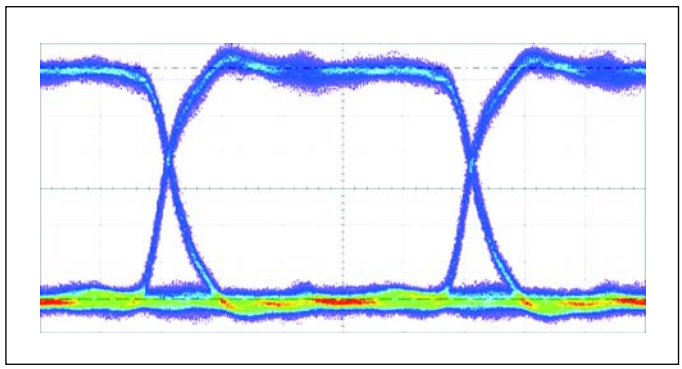

**Figure 10 · The DDR-II address interface simulated versus measured results.**

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