Agilent EEsof EDA

Presentation on Power Amplifier Design with Custom Templates

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Seminar: Gain Without Pain
November 2000

Making Power Amplifier Design Easier with Custom Templates

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Abstract
Designing power amplifiers has become increasingly complex, particularly with respect to linearity and power-added efficiency. Attaining optimum design results--and product success--requires a comprehensive and detailed analysis of the myriad trade-offs that result from adjusting all key specifications, including accurate simulations of each potential deployment strategy. Time-to-market and design efficiency are also critical. The Agilent Power Amplifier Designer's Application Kit is designed to make the entire power amplifier design process easier, as well as providing access to standard analysis techniques. The kit includes specification and templates matrices, sample design flows for power amplifiers, classic design topologies, circuit and display templates, plus complete documentation and reference materials.

Instructor's Biography
Andy Howard is a senior application development engineer with the Agilent EEsof facility located in Santa Rosa, California. Andy has over 15 years of experience designing and simulating circuits, with special emphasis on phase-lock loop and oscillator design. Andy's current responsibilities include the development of examples for use with the Agilent Advanced Design System, including RF integrated circuit and board applications.

Power Amplifier Design with Templates

This section of the workshop will focus on designing power amplifiers with the Agilent Advanced Design System using custom templates. Templates simplify the use of ADS and are a powerful productivity tool for designing power amplifiers.

Topics

- Templates
  - What they are and how they help
- Power amplifier design flow examples
  - Specifications and other parameters that can be simulated
- Template examples
  - DC simulations of I-V curves
  - High-frequency nonlinear simulations

First we'll describe what simulation and data display templates are. Then we'll cover what they can do.

Second, we'll look at several example design flows for power amplifiers, including an overview of the specifications and parameters that can be simulated. Our design flow examples include a small-signal design using only linear S-parameters, one for Class A design when a nonlinear model is available, and finally more advanced simulations that are useful for nonlinear amplifier design and characterization.

The last part of this section includes examples of schematic and data display templates.

Templates --What They are and How They Help

- **Simulation Templates:**
  Pre-configured schematics for simulating noise figure, gain, ACPR, gain compression, etc.
- **Synthesis Templates:**
  Pre-configured schematics for synthesis or optimization of matching networks, bias networks, harmonic impedance terminations, etc.
- **Data Displays:**
  Pre-configured results reporting

The Agilent Advanced Design System is a powerful and flexible simulation tool, but its complexity can also make it cumbersome, especially for the occasional user. This situation is remedied in large part by the numerous examples that are included with version 1.0 and 1.1. But we've gone a step further. To make ADS a truly user-friendly tool, we are in the process of developing a series of highly useful templates. These templates include preconfigured schematics ideal for simulating standard sets of common parameters, plus preconfigured data displays for displaying and reporting results.

Templates are broken into two groups. The first type are used for simulation only, while the second type are used to perform synthesis (via direct calculation) or optimization. These templates represent a powerful set of resources for designers.

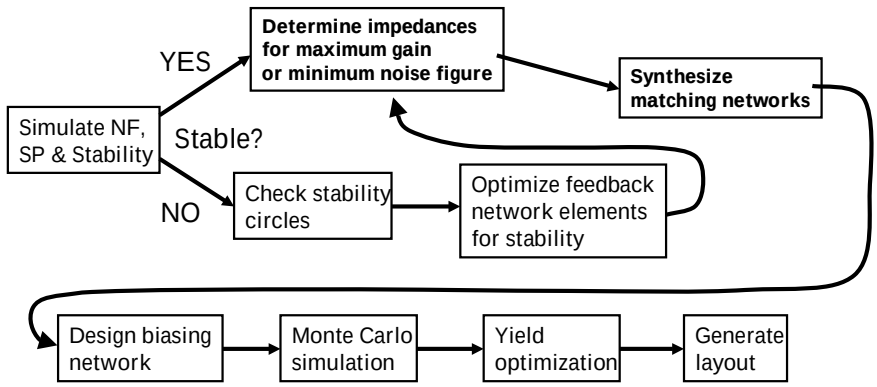
Small-Signal Amplifier Specifications for Simulations

- Noise figure
- Associated gain (gain with source matched for minimum noise figure, load for max. gain)
- Input and output match
- Reverse isolation
- Stability
- Group delay
- Frequency variation
- Statistical variation

This slide summarizes specifications that might be of interest to an engineer designing small-signal amplifiers. Depending on the application, they may all be important. The ADS can be used to simulate the entire list, and templates are currently being developed to include them all as well.

Linear Design Flow with S-parameters

(assumes measured device S-parameters and NF data available)



While this is a workshop for power amplifier design, much of the methodology used to design linear amplifiers (using only S-parameters) can be applied. This slide shows a process flow suitable for designing a linear amplifier when only S-parameters (and possibly noise parameters) are available. Steps could be added or removed and the order could be changed, but for our purposes it represents a good example.

In particular, Monte Carlo simulation and yield optimization are two steps that are often neglected by designers, yet can have a significant impact on product success. CAE is particularly well-suited for these types of simulations.

Large-Signal Amplifier Specifications for Simulations

(in addition to small-signal specifications)

- Input-Output power characteristic
- N-dB Gain compression point
- Nth-order Intermodulation distortion and/or TOI
- Power-added efficiency (PAE)
- Adjacent-channel power ratio (ACPR)
- Harmonics
- Supply current versus output power
- Noise power ratio
- AM-to-PM distortion
- Error vector magnitude

This slide summarizes a number of specifications that might be of interest to an engineer designing nonlinear power amplifiers. The ADS can be used to simulate the entire list, and templates are being developed that incorporate all of these specifications.

All of these specifications describe distortions due to nonlinearities in an amplifier's active device, and simulation accuracy is highly dependent on the models employed. The next section of this workshop provides information on device models in some detail.

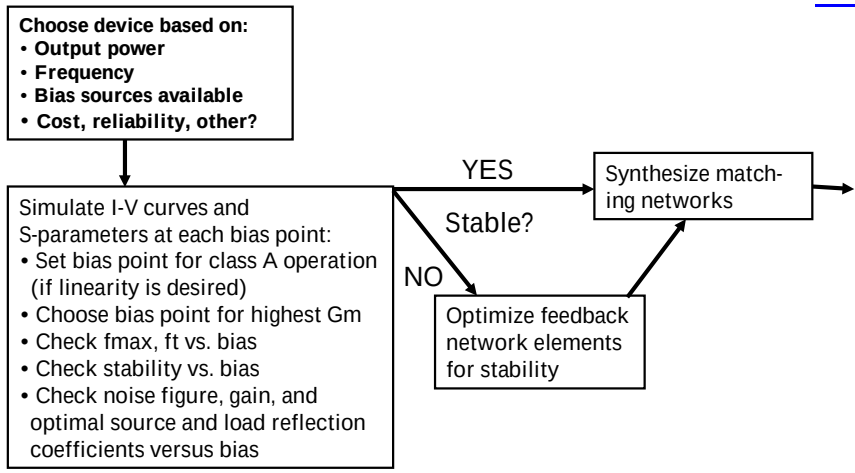
More Large-Signal Simulations

- Check all specifications versus temperature, bias, frequency, or other parameters
- Optimize harmonic source and load impedances to maximize TOI, Pout, PAE, etc.
- Load pull and source pull
- Large-signal input and output impedances
- Dynamic load line
- Time-domain voltage and/or current waveforms
- Cross-modulation

Complex nonlinear simulations, such as those listed in this slide, are also supported. Some will be described in more detail later in this section of the workshop.

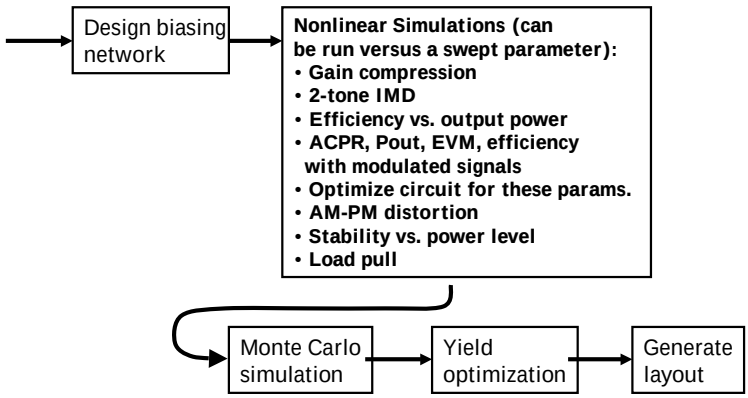
The ADS is highly flexible, enabling designers to simulate almost any specification or characteristic versus any swept parameter. This is a very powerful capability that enables designers to easily verify designs over temperature, frequency, bias conditions, etc. It also helps designers determine the relative effect that each user-defined parameter will have on final circuit characteristics, simplifying and speeding up the task of setting them correctly. This flexibility also enables complex optimizations to be carried out with relative ease.

Design Flow for Large-Signal Simulation (Slide 1 of 2)



Assuming that a nonlinear device model is available, this slide and the next one describe an example design flow for a large-signal power amplifier simulation. The process begins with simulations to help the designer choose a bias point. The design flow then proceeds to stabilization if necessary, and then to synthesis of matching networks, similar to the design flow shown previously.

Design Flow for Large-Signal Simulation (Slide 2 of 2)



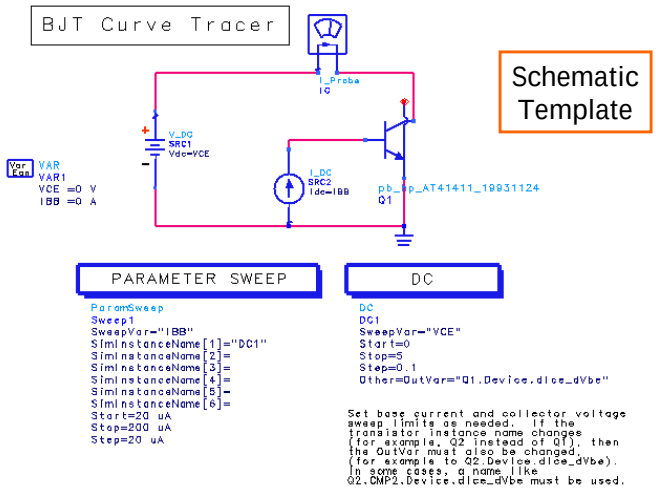
The design flow continues with bias network design, and then proceeds with any of a series of possible nonlinear simulations which are chosen based on specifications critical to the design.

Topics

- Templates
  — What they are and how they help
- Power amplifier design flow examples
  — Specifications and other parameters that can be simulated
- Template examples
  — DC simulations of I-V curves
  — High-frequency nonlinear simulations

At this stage, we will investigate several simulation examples utilizing the schematic and data display templates.

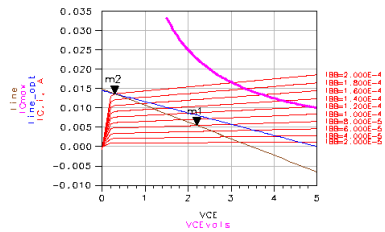
BJT I-V Curve Simulation



This slide shows a schematic template for a simple setup used to simulate the DC current-versus-voltage (I-V) curves of a bipolar junction transistor (BJT). The base current is swept, and for each value the collector voltage is also swept. At each bias point, the collector current and DC transconductance is computed. The resulting I-V curves provide the basis for determining where to set the bias point for each class of operation.

Biasing for Class A Operation

Data Display Template



m2
VCE=0.300000
IBB=0.000200
IC.i=0.013643

m1
VCE=2.200000
IBB=0.000080
IC.i=0.005477

1) Move marker m2 to the knee of the I-V curve.
2) Specify maximum allowed VCE, VCEmax.
3) Position marker m1 at desired bias point.
4) DC power consumption, average output power in linear operation, DC-to-RF efficiency are all dependent on position of marker m1.
5) Load resistance for maximum output power, Rload_opt is dependent on marker m2 and maximum voltage, VCEmax.

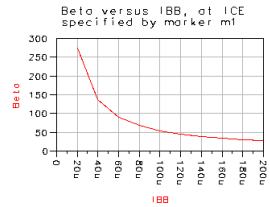
Eqn VCEmax=5 Eqn PDmax=0.05

Marker m1 bias point values, (Assuming Class A.)

Output Power Watts	dBm	DC-to-RF Efficiency,%
5.203m	7.163	43.182

Rload	DC Power Consumption
232.683	12.049m

Beta versus IBB, at ICE specified by marker m1



Optimal Class A bias point values.

Output Power at Optimal Bias Watts	dBm	DC-to-RF Efficiency,%	Optimal VCE
8.015m	9.039	44.340	2.650

Rload at Optimal Bias	DC Power Consumption at Optimal Bias	Optimal ICE
344.508	18.076m	6.821m

This slide illustrates the use of a data display template used to report simulation results, as well as several amplifier characteristics, depending on the selected bias point. One load line is drawn between marker m2 (which the user should position at the “knee” of the I-V curves) and the maximum collector-emitter voltage (VCEmax), which may be specified by the user.

The optimum values are calculated assuming that:

1) the optimum load resistance is present at the device output;

2) that the collector-emitter voltage swings between VCEmax and the voltage at the “knee” (marker m2); and

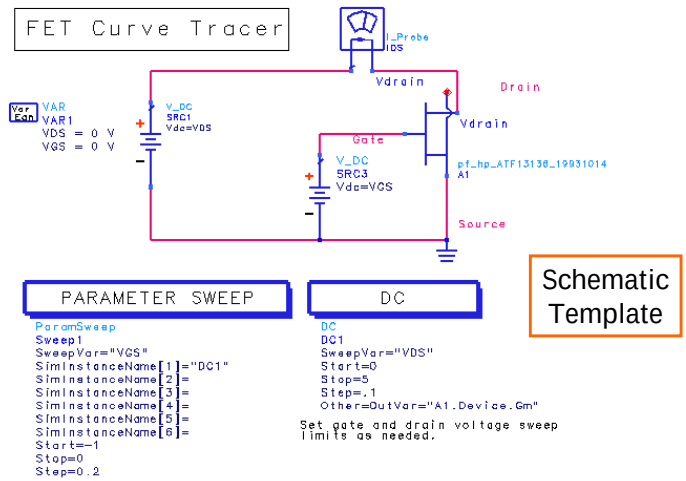
3) that the collector current swings between zero and the “knee” (marker m2).

Marker m1 can be moved to an arbitrary bias point. A different load line is generated between this marker and marker m2. In this case, the values are calculated assuming that:

1) the collector-emitter voltage never goes above the point at which the new load line intersects the x-axis and is symmetrical about marker m1; and

2) that the collector current never goes below zero and is also symmetrical about marker m1.

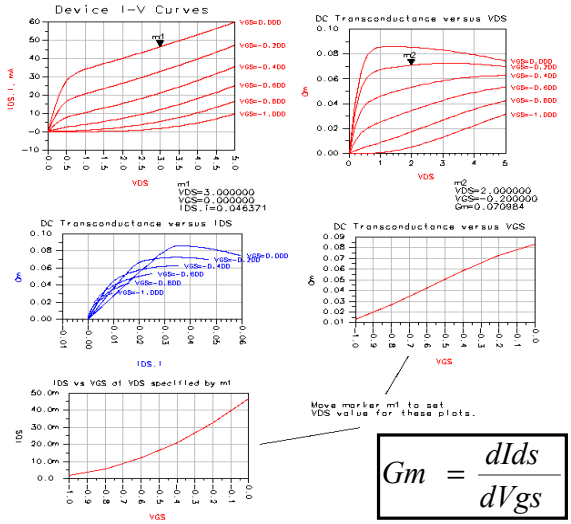
FET I-V Curve Simulation



This slide shows a simple setup that can be used to simulate the DC current-versus-voltage (I-V) curves for a field effect transistor (FET). The gate voltage is swept, and for each value the drain voltage is also swept. At each bias point, the drain current and DC transconductance is computed. From the device's I-V curves, a designer can easily determine where to set the bias point for a particular class of operation. For FETs, the transconductance (Gm) varies with the bias point, so this simulation can be used to indicate which bias point will maximize Gm.

FET Transconductance (Gm) vs. Bias Point

Data Display Template



Select this listing column, then "View/Scroll Data" to scroll through the data.

VDS	Gm
VGS=-1.000	
0.000	0.000
0.100	0.000
0.200	0.000
0.300	0.000
0.400	0.000
0.500	0.000
0.600	0.000
0.700	0.000
0.800	0.000
0.900	0.000
1.000	0.000
1.100	0.001
1.200	0.001
1.300	0.001
1.400	0.002
1.500	0.002
1.600	0.003
1.700	0.003
1.800	0.004
1.900	0.004
2.000	0.005
2.100	0.006
2.200	0.006
2.300	0.007
2.400	0.008
2.500	0.009
2.600	0.010
2.700	0.010
2.800	0.011
2.900	0.012
3.000	0.013
3.100	0.014
3.200	0.015
3.300	0.016
3.400	0.017
3.500	0.018

$$Gm = \frac{dIds}{dVgs}$$

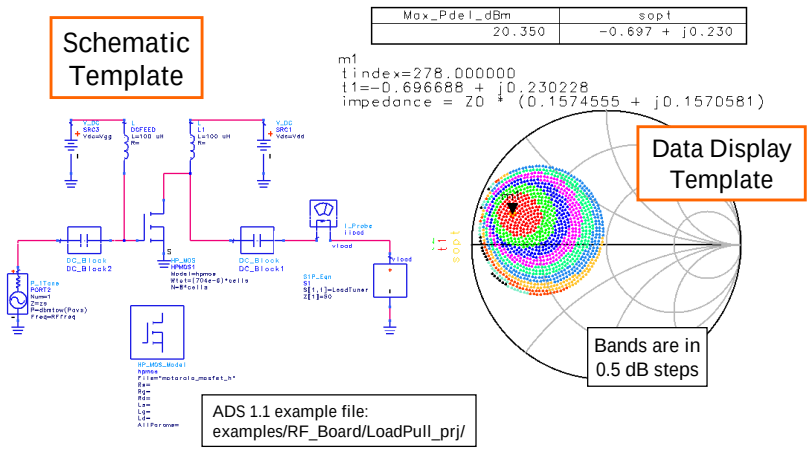
This slide shows the results of the simulation of DC current-versus-voltage (I-V) curves for an FET. Transconductance (Gm) is plotted versus drain voltage, collector current, and gate voltage (at a single drain voltage value). Using these plots, a designer can easily predict the bias point that will maximize Gm.

High Frequency Nonlinear Simulation Setups and Results

- Load-pull
- Harmonic impedance optimization
- Swept single input tone
  - Available source power sweep
  - 1-dB gain compression point versus bias
- Swept two input tones
- Multi-tone inputs
- Swept power source with CDMA modulation

The remainder of this section will cover a number of examples of other nonlinear simulations, including setups and results.

Load-Pull Simulation



This slide illustrates the setup used for a load-pull simulation, as well as the corresponding results presented with an ADS data display template. The user specifies a circular region within the Smith Chart where the load impedances are generated. The circuit is then simulated for each load impedance and the output power is plotted as different colored bands on the Smith Chart (based on user-specified steps). In this example, the impedance was varied at the fundamental frequency only. In an actual simulation, the user could specify arbitrary load impedances at each harmonic frequency, and arbitrary source impedances at the fundamental frequency as well as each harmonic frequencies.

Load-pull simulations can also be setup using two input tones. For two-tone simulations, the source and load “beat” frequency (the difference between the two input tone frequencies) impedance can also be specified. The third-order intercept (TOI) can be plotted on a Smith Chart, but input power may need to be reduced, since TOI is extrapolated from relatively low levels of distortion.

Source-pull simulations indicating how output power or TOI might be affected by source impedance can also be run.

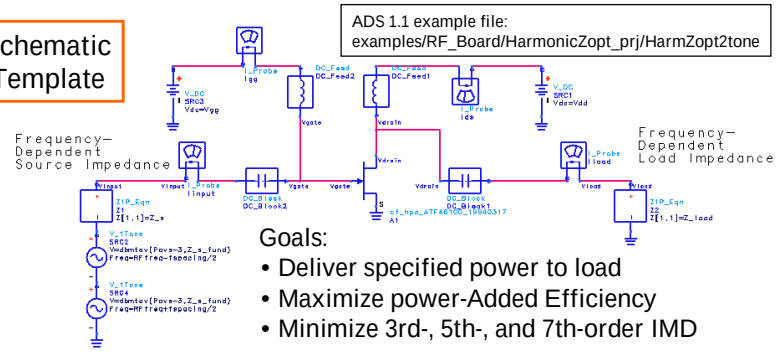
Before running any of these simulations, it’s a good idea to check the stability of the circuit, since source and load impedances from unstable regions can result in simulations that will not converge. Actual measurements of a circuit under these conditions would likely reveal oscillations.

Load-pull contours are currently scheduled for release in ADS Version 1.3.

Source and Load Harmonic Impedance Optimization

ADS 1.1 example file:
examples/RF_Board/HarmonicZopt_prj/HarmZopt2tone

Schematic Template



Two-tone Source

Goals:
- Deliver specified power to load
- Maximize power-Added Efficiency
- Minimize 3rd-, 5th-, and 7th-order IMD

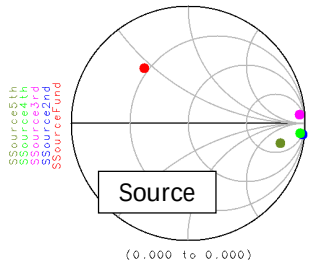
Optimize:
- Source and load fundamental and harmonic impedance terminations
- Source power level

This slide shows an alternate approach to achieving high output power versus conventional load-pull techniques. In this case, optimization is used to deliver the specified power to the load, to maximize power-added efficiency, and to minimize intermodulation distortion. Parameters that can be modified during optimization include source and load impedances at fundamental and harmonic frequencies, as well as available source power.

This simulation approach is potentially much more powerful than load-pull simulation, since source and load impedances can be varied simultaneously.

As in the previous example, the user must consider the stability of the circuit. An unstable circuit with load and source impedances that can vary anywhere on the Smith Chart is likely to exhibit convergence problems. It's worth noting that the user can set the range of impedances that are allowed during optimization.

Optimal Load and Source Fundamental and Harmonic



ZSourceFund
15.014 + j22.279

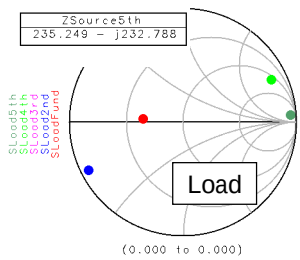
ZSource2nd
132.705 – j994.156

ZSource3rd
518.799 + j1000.000

ZSource4th
386.683 – j999.123

ZSource5th
235.249 – j232.788

Data Display Template



ZLoadFund
23.873 + j1.391

ZLoad2nd
1.764 – j12.107

ZLoad3rd
725.557 + j998.550

ZLoad4th
66.790 + j198.859

ZLoad5th
759.044 + j986.554

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Power AmplifierDesign with Templates, A.Howard

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The Smith Charts on this slide reveal the optimal source and load reflection coefficients at the fundamental and harmonic frequencies for the load and source impedance optimization in the previous example. The optimal impedances, computed from the reflection coefficients, are also shown.

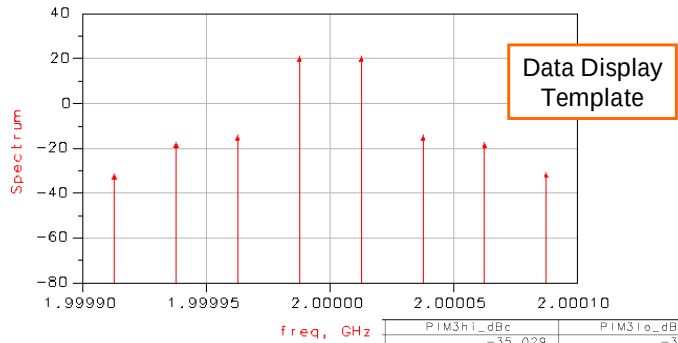
Additional information on harmonic impedance terminations is available in the following reference papers:

S. Mazumder, et al., "Improvement of a Class-C Transistor Power Amplifier by Second-Harmonic Tuning", IEEE Transactions on MTT, Vol. MTT-27, No. 5, May, 1979, page 430.

L. C. Hall and R. J. Trew, " Maximum Efficiency Tuning of Microwave Amplifiers", 1991 IEEE MTT Symposium Digest, Session D-1, Page 123.

S. Nishiki and T. Najima, "Harmonic Reaction Amplifier--A Novel High-Efficinecy and High-Power Microwave Amplifier", 1987 IEEE MTT Symposium Digest, Session DD-5, Page 963.

Output Spectrum Near Fundamental Tones



Data Display Template

Intermodulation Distortion Levels

PIM3hi_dBc	PIM3lo_dBc
−35.029	−35.138

PIM5hi_dBc	PIM5lo_dBc
−38.289	−38.464

PIM7hi_dBc	PIM7lo_dBc
−51.712	−52.465

This slide shows the output spectrum and intermodulation distortion levels (in dBc) with optimal source and load impedances, for the load and source impedance optimization in the previous example.

Gain, Output Power, PAE, and Power Dissipation

Data Display Template

Gain_operating	Gain_transducer
20.163	9.958

Gain(operating)=(Power delivered to load)/ (Power delivered to device)

Gain(transducer)=(Power delivered to load)/ (Power available from source)

Pdel_dBm	Pdel_Watts
23.822	0.241

PAE
21.477

Pdel_Watts is the power in the two fundamental output tones only, thus it is less than total power.

Thermal_diss	Pdc	Total_input_pwr	Total_output_pwr
0.769	1.009	1.011	0.242

This slide shows a range of results for the load and source impedance optimization in the previous example. It includes operating and transducer power gains at fundamental frequencies, power delivered to the load in both fundamental frequencies, power-added efficiency, thermal dissipation, DC power consumption, and total input and output power. Total input power includes the power delivered to the network at all frequencies, plus the DC power. Total output power includes the power delivered to the load at all frequencies.

The large difference between operating and transducer power gains (which include power in the fundamental tones only) indicates that power delivered to the device is much smaller than the power available from the source. This indicates a significant mismatch at the input in the fundamental frequencies.

Equations Used for Optimization

Computation of power delivered and power-added efficiency

```
MeasEqn
meas1
    Pdel1_W=0.5*real(mix(Vload,{1,0})*conj(mix(Iload.i,{1,0})))
    Pdel2_W=0.5*real(mix(Vload,{0,1})*conj(mix(Iload.i,{0,1})))
    Pdel_Watts=Pdel1_W+Pdel2_W
    Pdel_dBm=10*log(Pdel_Watts) +30
MeasEqn
meas2
    Pdc=mag(Ids.i[0] * Vdrain[0]) +mag(Igg.i[0]*Vgate[0])
    Pavs_Watts=10**((Pavs_test-30)/10)
    PAE=100*((Pdel1_W +Pdel2_W)-Pavs_Watts)/Pdc
```

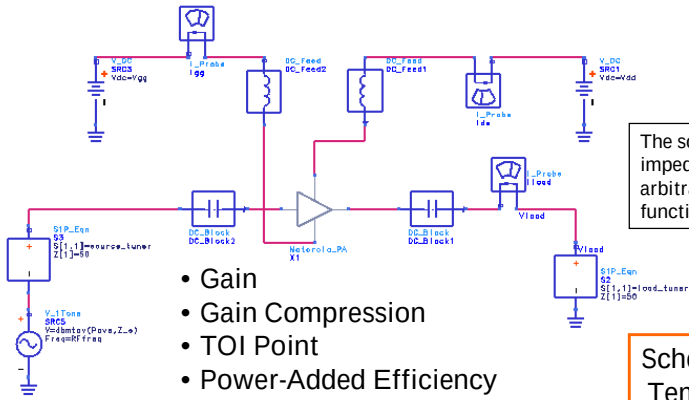
Computation of intermodulation distortion terms

```
MeasEqn
meas3
    PIM3hi_W=0.5*real(mix(Vload,{-1,2})*conj(mix(Iload.i,{-1,2})))
    PIM3lo_W=0.5*real(mix(Vload,{2,-1})*conj(mix(Iload.i,{2,-1})))
    PIM3hi_dBc=10*log(PIM3hi_W/Pdel2_W)
    PIM3lo_dBc=10*log(PIM3lo_W/Pdel1_W)
MeasEqn
meas4
    PIM5hi_W=0.5*real(mix(Vload,{-2,3})*conj(mix(Iload.i,{-2,3})))
    PIM5lo_W=0.5*real(mix(Vload,{3,-2})*conj(mix(Iload.i,{3,-2})))
    PIM5hi_dBc=10*log(PIM5hi_W/Pdel2_W)
    PIM5lo_dBc=10*log(PIM5lo_W/Pdel1_W)
MeasEqn
meas5
    PIM7hi_W=0.5*real(mix(Vload,{-3,4})*conj(mix(Iload.i,{-3,4})))
    PIM7lo_W=0.5*real(mix(Vload,{4,-3})*conj(mix(Iload.i,{4,-3})))
    PIM7hi_dBc=10*log(PIM7hi_W/Pdel2_W)
    PIM7lo_dBc=10*log(PIM7lo_W/Pdel1_W)
```

```
MeasEqn
meas6
    Spectrum=10*log(0.5*real(Vload*conj(Iload.i))) +30
    Vout=Vload
    Iout=Iload.i
    Vin=Vinput
    Iin=Iinput.i
MeasEqn
meas8
    Gain_transducer=Pdel_dBm-Pavs_test
    Pin1_W=0.5*real(mix(Vinput,{1,0})*conj(mix(Iinput.i,{1,0})))
    Pin2_W=0.5*real(mix(Vinput,{0,1})*conj(mix(Iinput.i,{0,1})))
    Pin_Watts=Pin1_W+Pin2_W
    Pin_dBm=10*log(Pin_Watts) +30
    Gain_operating=Pdel_dBm-Pin_dBm
MeasEqn
meas9
    Total_input_pwr=Pdc+sum(0.5*real(Vinput*conj(Iinput.i)))
    Total_output_pwr=sum(0.5*real(Vload*conj(Iload.i)))
    Thermal_diss=Total_input_pwr-Total_output_pwr
```


This slide includes some of the equations used to compute the results in the previous series of slides. Many hours were spent developing these equations and designing the data display templates to present results in a convenient format—a testament to the value that they provide. And many more, equally complex, templates are under development. The end result is that users are saved the tedious task of learning the intricate details of ADS to develop these calculations and displays, providing a significant boost in productivity.

1-Tone, Swept Power Simulation



The source and load impedance can be set arbitrarily, and as a function of frequency.

- Gain
- Gain Compression
- TOI Point
- Power-Added Efficiency
- DC Drain Current

...versus Swept Input Power

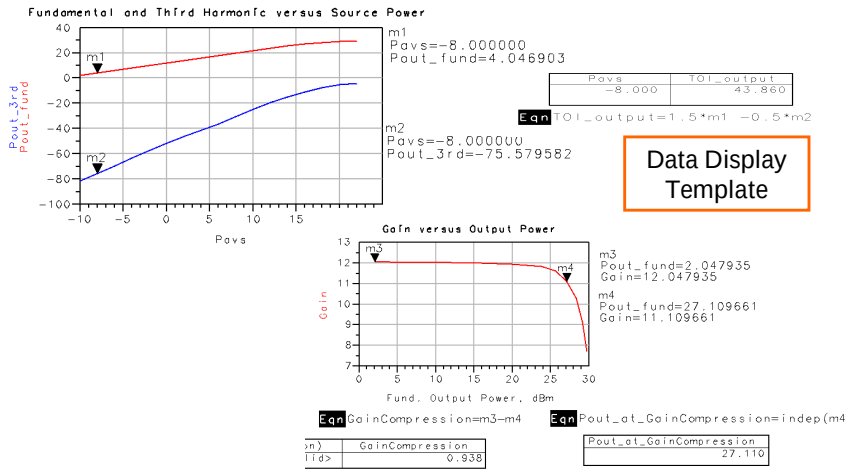
Schematic Template

ADS 1.0 example file:
examples/RF_Board/NADC_PA_prj/PA_HB1tone

Once the optimal source and load impedance is known for each harmonic frequency, input and output matching networks can be created—a step that is not depicted here.

In the next step, shown in this slide, we analyze the performance of the completed amplifier. Using a sinusoidal signal as input, a number of characteristics can be simulated with available power as a swept parameter. This template enables the user to set source and load harmonic impedances arbitrarily, a useful feature when evaluating unmatched devices. With matching networks already created, source and load impedances are fixed at 50 ohms for all frequencies.

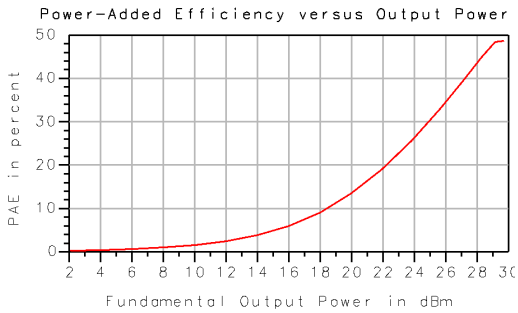
1-Tone Gain Compression, TOI



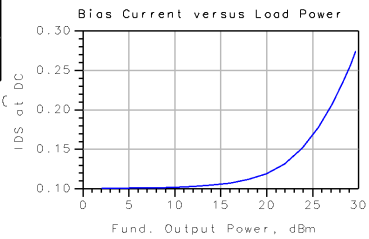
This slide shows the fundamental frequency and the third harmonic versus available source power. Also depicted are gain versus fundamental output power, the approximate 1-dB gain compression point, and the third-order intercept point. A more precise 1-dB gain compression point can be calculated using the “Gain Compression” simulation controller or by simply sweeping the available source power using finer resolution.

A similar example of the simulated and measured gain compression of an amplifier was presented at the Hewlett-Packard 1999 RF Design and Measurement Seminar. The measured data is shown on page 95 of the seminar text, while the simulated data is shown on page 96. In the seminar example, the simulated output power at the 1-dB gain compression point was 27.1 dBm versus a measured value of 27.6 dBm. The simulated gain at the 1-dB compression point was 23.91 dB, versus 23.93 dB measured.

Power-Added Efficiency, Drain Current versus Output Power

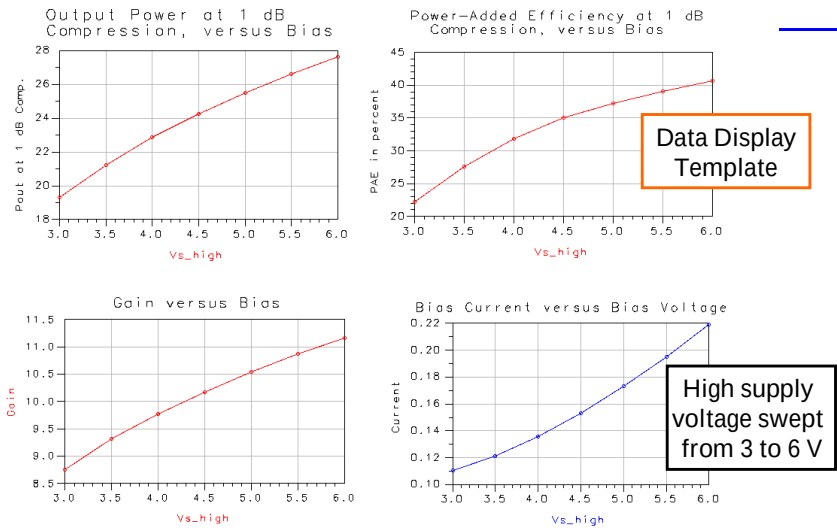


Data Display Template



This slide shows power-added efficiency and bias current versus fundamental output power from the same example used in the previous series of slides.

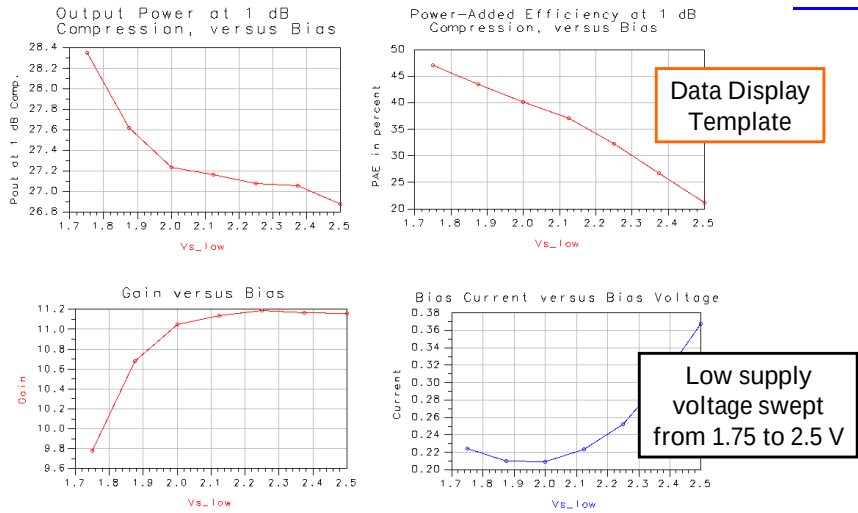
Swept Bias Simulation (Slide 1 of 2)



It is useful to know how the amplifier will perform based on parameters such as bias voltage. This slide shows the results of the amplifier's simulated characteristics versus high supply voltage (drain bias). This information could be helpful in setting bias voltage and current, as well as understanding the device's sensitivities. In this case, the low supply voltage (gate bias) was fixed at 2 volts.

The characteristics of the amplifier can also be simulated versus other parameters such as temperature, assuming that the device model includes temperature dependencies.

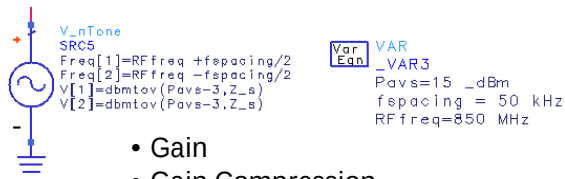
Swept Bias Simulation (Slide 2 of 2)



This slide shows the results from a similar simulation as the previous example, except that low supply voltage (gate bias) is the swept parameter. According to these results, the amplifier can achieve higher 1-dB gain compression power and higher power-added efficiency (at the expense of lower gain) by slightly lowering gate bias voltage.

2-Tone, Swept Power Simulation

Same schematic as 1-Tone, swept power simulation except for 2-tone input source



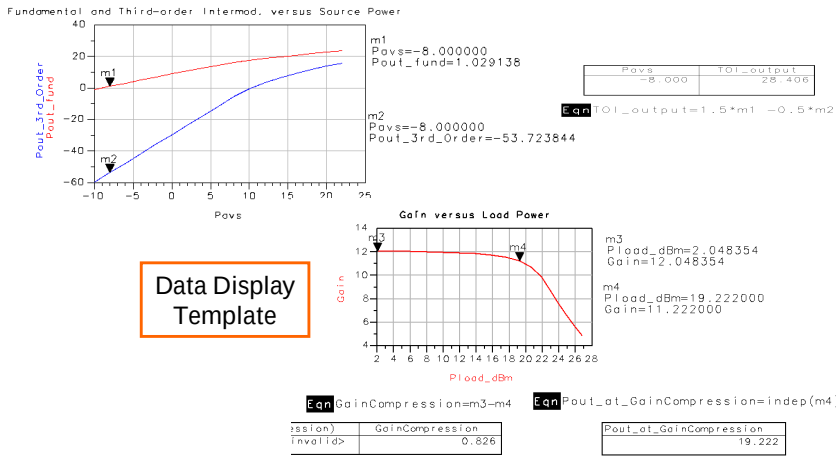
- Gain
- Gain Compression
- TOI Point
- Power-Added Efficiency
- DC Drain Current

...versus Swept Input Power

ADS 1.0 example file:
examples/RF_Board/NADC_PA_prj/PA_HB2tone

The previous amplifier was simulated again, this time using two closely-spaced input tones.

2-Tone Gain Compression, TOI

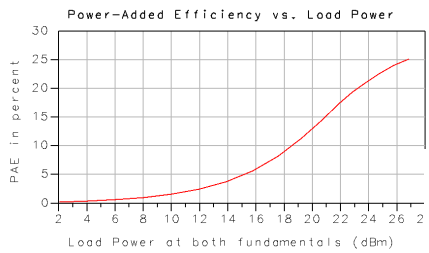


This slide shows one fundamental tones and the power in one third-order intermodulation tone versus available source power. Also depicted here is the computed TOI point using these tones, gain versus fundamental output power (for both tones), and the approximate 1-dB gain compression point. A more precise 1-dB gain compression point can be found by simply sweeping the available source power using finer resolution.

Note that 1-dB gain compression occurs at 19 dBm, which is much lower than the 27 dBm power level required for the previous single tone example. This example confirms that the gain compression point of an amplifier is highly-dependent on the signal that it amplifies. This also reveals that using a sinusoid input when simulating an amplifier may be inadequate for many applications.

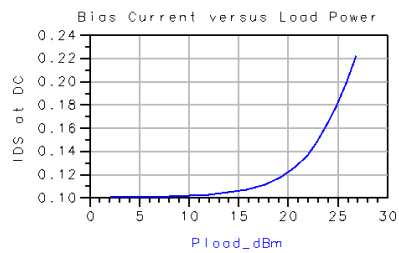
Also, different values are obtained for the TOI point when it is computed using the intermodulation distortion product versus using the third harmonic. There are several possible explanations. For starters, in the two-tone case, the output power in the desired signal is 3 dB less than in the one-tone case. For an ideal amplifier, this factor would result in a 4.5 dB reduction in the TOI point for the 2-tone case. Unfortunately, this amplifier exhibits much more reduction in the TOI point. Another consideration is the distortion generated by the amplifier, which is dependent on the source and load impedances at the beat frequency (50 kHz) in the two-tone case, but is not in the 1-tone case.

Power-Added Efficiency, Drain Current versus Output Power



2-Tone Input

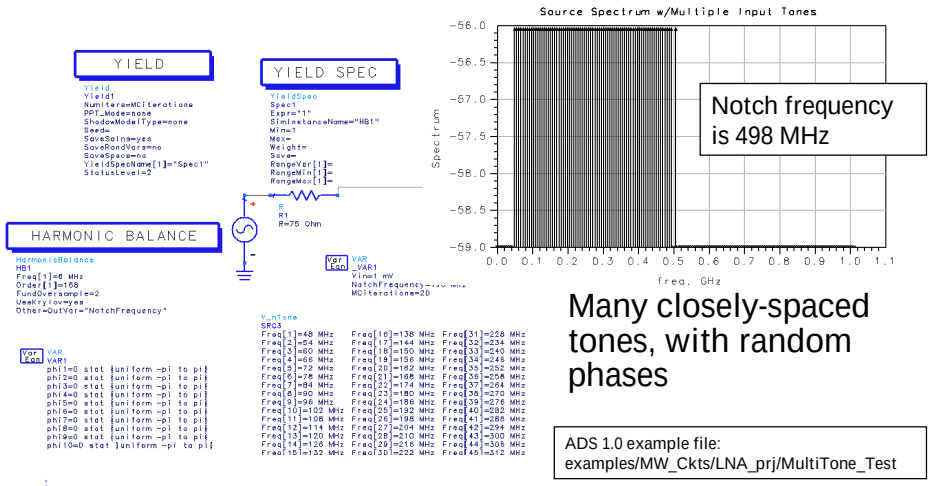
Data Display Template



This slide shows the power-added efficiency and bias current versus output power for both fundamental frequencies. The power-added efficiency in the two-tone example is 23 percent, which is somewhat lower than the 30 percent value exhibited in the one-tone example.

Multi-tone Simulation

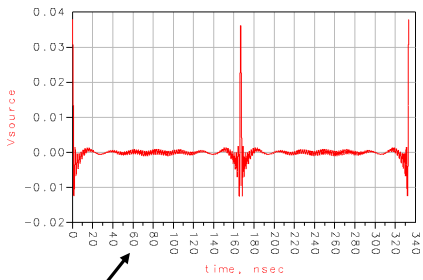
Useful for satellite and CATV amplifier testing



For simulating amplifiers for applications such as CATV (Closed Access Television) and satellites, one- or two-tone signal sources are probably not sufficient for modeling actual behavior. Thanks to improvements in our ability to solve harmonic balance equations, the ADS easily handles very large numbers of input tones without running out of memory.

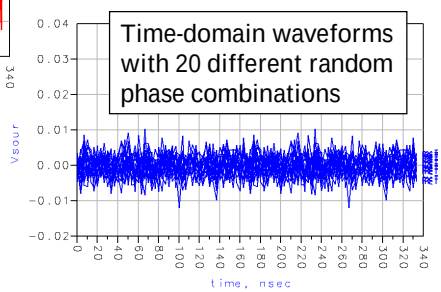
This slide shows a multitone simulation setup. In this case, 76 closely-spaced sinusoids are generated to create a test signal. The tones are evenly spaced, and the second-to-last tone is turned off to create an empty channel. Distortion in the amplifier causes an intermodulation tone to appear in the empty channel at the output, which is the result of many different mixing products that all appear at the same frequency. The noise-power ratio is then computed from the relative amplitude of the intermodulation tone, and a Monte Carlo simulation is run to randomize the relative phases of the input tones. The amplitude of the intermodulation signal changes depending on the relative phases of the input tones, as will be seen in the simulation results. Note that earlier releases of the ADS perform Monte Carlo simulation by running yield analysis with a dummy yield specification that is always satisfied.

Why Randomize Phases?



Time-domain waveform with all signals in phase

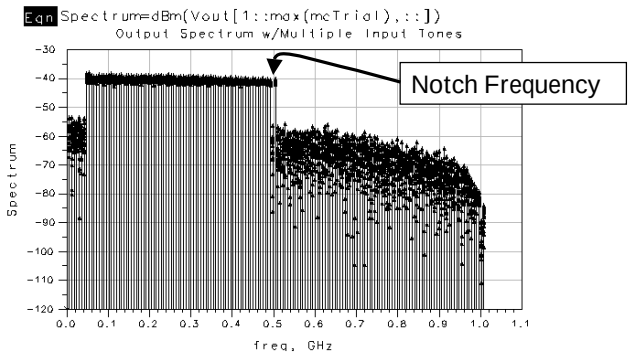
Peak-to-average power ratio is unrealistically large without randomization



Time-domain waveforms with 20 different random phase combinations

This slide reveals why the input signal phases must be randomized in multitone simulations. With all signals in phase, the generated signal exhibits an unrealistically high peak-to-average power ratio. The number of random phase combinations are controlled via the number of iterations selected for yield analysis.

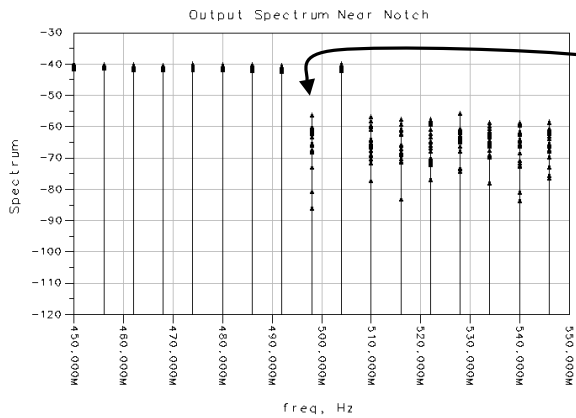
Output Spectrum



There is an empty channel (no input signal) at NotchFrequency (in this case, 498 MHz). If there were no distortion in the circuit, the depth of this notch in the output spectrum would be infinite. The smaller the depth of this notch, the greater the distortion contributed by the circuit.

This slide shows the resulting simulated output spectra of the previous multitone simulation, with source input signal phases randomized. It includes desired tones as well as those due to intermodulation distortion. The empty channel or “notch frequency” is no longer empty.

Close-Up Near Notch Frequency



The depth of the notch at the amplifier output is a measure of the added distortion.

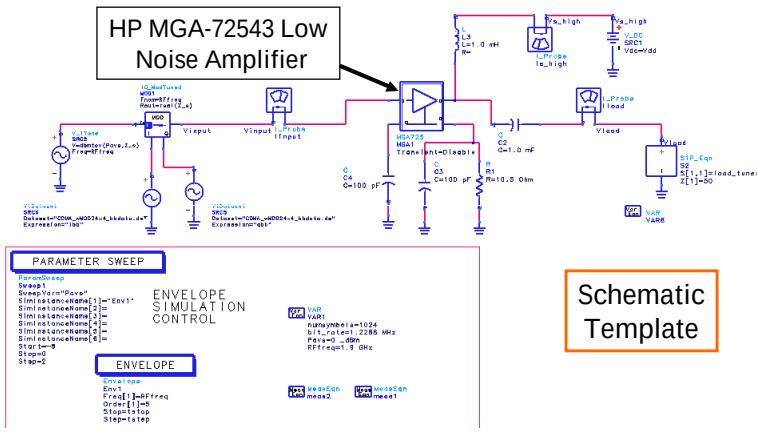
Mean-square notch depth = -21.9 dBc

The relative depth of the notch compared to desired signals in adjacent channels indicates the noise-power ratio. That is, the lower the distortion in the circuit, the greater the notch depth.

A useful reference for cable television system measurements is Jeffery L. Thomas' "Cable Television Proof-of-Performance : A Practical Guide to Cable TV Compliance Measurements Using a Spectrum Analyzer," published by Prentice Hall in 1995. Many of the examples included in the book can be simulated with the HP ADS.

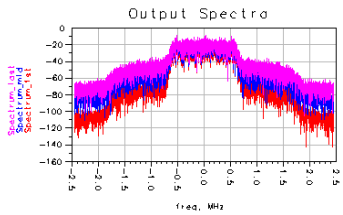
Simulation with CDMA Signal

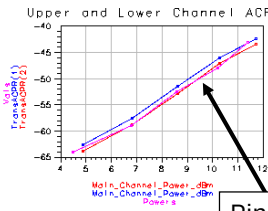
Amplifier ACPR, PAE, Pout, and Gain Simulation with a CDMA Input Signal, with an Arbitrary Swept Parameter

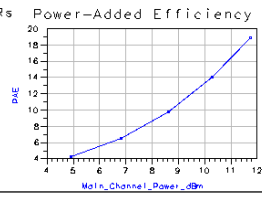


Up to this point, all of the examples have used one or more sinusoids as input signals. In this slide, a low-noise amplifier is simulated using a modulated input signal according to the reverse link requirements of IS-95. The amplifier's upper- and lower-channel adjacent-channel power ratios, main-channel power, DC power consumption, power-added efficiency, and transducer and operating power gains were all simulated versus available source input power.

CDMA Simulation Results







Pink trace is measured data

Available Source Power, dBm	DC Power Consumption, Watts	Main Channel Output Power, dBm	Power-Added Efficiency, %	Main Channel Output Power, dBm	Lower Channel ACPR, dBc	Upper Channel ACPR, dBc
-8.000	0.069	4.896	4.215	4.896	-62.619	-63.789
-6.000	0.070	6.805	6.504	6.805	-57.543	-58.773
-4.000	0.070	8.631	9.802	8.631	-51.509	-52.774
-2.000	0.072	10.289	14.066	10.289	-45.988	-47.116
0.000	0.074	11.725	18.857	11.725	-42.427	-43.421

Data Display Template

Agilent Technologies

Power AmplifierDesign with Templates, A.Howard

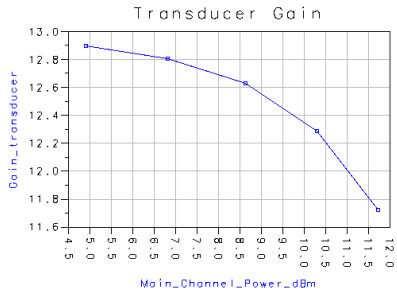
November 2000
37

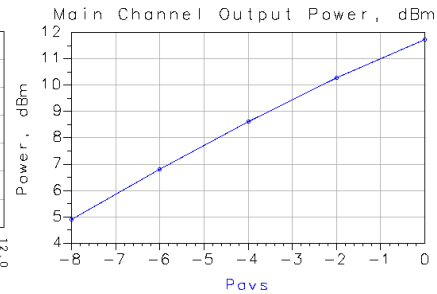
Slide 41 reveals the results of the previous simulation, which exhibit close agreement with respect to the measured data for ACPR versus output power. ACPR was measured as the ratio of power in 30 kHz bands +/-1250 kHz from the carrier frequency to the power in the main 1.2288 MHz wide channel. This simulation can be performed for any other swept parameter in the circuit—for example, bias voltage.

A similar example was presented at the Hewlett-Packard 1999 RF Design and Measurement Seminar. Using a CDMA input signal, the output power and ACPR of a different amplifier was simulated and measured. The data, which is included on pages 116 and 117 of the seminar text, reveals that the simulated output power is 11.2 dBm versus a measured value of 10.8 dBm. Simulated and measured ACPR values are <-70 dBc. In saturation, the simulated and measured ACPR values are within 1-2 dB at output power equal to 23.7 dBm (simulated) and 23.2 dBm (measured).

For another example of a measured versus modeled ACPR simulation using HP-EEsof's Circuit Envelope, see the October 1996 issue of *Microwave Journal,* "Simulation of Adjacent-Channel Power for Digital Wireless Communication Systems," by John Sevic and Joseph Staudinger.

Simulated Gain and Output Power





Main Channel Output Power, dBm	Transducer Power Gain, dB	Operating Power Gain, dB
4.896	12.896	14.978
6.805	12.805	14.910
8.631	12.631	14.782
10.289	12.289	14.528
11.725	11.725	14.105

Data Display Template

This slide reveals the resulting gain and output power from the previous simulation. The charts here show transducer power gain versus main channel output power, as well as main channel output power versus available source power. Transducer power gain is the ratio in dB of the power delivered to the load divided by the power available from the source. Similarly, operating power gain is the ratio in dB of the power delivered to the load divided by the power delivered to the amplifier.

Summary

- Templates enhance productivity via
  - Preconfigured complex simulation setups
  - Preconfigured complex data displays
  - Synthesis and optimization setups
- The Agilent Advanced Design System provides the power and flexibility to quickly develop highly-optimized solutions

ADS is an extremely powerful and flexible tool. Templates are designed to package these powerful capabilities in a format that is easy to use. They help designers carry out complex simulations and gather useful information without forcing them to become ADS experts.

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Revised: March 27, 2008

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Printed in USA, November 01, 2000
5989-9082EN

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