Presentation on Power Amplifier Design using
ADS

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Power Amplifier Design using ADS

PA Workshop

Wilfredo Rivas-Torres
Technical Support Application Engineer
October 12, 2004
Outline

• Introduction
• DC and Loadline analysis
• Bias and Stability
• LoadPull
• Matching using Smith Chart Utility
• SourcePull
• PA Characterization – Did we meet the specification?
• Optimize/Fine Tune the design
• Test Design with real world modulated signals
• Layout
Why do we need a Power Amplifier?

Power Amplifiers (PA) are in the transmitting chain of a wireless system. They are the final amplification stage before the signal is transmitted, and therefore must produce enough output power to overcome channel losses between the transmitter and the receiver.

**Basic Transmitter**
PA requirements

• The PA is typically the primary consumer of power in a transmitter. A major design requirement is how efficiently the PA can convert DC power to RF output power.

• The design engineer has to often concern himself with the Efficiency of the Power Amplifier. Notice that efficiency translates into either lower operation cost (e.g. cellular basestation) or longer battery life (e.g. wireless handheld).

• PA linearity is another important requirement, the input/ output relationship must be linear to preserve the signal integrity.

• The design of PAs often involves the tradeoff of efficiency and linearity.
PA Design Requirement

- RF Output Power: 50 W PEP
- Input Drive Level: 1 W
- Output Load (RL): 50 Ω
- Efficiency ($\eta$) > 50%
- Bias Voltage: 28 V
- Device: MRF9045M
DC Curves

FET Curve Tracer

V_DC
SRC1
Vdc=VDS

V_DC
SRC2
Vdc=VGS

VAR
VAR1
VDS =0 V
VGS =0 V

I_Probe
IDS

FSL_MRF_MET_MODEL
MRF1
MODEL=MRF9045M

Eqn
VAR
VAR1
VGS =0 V
VDS =0 V

Set drain and gate voltage sweep limits as needed.

ParamSweep
Sweep1
SweepPlan="SwpPlan1"
Start=2.5
Stop=5.0
Step=0.1

DC
DC1
SweepVar="VDS"
Start=0
Stop=28*2
Step=0.1

DisplayTemplate
disptemp1
"FET_curve_tracer"
DC Curves

Load Line

IDS.i, A

VDS

VDSat

VDsat

VGS=3.800000

IQ

VDS=28.000

IDS.i=0.717

VGS=3.800000

m3

VDS=33.400

IDS.i=0.004

VGS=2.500000

VDS=0.600

IDS.i=0.562

VGS=3.800000
Stability Analysis

**S-Parameters**

- S_Param
  - SP2
  - Start=1 MHz
  - Stop=3000 MHz
  - Step=1.0 MHz

**FSL_Tech_Include**

- FTI
  - MuPrime
    - MuPrime1=mu_prime(S)
  - Mu
    - Mu1=mu(S)
  - StabFact
    - StabFact1=stab_fact(S)
  - StabMeas
    - StabMeas1=stab_meas(S)
  - MuPrime
    - MuPrime1=mu_prime(S)

**Stabilization Measures**

- StabFact1=stab_fact(S)
- StabMeas1=stab_meas(S)
- Mu1=mu(S)
- MuPrime1=mu_prime(S)

**Circuit Diagram**

- Power Amplifier MRF9045M_Amp with X1
- Term R3

**Ports and Connections**

- P_1Tone
  - PORT1
  - Num=1
  - Z=50 Ohm
  - P=polar(dbmtow(-60),0)
  - Freq=fss

- VDD
  - VGG
  - Z=50 Ohm
  - Num=2
  - Z=50 Ohm

- V_DC
  - SRC1
    - Vdc=VGS
  - SRC2
    - Vdc=VDS

- I_Probe
  - IDD
  - I_Probe
  - IGG

- V_DD
  - VGG

**Component Values**

- VGS = 3.8 V
- VDS = 28 V
- VGS = 3.8 V

**Design Details**

- ADS Power Amp Design
Stability Analysis

freq, GHz
Impedance Matching

• The need for matching circuits is because amplifiers, in order to perform in a certain way (e.g. maximize output power), must be presented with a certain impedance at both the load and the source ports.

• For example in order to deliver maximum power to the load $R_L$ the transistor must have termination $Z_s$ and $Z_L$.

• The input matching network is designed to transform the generator impedance $R_s$ to the optimum source impedance $Z_s$.

• The output matching network transform the load termination $R_L$ (50 Ω) to the optimum load impedance $Z_L$.

• A LoadPull measurement will help the designer determine the optimum load impedance $Z_L$. 
LoadPull Setup

PARAMETER SWEEP
- Param Sweep
- Sweep2

HARMONIC BALANCE
- Harmonic Balance
- HB1
  - Freq[1]=RFfreq
  - Order[1]=15

Set Load and Source impedances at harmonic frequencies
- VAR
  - VAR2
    - Z_1.2 = Z0 + j*0
    - Z_1.3 = Z0 + j*0
    - Z_1.4 = Z0 + j*0
    - Z_1.5 = Z0 + j*0
    - Z_s_fund = 1.0 + j*0
    - Z_s_2 = Z0 + j*0
    - Z_s_3 = Z0 + j*0
    - Z_s_4 = Z0 + j*0
    - Z_s_5 = Z0 + j*0

Set these values:
- VAR
  - STIMULUS
    - Pavs=30 dBm
    - RFfreq=760 MHz
    - Vhigh=28.0
    - Vlow=3.8
LoadPull Contours

m2
indep(m2)=6
Pdel_contours_p=0.914 / 171.170
level=44.195857, number=1
impedance = 2.265 + j3.852

m1
indep(m1)=6
PAE_contours_p=0.914 / 171.180
level=47.552308, number=1
impedance = 2.265 + j3.848
Matching using Smith Chart Utility
Matching using Smith Chart Utility

![Smith Chart Utility Interface](image)
Output Match

Port P1
Num=1

Port P2
Num=2

TLIN TL1
Z=50 Ohm
E=8.891
F=760 MHz

TLIN TL2
Z=50 Ohm
E=32.25
F=760 MHz

TLIN TL3
Z=22.85 Ohm
E=25.92
F=760 MHz

C C1
C=12.975203 pF

C C2
C=2.307137 pF

C C3
C=27.689016 pF

DA_SmithChartMatch1_output_match_design
DA_SmithChartMatch1
F=760 MHz
Zs=50 Ohm
Zl=(2.300-j*3.800) Ohm
Z0=50 Ohm
**SourcePull Contours**

- **m2**
  - indep(m2)=4
  - Pdel_contours_p=0.960 / 174.023
  - level=46.038749, number=1
  - impedance = 1.016 + j2.609

- **m1**
  - indep(m1)=4
  - PAE_contours_p=-0.952 + j0.100
  - level=58.130703, number=1
  - impedance = 1.096 + j2.618
Complete Design Power Sweep

\[
V_{\text{load}} \quad \text{input_match} \quad X5 \quad \text{MRF9045M_AMP} \quad X4 \quad \text{output_match} \quad X3
\]

\[
I_{\text{load}} \quad R \quad R=50 \text{ Ohm}
\]

\[
\text{VAR} \quad \text{VAR1} \quad \text{VDS}=28 \text{ V} \quad \text{VGS}=3.8 \text{ V} \quad \text{Pin}=30
\]

\[
\text{fo}=760.0 \text{ MHz}
\]

\[
P_{1\text{Tone}} \quad \text{PORT1} \quad \text{Num}=1 \quad Z=50.0 \text{ Ohm} \quad P=\text{dbmto}w(\text{Pin}) \quad \text{Freq}=\text{fo} \quad \text{Vdc}=
\]

\[
V_{\text{DC}} \quad \text{SRC1} \quad V_{\text{dc}}=V_{\text{DS}}
\]

\[
V_{\text{DC}} \quad \text{SRC2} \quad V_{\text{dc}}=V_{\text{GS}}
\]

\[
\text{HARMONIC BALANCE}
\]

\[
\text{HARMONIC BALANCE} \quad \text{HB1} \quad \text{Freq}[1]=\text{fo} \quad \text{Order}[1]=15 \quad \text{SweepVar}="\text{Pin}" \quad \text{Start}=-30 \quad \text{Stop}=40 \quad \text{Step}=1
\]

\[
\text{FSL\_TECH\_INCLUDE} \quad \text{FTI}
\]

\[
\text{Agilent Technologies}
\]
Power Compression Curve

Output
Pin=30.000
Pdel_dBm=45.570

Output Pin= Pdel_dBm=45.570

Pin
Pdel_dBm
Gain Compression Curve

LinearGain
Pin=-30.000
Gp=17.341

GainComp
ind Delta=60.00
dep Delta=-1.771
delta mode ON

Pin
Gp

ADS Power Amp Design
Page 21
Power Added Efficiency

m1
Pin=30.000
PAE=49.618
Getting ready to Optimize the PA

• The next step is to optimize the design to meet the requirements.
• The Designer can take the opportunity to see if other requirements, such as layout will require any changes before proceeding to optimize.
• Example: we notice that the transistor pads are rather wide and the Tlines leading up to it are not the same width.
• Since the Tlines are much narrower, we could add a taper so we have a nice transition.
• We included a MTAPER at the input and output side

MTAPER
Taper2
Subst="MSub1"
W1=199.971654 mil
W2=63.670079 mil
L=100.0 mil

<table>
<thead>
<tr>
<th>dBm(Vload[1])</th>
</tr>
</thead>
<tbody>
<tr>
<td>41.549</td>
</tr>
</tbody>
</table>
## Optimization Setup

<table>
<thead>
<tr>
<th>Optim</th>
<th>GOAL</th>
<th>GOAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Optim</td>
<td>Goal</td>
<td>Goal</td>
</tr>
<tr>
<td>Optim1</td>
<td>Goal1</td>
<td>Goal2</td>
</tr>
<tr>
<td>OptimType=Gradient</td>
<td>Expr=&quot;dBm(Vload[1])&quot;</td>
<td>Expr=&quot;dBm(Vload[2])-dBm(Vload[1])&quot;</td>
</tr>
<tr>
<td>MaxIters=25</td>
<td>SimInstanceName=&quot;HB1&quot;</td>
<td>SimInstanceName=&quot;HB1&quot;</td>
</tr>
<tr>
<td>DesiredError=0.0</td>
<td>Min=47.0</td>
<td>Min=</td>
</tr>
<tr>
<td>FinalAnalysis=&quot;None&quot;</td>
<td>Max=</td>
<td>Max=-40</td>
</tr>
<tr>
<td>NormalizeGoals=no</td>
<td>Weight=</td>
<td>Weight=</td>
</tr>
<tr>
<td>SetBestValues=yes</td>
<td>RangeVar[1]=</td>
<td>RangeVar[1]=</td>
</tr>
<tr>
<td>SaveSolns=yes</td>
<td>RangeMin[1]=</td>
<td>RangeMin[1]=</td>
</tr>
<tr>
<td>SaveGoals=yes</td>
<td>RangeMax[1]=</td>
<td>RangeMax[1]=</td>
</tr>
<tr>
<td>SaveOptimVars=no</td>
<td></td>
<td></td>
</tr>
<tr>
<td>UpdateDataset=yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SaveNominal=no</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SaveAllIterations=no</td>
<td></td>
<td></td>
</tr>
<tr>
<td>UseAllOptVars=yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>UseAllGoals=yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SaveCurrentEF=no</td>
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<td></td>
</tr>
</tbody>
</table>
## Optimization Results

<table>
<thead>
<tr>
<th>InitialEF</th>
<th>FinalEF</th>
</tr>
</thead>
<tbody>
<tr>
<td>67.187</td>
<td>0.000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>optIter</th>
<th>Goal1</th>
<th>Goal2</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>47.003</td>
<td>-40.017</td>
</tr>
</tbody>
</table>

**Before**

MLIN
TL39
Subst="MSub1"
W=63.670079 mil
L=2194.444882 mil opt{ 250 mil to 3500 mil }

**After**

MLIN
TL39
Subst="MSub1"
W =63.670079 mil
L =551.591 mil opt{ 250 mil to 3500 mil }
## Optimization Values

<table>
<thead>
<tr>
<th>TL39.L*1e5/2.54</th>
<th>TL15.L*1e5/2.54</th>
<th>TL7.L*1e5/2.54</th>
</tr>
</thead>
<tbody>
<tr>
<td>551.591</td>
<td>247.144</td>
<td>320.449</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TL30.L*1e5/2.54</th>
<th>TL8.L*1e5/2.54</th>
</tr>
</thead>
<tbody>
<tr>
<td>814.900</td>
<td>622.341</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TL31.L*1e5/2.54</th>
<th>TL9.L*1e5/2.54</th>
</tr>
</thead>
<tbody>
<tr>
<td>202.643</td>
<td>248.635</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TL32.L*1e5/2.54</th>
<th>TL10.L*1e5/2.54</th>
</tr>
</thead>
<tbody>
<tr>
<td>184.709</td>
<td>244.711</td>
</tr>
</tbody>
</table>
PA Results

![Graph showing PA Results]

- **Pin**: 30.000
- **Pdel_dBm**: 47.003
Power Added Efficiency

\[ \text{Pin} = 30.000 \]
\[ \text{PAE} = 56.736 \]
Gain Compression Curve

m4
Pin=30.000
Gp-Gp[0]=-0.728
Complex Modulated Signal

16 QAM Spectrum (dBm)

Frequency (MHz)

759.50 759.75 760.00 760.25 760.50

0 -20 -40 -60 -80 -100

759.75 760.00 760.25 760.50

Agilent Technologies
16 QAM Modulated Source

SymbolConverter S3
SymbolTime=2/bit_rate
Delay=0 sec
CodeIn=nrzIn
CodeOut=pam4Out

SymbolConverter S4
SymbolTime=2/bit_rate
Delay=0 sec
CodeIn=nrzIn
CodeOut=pam4Out

LPF_RaisedCosineTimed L4
Loss=0.0
CornerFreq=bit_rate/8
ExcessBw=0.5
Type=Model with pulse equalization
SquareRoot=Yes
Delay=16/bit_rate

SymbolConverter S5
SymbolTime=1/bit_rate
Delay=-1

SymbolConverter S6
SymbolTime=1/bit_rate
Delay=0 sec
CodeIn=nrzIn
CodeOut=pam4Out

SymbolConverter S7
SymbolTime=1/bit_rate
Delay=0 sec
CodeIn=nrzIn
CodeOut=pam4Out

SymbolConverter S8
SymbolTime=0 sec

SymbolConverter S9
SymbolTime=2/bit_rate
Delay=0 sec
CodeIn=nrzIn
CodeOut=pam4Out

LPF_RaisedCosineTimed L6
Loss=0.0
CornerFreq=bit_rate/8
ExcessBw=0.5
Type=Model with pulse equalization
SquareRoot=Yes
Delay=16/bit_rate

SymbolSplitter S1
SymbolTime=1/bit_rate
Delay=-1

SymbolSplitter S2
SymbolTime=1/bit_rate
Delay=-1

SymbolSplitter S3
SymbolTime=1/bit_rate
Delay=-1

SymbolSplitter S4
SymbolTime=1/bit_rate
Delay=-1
DSP and Analog Circuits Setup

• Create a subcircuit with your analog design.
• You need to add either Circuit Envelope or Transient controller to the analog circuit.
• We use Circuit Envelope specifically with our PA since we have a Modulated Carrier.
• Circuit Envelope will also allow the use of Fast Cosim (Automatic Verification Modeling – AVM). This will dramatically increase the simulation speed.
• In the DSP schematic we will create the Modulated Carrier, feed it to the PA and collect the signal samples and spectrum.
• The DSP schematic contains a Envelope Output Selector component used for interfacing between circuit subnetwork output and the signal processing components.
Fast Cosim Improvements

Simulation Time Benchmark:
Total bits: 1024 bits
AVM disabled: 410 sec
AVM enabled: 13 sec
AVM data reuse: 5.5 sec
AVM data reuse (16 Kbits): 17.5 sec
Cosimulation Results - Spectrum

Carrier Power
25 dBm

Carrier Power
30 dBm
Cosimulation Results - Constellation

Carrier Power
25 dBm

Carrier Power
30 dBm
## Cosimulation Results

### Carrier Power 30 dBm

<table>
<thead>
<tr>
<th>peakP_in</th>
<th>peak_avg_in</th>
<th>avgPin</th>
</tr>
</thead>
<tbody>
<tr>
<td>32.163</td>
<td>4.951</td>
<td>27.212</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>peakP_out</th>
<th>peak_avg_out</th>
<th>avgPout</th>
</tr>
</thead>
<tbody>
<tr>
<td>47.969</td>
<td>3.516</td>
<td>44.453</td>
</tr>
</tbody>
</table>

### Carrier Power 25 dBm

<table>
<thead>
<tr>
<th>peakP_in</th>
<th>peak_avg_in</th>
<th>avgPin</th>
</tr>
</thead>
<tbody>
<tr>
<td>30.000</td>
<td>7.788</td>
<td>22.212</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>peakP_out</th>
<th>peak_avg_out</th>
<th>avgPout</th>
</tr>
</thead>
<tbody>
<tr>
<td>44.715</td>
<td>4.832</td>
<td>39.883</td>
</tr>
</tbody>
</table>
Cosimulation Results – CCDF

Carrier Power
25 dBm

Carrier Power
30 dBm
EVM vs. Power Measurement

VAR
VAR3
Tstep=1/\text{bit\_rate*oversample)}
Tstop=\text{num\_bits/bit\_rate}
F_c=760 \text{ MHz}
\text{Pow}=30 \text{ dBm}

VAR
VAR2
\text{bit\_rate}=1.0 \text{ MHz}
oversample=4
\text{num\_bits}=4096*4

\text{Eqn}
\text{Var}
\text{VAR}
\text{VAR2}
\text{num\_bits}=4096*4
\text{oversample}=4
\text{bit\_rate}=1.0 \text{ MHz}

\text{Eqn}
\text{Var}
\text{EVM\_WithRef}
\text{Ref test}
\text{EVM  Ref}

\text{RES}
\text{R2}
\text{R}=50 \text{ Ohm}

\text{PARAMETER SWEEP}
\text{DF}
\text{DF1}
\text{SavedEquationName}[1]="Tstep"
\text{DefaultTimeStop}=Tstop
\text{DefaultTimeStart}=0
\text{DefaultNumericStop}=100
\text{DefaultNumericStart}=0

\text{QAM\_src}
\text{X2}
P_c=\text{Pow}

\text{PARAMETER SWEEP}
\text{DF}
\text{DF1}
\text{SweepVar}=\"\text{Pow}\"
\text{SimInstanceName}[1]="\text{DF1}"
\text{SimInstanceName}[2]=
\text{SimInstanceName}[3]=
\text{SimInstanceName}[4]=
\text{SimInstanceName}[5]=
\text{SimInstanceName}[6]=
\text{Start}=18
\text{Stop}=30
\text{Step}=1

\text{RES}
\text{R1}
\text{R}=50 \text{ Ohm}

\text{EnvOutShort}
\text{O1}
\text{OutFreq}=F_c

\text{MRF9045M\_AMP\_CE2}
\text{X1}

\text{DF}
\text{DF1}
\text{DefaultNumericStart}=0
\text{DefaultNumericStop}=100
\text{DefaultTimeStart}=0
\text{DefaultTimeStop}=Tstop
\text{SavedEquationName}[1]="Tstep"

\text{EVM\_WithRef}
\text{E2}
\text{StartSym}=10
\text{SymBurstLen}=1024
\text{SampPerSym}=16
\text{SymDelayBound}=-1
\text{NumBursts}=2
\text{MeasType}=\text{EVM\_rms}
\text{SymbolRate}=0.25 \text{ MHz}
EVM vs. Power Results

EVM vs. Carrier Power

EVM (%) vs. Power (dBm) graph
### ADS to VSA link

**QAM18 Source**
- QAM_src
- X2
- \( P_c = Pow \)

**MRF9045M_AMP_CE2**
- Env OutShort
- O1
- OutFreq=Fc

**ENV**
- OutShort

**RES**
- R1
- R=50 Ohm

**VSA_89600_1_Sink**
- VSATitle="Simulation output"
- TStep=Tstep
- SamplesPerSymbol=16
- SetupFile="C:\Program Files\Agilent\89600 VSA\Vector\User\PA_demod.set"
- SetFreqProp=YES

**FSL_TECH_INCLUDE**
- FTI

**DF**
- DefaultNumericStart=0
- DefaultNumericStop=100
- DefaultTimeStart=0
- DefaultTimeStop=Tstop
- SavedEquationName[1]="Tstep"

**VAR3**
- \( T_{step} = \frac{1}{(bit\_rate \times oversample)} \)
- \( T_{stop} = \frac{num\_bits}{bit\_rate} \)
- \( F_c = 760 \text{ MHz} \)
- \( Pow = 30 \text{ _dBm} \)

**VAR2**
- bit_rate=1.0 MHz
- oversample=4
- num_bits=1024*16
VSA Spectrum from ADS Cosim

B: Ch1 Spectrum

Range: 10 dBm

Left: 759 MHz
RBW: 76.2932 Hz

Right: 761 MHz
TimeLen: 19.661 mSec
VSA Constellation from ADS Cosim

Carrier Power
30 dBm
VSA Constellation from ADS Cosim

Carrier Power
30 dBm
## VSA EVM from ADS Cosim

**Carrier Power**

30 dBm

<table>
<thead>
<tr>
<th>Metric</th>
<th>Value 1</th>
<th>Unit</th>
<th>Value 2</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>EVM</td>
<td>4.1676</td>
<td>%rms</td>
<td>12.719</td>
<td>% pk at sym</td>
</tr>
<tr>
<td>Mag Err</td>
<td>3.1291</td>
<td>%rms</td>
<td>-11.221</td>
<td>% pk at sym</td>
</tr>
<tr>
<td>Phase Err</td>
<td>2.6647</td>
<td>deg</td>
<td>-11.881</td>
<td>deg pk at sym</td>
</tr>
<tr>
<td>Freq Err</td>
<td>5.1206</td>
<td>mHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IQ Offset</td>
<td>-65.85</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Quad Err</td>
<td>94.065</td>
<td>mdeg</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| SNR(MER)   | 25.051  | dB   |
| Gain Imb   | 0.01    | dB   |

Time: 27
PA Layout
Other Possibilities

• Run an EM Cosimulation – include layout effects in the simulation. Optimize design if necessary.

• Run Loadpull for IP3 or ACPR. The optimum load would then be a compromise between all the requirements.

• Use Connection Manager and real PA to validate design and compare vs. simulated results.

• Create a behavioral data model that can be used to protect you IP yet give access to your design results.

If there is any topic about PA Design and ADS you wish to discuss email me: wilfredo_rivas-torres@agilent.com