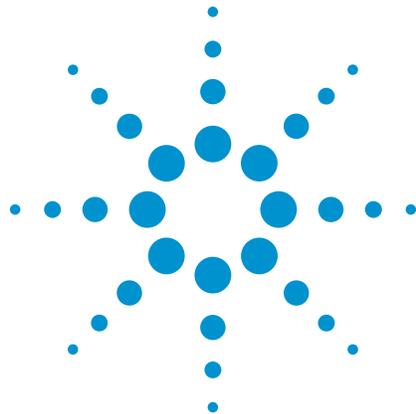


Identifying the Causes of DDR Data Corruption and Elusive Failures

Tutorial

Track Infrequent Errors-Glitch, Overshoot, etc.



There are times when tracking infrequent errors or events can be challenging because they do not happen regularly. What if a glitch happens once every 5 minutes and can only be observed in infinite persistence display mode? Without the ability to track it, the condition when the glitch happens cannot be fully understood. Some other scenarios include signal overshoot due to crosstalk when the adjacent signal transition or ISI failure is due to a specific DQ pattern.



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The InfiniiScan zone qualify trigger is a tool that can help you to track the signals. If the event can be observed, it can be tracked. You can set a tracking condition by drawing a “must intersect” or “must not intersect” zone directly on your signal on the oscilloscope screen. This allows you to easily isolate the signal of interest and track a specific error or event. Some examples can be observed in Figure 1 and 2.

Using a logic analyzer with a memory bus decoder provides extensive triggering and storage qualifications for protocol decode of memory transactions. The DDR protocol-decode software in the logic analyzer allows users to input system attributes such as burst length, CAS and additive latency, as well as chip selects to decode the key DDR bus signals. Using these attributes, the software then presents a display that lists the transaction type, address, data and command conditions. Protocol-decode software also supports user-defined symbols that can be easily added to the state listing display. This software allows you to decode and view transactions, commands, and data from a DDR2 or DDR3 memory bus in your target system. This combination provides memory bus triggering, debug and compliance verification measurements to help you find protocol violations within your system such as read or write to an interactive bank row, refresh command to an active bank, or bank row must be pre-charged before being activated. The data is decoded and displayed at any desired level of detail from the protocol to binary. The protocol-decode software then translates acquired signals into easily understood bus transactions, at the full bus speed.



Figure 1: A “Must Intersect” zone is used to track an infrequent glitch on the clock signal.



Figure 2: Using the InfiniiScan zones, a condition is set to track a specific DQ pattern of “01000010101”

Using colored filters helps zoom into a protocol error quickly: missing BI activate (turquoise) indicated that bank 1 is not activated before the read command is issued

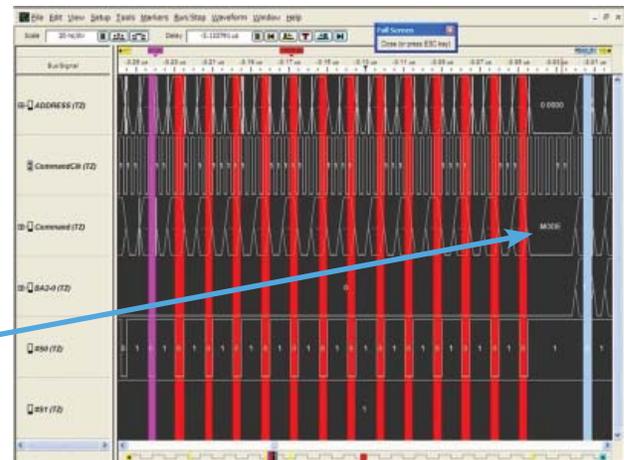


Figure 3. Using colored filters on the command signal can help detect missing commands that indicate a protocol violation.

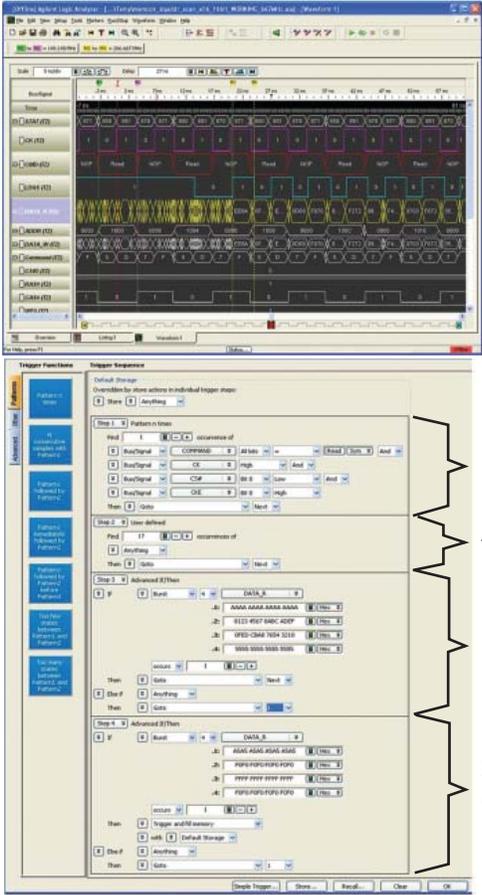


Figure 4. Use the advanced triggering features of the logic analyzer to check for data mismatches for bit error rate measurements.

The Protocol-decode software allows you to track and fix infrequent glitches and other signal anomalies that might otherwise be difficult to find.

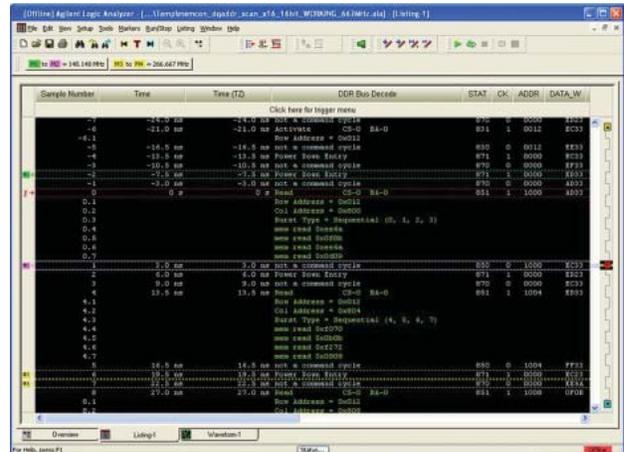


Figure 5. The DDR protocol decoder software provides memory bus decode in an intuitive, consolidated format, eliminating time consuming and tedious review of the waveform traces.

Publication name	Publication type	Publication number
DDR Memory Overview, Development Cycle and Challenges	Tutorial	5990-3180EN
DDR Design and Verification through Simulation	Tutorial	5990-3317EN
DDR Probing for Physical Layer and Functional Testing	Tutorial	5990-3182EN
Debugging Signal Integrity and Protocol Layers on DDR Designs	Tutorial	5990-3189EN
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