Conventional Methods of Separation

To analyze the signal integrity of DDR signals, you need to differentiate the complex traffic on the data bus to independently analyze the signal performance for both DDR chip and memory controller.

Read and write data transfers are bi-directional on the same data bus (see Figure 1), making DDR validation a challenge. Read data transfer comes from the DRAM chip, while write data comes from the memory controller. When neither is transmitting, the bus reverts to high-impedance state. Unfortunately traditional methods used to separate read/write signals offer varying degrees of reliability.

Figure 1. Read and write data transfers use the same data bus. The read signal aligns with the strobe edges whereas the write signal straddles it.
Trigger on Read-Write Preamble Width

In some cases, you can isolate the data signals by triggering on the read or write preamble width. From the DDR specification, the read preamble width ranges from 0.4 to 0.6 of the clock period. The write preamble width is specified to be larger than 0.35 of the clock period but has no upper limit. Thus, you need to first determine the preamble width before setting the trigger condition. If the preamble widths are distinctive, then the method can separate read and write data; however this method has weaknesses.

First, because the Joint Electronic Devices Engineering Council (JEDEC) loosely defines these widths, the width varies with different ASIC/DIMM vendors. Also, since the upper limit of the write preamble is not defined, it could have the same width as the read preamble. If these values are too close, separating the read-write signal will be difficult.

Second, the write signal with a preamble of 0.5 clock cycle has a width similar to that for one data bit period. When this occurs the hardware trigger cannot differentiate the write preamble bit from the normal bit.

Third, as the DDR data rate gets faster, the clock period gets narrower. Thus, the preamble width will be greatly reduced for the write signal. For example, the minimum preamble width for DDR3-1600 is about 200 ps. The oscilloscope may not be able to trigger on such a narrow pulse width.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>DDR2-667 min</th>
<th>DDR2-667 max</th>
<th>DDR2-800 min</th>
<th>DDR2-800 max</th>
<th>Units</th>
<th>Specific Notes</th>
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<tr>
<td>Write preamble</td>
<td>tWPRE</td>
<td>0.35</td>
<td>x</td>
<td>0.35</td>
<td>x</td>
<td>tCK(avg)</td>
<td></td>
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<tr>
<td>Read postamble</td>
<td>tRPST</td>
<td>0.4</td>
<td>0.6</td>
<td>0.4</td>
<td>0.6</td>
<td>tCK(avg)</td>
<td>19.42</td>
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</table>

Table 1. The read and write preamble width from the JEDEC specification shows they overlap, making it unreliable to use them to separate read and write signals.
Trigger on Amplitude

Typically the read and write signals have different amplitudes. You can therefore isolate them by triggering on the signal with the larger amplitude. However, the larger amplitude is not exclusive to the read or write signal.

Although you can trigger on the larger signal, you cannot choose whether this is the read or write signal, so you can only analyze the signal with larger amplitude. This could be a problem if the read and write signals have similar amplitude levels.

Innovative method for separation

Many engineers are frustrated with conventional methods for separation, because they spend considerable time setting up their scopes to isolate read and write signals and still find consistency and repeatability unacceptably low.

Figure 3. You may be able to separate the read and write signals based on signal amplitude. In the example, the read amplitude is slightly higher than the write. Thus you could only separate out the read, but not the write signals.
Trigger on Zones with InfiniiScan

To quickly and reliably separate read and write signals on a high-speed, bi-directional bus, you may need a new capability: InfiniiScan, available on Keysight Technologies, Inc. oscilloscopes. InfiniiScan provides zone triggering, enabling the scope to separate read and write cycles based on the distinctive pattern of the waveforms.

The InfiniiScan zone trigger lets you draw zones on the oscilloscope screen to visually determine the event identification condition. With the zone trigger capability, you can track a signal of interest depending on whether the waveform intersects or does not intersect the zones.

The DDR signal (see Figure 4, top) shows a distinctive read and write signal pattern in infinite persistence mode. No silicon signals have similar electrical characteristics, which explains the difference in the signal pattern on the DQS signal. In addition, you can observe the DDR waveforms in different states, allowing you to take away the signal condition that you do not want to observe. This ensures that you are triggering on the correct signals.

In Figure 4, the DQS waveform is the yellow waveform and the DQ waveform is green. When the hardware edge trigger is set on the DQS signal, the DQ shows that the read and write signal pattern overlap each other. Using the zone trigger, you can draw zones to easily separate the read and write patterns using the zone trigger feature. To be able to identify a read or write burst, you can check the edge relationship between the DQS and DQ edges. For read bursts, the edges of DQS and DQ are aligned; for write bursts DQS is centered on DQ.

Figure 3. You may be able to separate the read and write signals based on signal amplitude. In the example, the read amplitude is slightly higher than the write. Thus you could only separate out the read, but not the write signals.
When working with a logic analyzer, the method of separating the read and write signals is based on the clock alignment. Because the read signal is aligned with the edge of the clock and the write signal is aligned with the center, the signals can be separated for viewing. The logic analyzer’s dual sample mode architecture enables read and write data to be sampled at different times. By setting the thresholds of your signals, you can see the read and write signals in different windows.

Using InfiniiScan software and dual sample mode, designers and engineers can alleviate the difficulties of triggering on read or write data and enjoy faster debug and greater insight into performance.

For more detailed instructions on analyzing your DDR signals see Application Note 1591: A Time-Saving Method for Analyzing Signal Integrity in DDR Memory Buses.
Related Literature

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<th>Publication title</th>
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<th>Publication number</th>
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<td>DDR Memory Overview, Development Cycle and Challenges</td>
<td>Application Note</td>
<td>5990-3180EN</td>
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<tr>
<td>DDR Design and Verification through Simulation</td>
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<td>Ensuring Compliance and Interoperability in DDR Designs</td>
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<td>5990-3324EN</td>
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