

Debugging Signal Integrity and Protocol Layers on DDR Designs

Tutorial

As DDR data transmission rates increase, signal integrity and clarity become critical concerns. So one of the primary challenges with DDR is debugging failures. Engineers and designers need to find the root cause of failures to fix problems. Using the right tools can save considerable time when you need to identify and troubleshoot issues. Without effective tools, finding the source of problems can take days or weeks – pushing back project schedules and time to market.

A wide eye opening suggests good signal integrity

Inactivity indicates a dead bit or bad signal connection

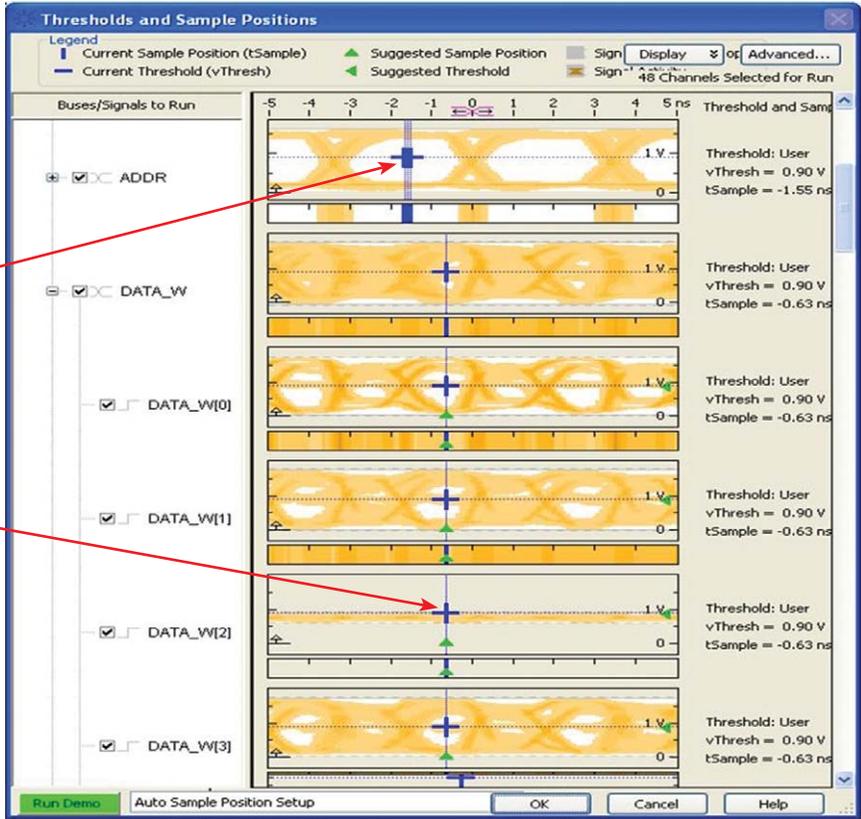


Figure 1. Identify problem signals quickly by viewing eye diagrams across all buses and signals simultaneously

Debugging Eye-Diagram Failures

The logic analyzer's Eye Scan feature allows you to quickly identify problem signals by simultaneously viewing eye diagrams across all DRAM buses. Expand the bus to find the signal(s) impacting the eye, then conduct further parametric analysis with a scope. Eye scan provides a graphical view of the signal behavior from both horizontal and vertical scans. You may set the thresholds and sample positions to help position the logic analyzer's setup/hold window (or sampling position) and specify the threshold voltage. This ensures that the data on high-speed buses is captured accurately – in other words, that the data is sampled when it is valid.

Once the worst eye is found on the DRAM buses, you can then use the oscilloscope to further look at the signal or debug if there's an issue. Using this methodology, you can save a lot of time compared to looking at each of the signals with an oscilloscope.

After locating the worst eye, you can then connect the signal to the oscilloscope to perform eye-diagram analysis. Since oscilloscopes provide more resolution than the logic analyzer, you can see the signal integrity performance of your signal more clearly. The mask can be configured based on the JEDEC requirement, so when the eye violates the mask you know there is an issue with your signal. If the signal violates the mask, the mask unfolding feature lets you unfold the composite eye-diagram. After unfolding, the scope will pinpoint the exact location where the violation occurs. If there is more than one violation in a waveform, you can navigate through each of the failure positions. To find the root cause, you then measure the timing relationships between signals when the violation occurs or examine the DQ pattern if the failure is related to intersymbol interference (ISI).

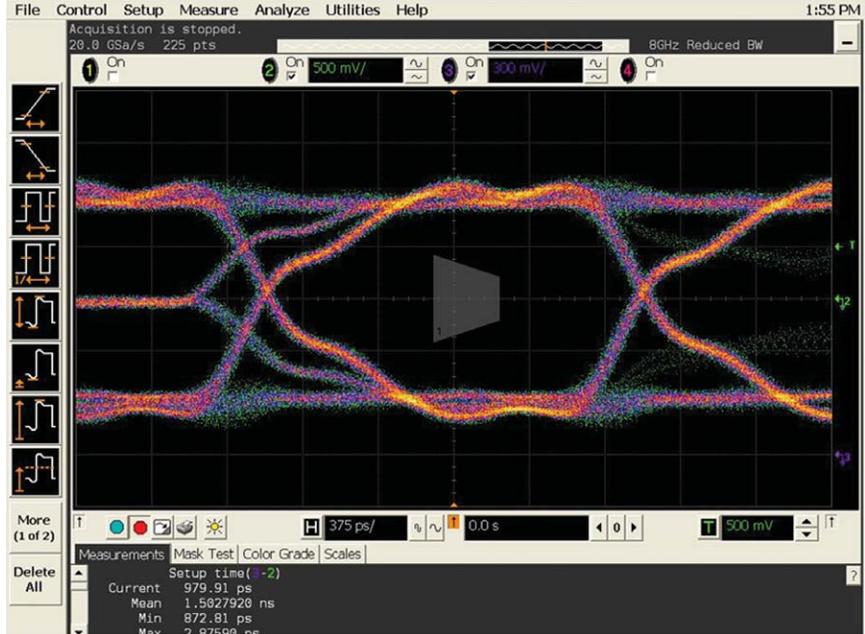


Figure 2. Perform eye diagram analysis of the signal on the oscilloscope to view signal integrity performance.

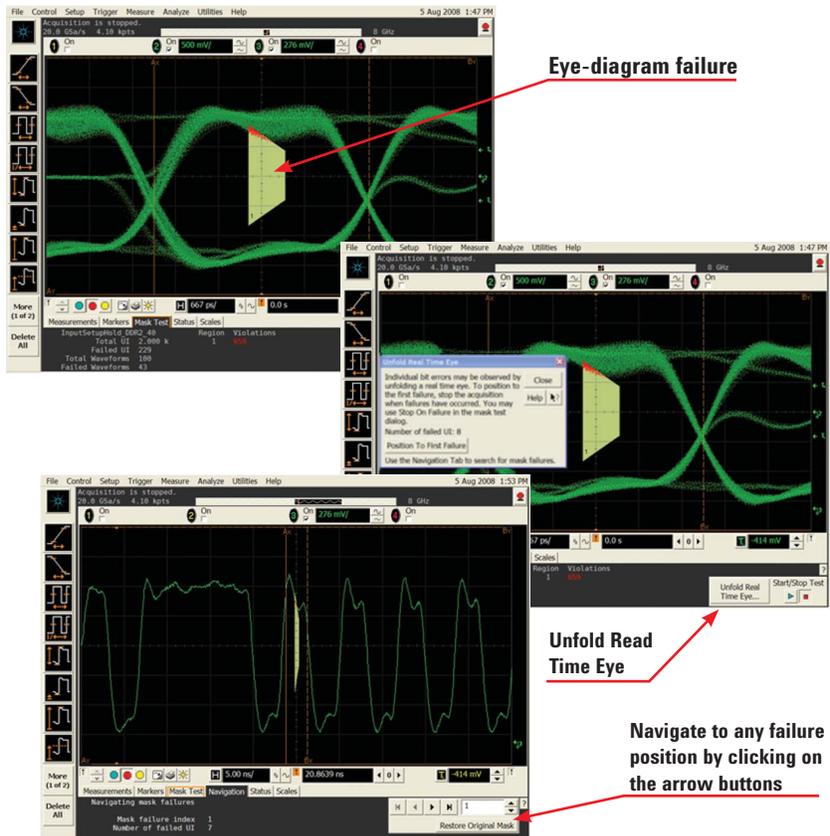


Figure 3. Mask unfolding pinpoints the waveform that violates the eye-diagram and allows further analysis of the failure.

Debugging jitter and identifying the source

The Joint Electronic Devices Engineering Council (JEDEC) specifications have strict jitter requirements for the clock. To qualify, the clock must pass a long list of jitter tests. With automated DDR software, the jitter measurements can be carried out more efficiently and effectively.

Many different sources of jitter can cause failure. On-board oscillators and power supplies can couple into the high-speed clock signal. Intra-lane skew in differential clock can cause duty-cycle distortion (DCD). Components used in design may contribute white noise that results in failures. Without a way to pinpoint the source of the jitter, figuring out the cause of failures can prove daunting.

Agilent's EZJIT tool can make it simpler. Using the Agilent EZJIT tool, you can view the clock time interval error (TIE) in the histogram, jitter trend and jitter spectrum. Depending on the jitter source frequencies, different plots are used.

The jitter spectrum view performs a Fast Fourier Transform (FFT) on the clock TIE measurement trend to show all jitter frequencies. Figure 5 shows a few spikes on the spectrum. The frequencies of these spikes can be measured by the markers. The higher the magnitude of the spikes, the more jitter contributed by the source. The markers show the frequencies of the larger spikes to be 12.5MHz, 25MHz and 50MHz, which correspond to frequencies of the on-board oscillators. These frequencies are caused by poor shielding of the on-board oscillators and are coupled into the high-speed clock signal. To improve the clock jitter, you must first shield the oscillator coupling.

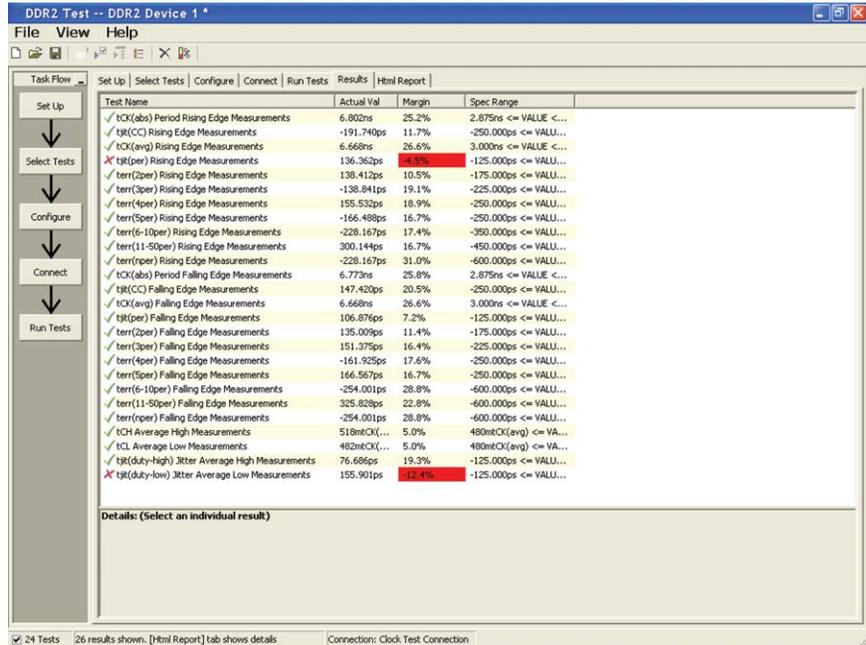


Figure 4. Automated DDR test software can efficiently and effectively identify clock jitter.

Observing lower frequency using spectrum view is more difficult, but the smoothing function on the TIE measurement trend helps. Averaging out the high-frequency noise on the measurement trend leaves the jitter for the low frequencies. Using a marker, you can again measure the jitter frequency. Figure 6 shows the low frequency with jitter at 180 kHz, which is caused by the switching power supply coupling into the high-frequency signal.

The correlation can also be made by comparing the smoothed clock jitter trend and switching power supplies.

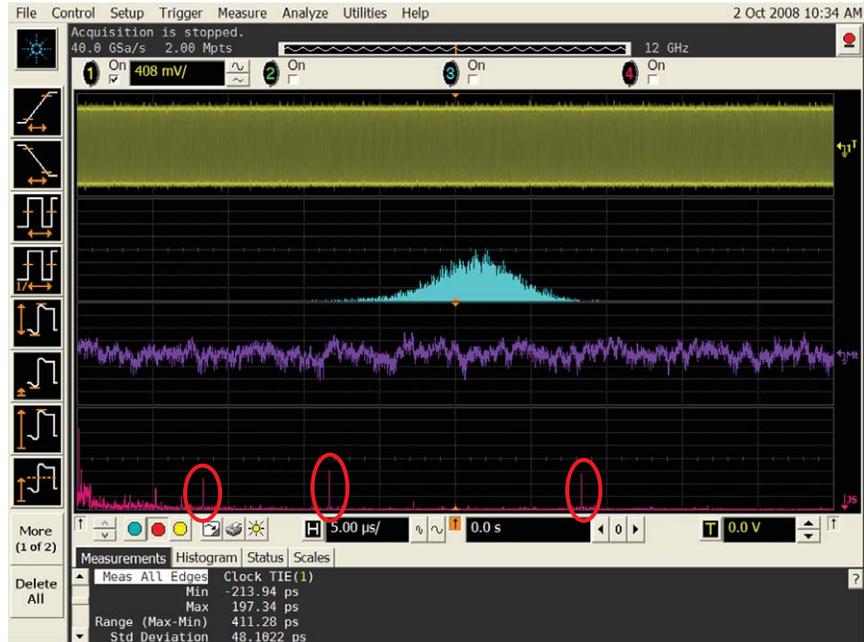


Figure 5. EZJIT displays the jitter in the spectrum, with spikes at 12.5MHz, 25MHz and 50MHz. The spectrum display can be useful to identify sources of jitter from their frequency components. Here the jitter is caused by poor shielding of the on-board oscillators.



Figure 6. EZJIT lets you observe and measure the low-frequency jitter. Again the spectrum can help identify sources of jitter from frequency components. The low frequency with jitter of 180 kHz is due to a nearby switching power supply.

Separating jitter components

The EZJIT Plus tool separates the various jitter components on the clock signal into random jitter (RJ), periodic jitter (PJ) and deterministic jitter (DJ). Knowing which type of jitter contributes to the jitter can help you determine the root cause of problems.

RJ tells you that a component is contributing white noise to your clock. Using a scope probe, you can evaluate each component to determine the RJ contribution and eventually swap out the noisy component with a better one.

PJ tells you an oscillating signal is coupling to the clock. You can identify the signal with the EZJIT tool.

If DJ dominates, DCD is mostly likely the cause; ISI does not exist on a clock. DCD is due to intra-lane skew, which is often caused by the length of the signal route. One signal is longer than the other, causing a delay in its differential lane.

Using these tools to test and debug your designs improves your signal integrity, allowing you to quickly identify and fix problems.

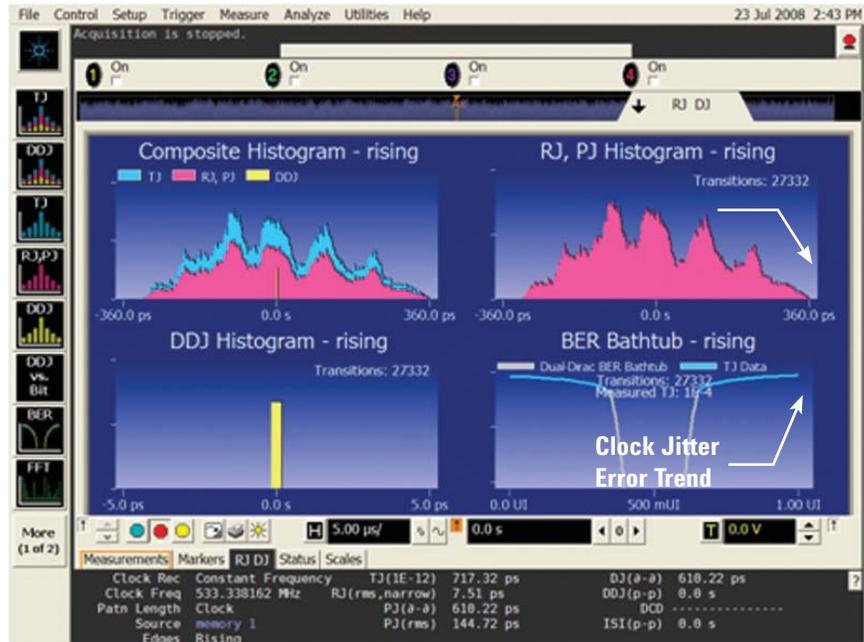
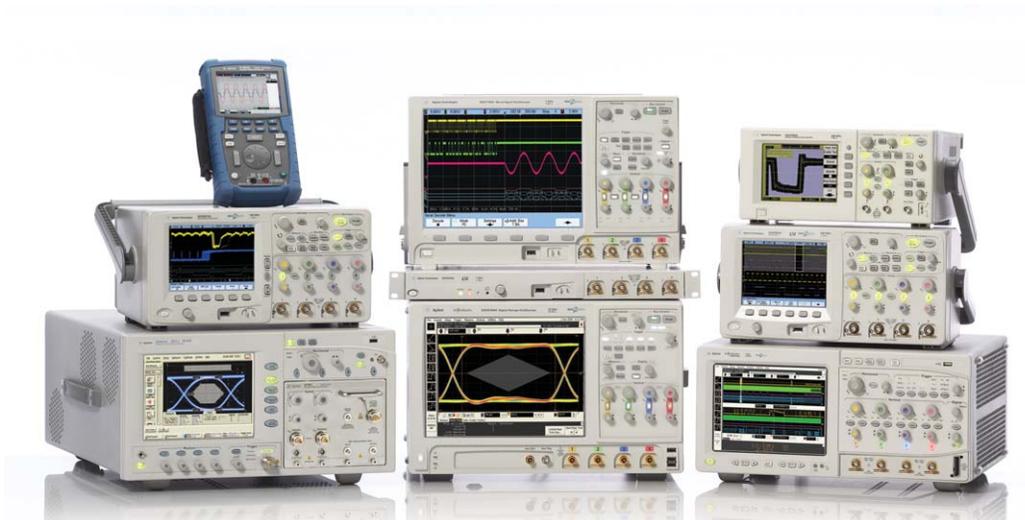


Figure 7. EZJIT Plus separates the jitter components on the clock. Here the PJ contribution appears highest, which is due to oscillating signals coupling to the high-speed signal

Related Literature

Publication name	Publication type	Publication number
<i>DDR Memory Overview, Development Cycle and Challenges</i>	Tutorial	5990-3180EN
<i>DDR Design and Verification through Simulation</i>	Tutorial	5990-3317EN
<i>DDR Probing for Physical Layer and Functional Validation</i>	Tutorial	5990-3182EN
<i>Identifying the Causes of DDR Data Corruption and Elusive Failures</i>	Tutorial	5990-3183EN
<i>Separating Read/Write Signals for DDR DRAM and Controller Validation</i>	Tutorial	5990-3187EN
<i>Ensuring Compliance and Interoperability in DDR Designs</i>	Tutorial	5990-3188EN
<i>Agilent DDR Memory Solutions</i>	Brochure	5990-3324EN



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Revised: October 1, 2008

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Printed in USA, December 19, 2008
5990-3189EN



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