Introduction

J-BERT N4903B high-performance serial BERT with complete jitter tolerance testing for forward clocking topologies

- All jitter sources built-in (DJ, RJ, ISI, Si)
- Half-rate clocking with duty cycle variation
- Common and differential mode interference
- Flexible pattern sequencer
- Automated measurements for RX and TX physical layer parameters

This document describes the receiver (Rx) jitter tolerance test requirements resulting from forward clocking topologies. It explains how these requirements can be efficiently fulfilled for compliance and characterization test by using the Keysight Technologies, Inc. J-BERT N4903B high-performance serial BERT with complete jitter tolerance testing.

Traditional synchronous clock distribution reaches a limit at several hundred megabits per second (Mb/s). As the data rate goes up, setup and hold times become increasing critical, particularly given the manufacturing tolerances of chips and PC boards. Consequently, designers of chips and PC boards developed a technique to skip clock distribution. This technique is called embedded clocking and uses a data signal to extract the clock, eliminating the clock signal routed between the transmitter (Tx) and Rx at the Rx side. This technique can be used up to ultra high data rates; however, high-frequency jitter behavior becomes an issue when clock-data recovery (CDR) circuits are used. Additionally, embedded clocking requires some data coding, adding significant overhead to the amount of data and raising the data rate beyond the base rate.

The invention of delay locked loop (DLL) circuits then helped to push the range of data rate further, while keeping a clock distributed. The benefit of this clock topology is that the skew can be adjusted to the setup and hold time requirements at the receiving end. Consequently, various types of jitter are added that similar to clock and data jitter, and the issue of high-frequency jitter is reduced; Rx functionality and performance is maintained at data rates in the gigabits per second (Gb/s) range.

Xilinx popularized the use of forward clocking topology with help of DLLs in the Virtex FPGA family [1]. At the time of writing this document, the main drivers of forward clocking topology are Intel with QuickPath Interconnect (QPI) [2] and AMD. Other applications using similar concepts are memory interfaces like double data rate memory (DDR) and graphics double data rate memory (GDDR) [3] and the Serdes Framer Interface Level 5 (SFI-5) [4]. Figure 1 depicts the clocking topology tree.

Figure 1. Clock topology tree

Figure 2. Forward clocking topology
Forward Clocking Topology

The architecture of the forward clocking topology is depicted in Figure 2. This topology is also referred to as half-rate clocking, since the clock frequency is typically half of the data rate. It is also referred to as source synchronous clocking, since several data lanes are accompanied by a clock lane running at half rate. On the Rx side, a DLL circuit block compensates for tolerances in the clock distribution network. This provides several advantages:

- Data and the half-rate clock require the same bandwidth in the transmitter output, the channel, and the receiver input. Any design limitation causes similar distortion on both the clock and data.
- In case of jitter due to cross-talk, the compensation will add-up similar to data and clock, so at the receiver tolerances arrive synchronous and cancel out.
- The DLL-based clock distribution eliminates tolerances within the clock distribution network, thus enabling the data transfer of multiple lanes at gigabit speed.

The Difference of Phase-Locked Loop (PLL) versus DLL

The basic concepts of a PLL versus a DLL are depicted in Figure 3. A PLL is basically the same as a CDR. So comparing a PLL and a DLL extracts the differences between systems based on embedded clocking versus forward clocking.

The PLL in Figure 3 (right side) uses a voltage controlled oscillator, which generates a clock signal that follows a reference clock signal. The control logic, consisting of a phase detector and a loop filter, adjusts the voltage controlled oscillator’s (VCO’s) frequency and phase by comparing the reference input clock with the feedback clock. When the reference oscillator clock edge aligns with the feedback clock edge, the PLL is locked. The loop filter is a low pass filter of a second or higher order. The bandwidth of the filter together with the phase detector is within a couple of megahertz (MHz.) Consequently, the jitter tracking depends on the cut-off and peaking/damping characteristics of this filter. The disadvantage of a CDR is that it cannot track high-frequency jitter. Thus, jitter transfer is a weakness of the CDR design and jitter transfer measurements become a major task.

The DLL consists of a variable delay line (VDL) and control logic. The delay line is implemented as an analog delay line controlled by a voltage or a digital delay line containing a chain of gates, or a mix of both. With the help of the control logic, the propagation of the delay line is adjusted until the edges from the clock input and the feedback clock from the clock distribution network align. When the edges line up, the DLL is locked. Thus, the DLL output clock compensates for the delay in the clock distribution network. This compensation is sometimes referred to as a negative delay generated by the DLL. In actuality, the DLL incorporates a handful of clock cycles that can be seen when running a bursted clock, which is a valid operating model.

Once locked, there is no need for any further action, except for some compensation for very slow drift due to temperature effects. Fully digital DLLs allow the control logic to be turned off once the DLL is locked. The DLL can be designed to generate clocks with various phases, or it can incorporate clock doublers, including a compensation for a clean and exact 50 percent duty cycle. In most systems, a crystal oscillator generates the system clock.

Most crystal oscillators produce a signal with a tolerance of 100 ppm, meaning a 0.01 percent change in the clock period. A DLL tolerates a frequency drift of significantly higher magnitude. The output clock signal of a DLL reflects any instability on the input clock signal. This is desired to track edge changes due to jitter. Any jitter, including high-frequency jitter, is tracked by the DLL and is not limited by the bandwidth of the delay line—which is as high as the clock rate or higher.

The forward clocking topology uses DLLs with clock doublers. Clock doublers are sensitive to the duty cycle distortion of the input clock. Thus, the variation of the clock duty cycle is of vital importance for stress testing. As the propagation path of the data and clock to the Rx input differs only for a couple of clock cycles, only very high frequency jitter may cause an eye closure due to phase shift. Consequently, the stress signal for the Rx is mostly composed of inter-symbol interference (ISI) jitter, with a small amount of standard random jitter/deterministic jitter (RJ/DJ) added.

Figures 3a and 3b. DLL vs. PLL
Intel QPI

Starting in 2008, Intel's new system architecture and platform technology will be called Intel QuickPath Technology. It features new system architecture which integrates a memory controller into each microprocessor and connects processors and other components with a new high-speed interconnect. Previously announced under the code name Common System Interface or CSI, the Intel QuickPath Technology is designed to allow uninhibited performance of Intel's future generations of multi-core processors.

The Intel QPI (also known as QuickPath) is point-to-point processors interconnected. Each QPI comprises two 20-bit, point-to-point links. One link is used in each direction, with a separate clock in each direction, for a total of 42 signals. Each signal is a differential pair, so the total number of pins is 84. Performance numbers for QPI are reported to be 4.8 to 6.4 Gb/s per data lane. The forwarded clock runs on a frequency that equals the data rate divided by two:

\[
\text{Clock frequency} = \frac{\text{Data rate}}{2} \quad (1)
\]

Example: For the data rate of 6.4 Gb/s, the clock frequency is 3.2 GHz.

The following make the high data rate possible:
- The differential clock and data travel together and run at the same frequency.
- The same crystal drives the reference clocks on different agents.
- The clock phase and data are “trained” and aligned at the receiver.
- The receiver sampling is based on the forwarded clock, while DLLs are used for clock alignment and multiplying, thus any jitter is adding to the clock and data in a similar way and they stay in phase.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRX-Gaussian</td>
<td>0.02 UI rms</td>
</tr>
<tr>
<td>TRX-DJ</td>
<td>0.3 UI</td>
</tr>
<tr>
<td>TRX-SSC</td>
<td>500 ppm @ 33 kHz</td>
</tr>
<tr>
<td>TRX-DCD-CLK</td>
<td>0.05 UI</td>
</tr>
<tr>
<td>VRX-min-max-ratio</td>
<td>4</td>
</tr>
<tr>
<td>VRX-input</td>
<td>200 mV</td>
</tr>
<tr>
<td>TRX-input</td>
<td>0.5 UI</td>
</tr>
<tr>
<td>VRX-CLK</td>
<td>200 mV</td>
</tr>
<tr>
<td>TRX-min pulse</td>
<td>0.6 UI</td>
</tr>
</tbody>
</table>

Table 1. Receiver margining specifications

Important aspects for jitter tolerance margining, also referred to as jitter stress test, include:
- Forwarded (half rate) clock shall be jitter free, and include variable duty cycle
- The data and clock carry identical jitter/spread spectrum clocking (SSC) except for inter-symbol interference (ISI), which is present on data only
- Data is looped back to bit error ratio test (BERT) error detector for the bit error ratio (BER) and jitter tolerance testing
Intel QPI (continued)

The jitter parameters according Table 1 have the following meanings:

1. **Rx-Gaussian**: Calibrated RJ requested, amount as specified. This is provided by J-BERT N4903B as calibrated dial.

2. **TRx-DJ**: Calibrated ISI is requested. As the specification is applied at the physical pin of the receiver package, it may require to de-embed the actual fixture or to add some additional ISI. This needs insight to the design of the actual fixture. A good practice for the fixture design is to include a reference trace with coaxial connectors on both sides. This allows ISI measurements, as well as collecting the s-parameters. If de-embedding is needed, the use of the Keysight J-BERT N4903B in conjunction with the Keysight N4916A de-embedding signal converter is recommended, or if additional ISI is necessary the use of the Keysight J-BERT N4903B interference channel is recommended to add ISI by the selectable ISI traces.

3. **VRx-min-max-ratio**: This is another description of loss by ISI in the channel. Same recommendation applies as for the item before (TRx-DJ).

4. **TRx-SSC**: Calibrated SSC is requested, amount as specified. This is provided by the J-BERT N4903B as dial.

5. **TRx-DCD-CLK**: Calibrated duty-cycle distortion (DCD) requested, amount as specified. This is provided by the J-BERT N4903B as calibrated dial with the divided clock output.

6. **VRx-CLK**: This is again a matter of loss. Using the reference trace is a good practice. Measure the opening (millivolt (mV) height at the center of the eye) of the differential voltage eye of the 1010 Pattern out of the forwarded clock output as measured over a >100000 unit interval (UI).

7. **TRx-minPulse**: A minimum pulse width has to be applied to the Rx input. This is due to the ISI caused by the channel. Using a reference trace as described under Item 2 is recommended. For calibration/verification of the required amount of eye closure, the signal has to be measured over at least 1000000 UI with help of a real time scope.

8. **VRx-input**: This is the voltage eye (maximum eye height (mV) within a BER = 1E - 12 contour) that needs to be obtained by looping back the BERT output to itself and measuring the eye with a CDR clock or the forwarded clock looped back to itself. The user needs to send a PRBS31 pattern out of the BERT transmitter, keeping the external equalizer, if any, off. The jitter parameters should be tuned within their maximum specification. Additionally, the voltage amplitudes, along with any common mode noise injected, should be adjusted so as to obey this specification.

9. **TRx-input**: This is the timing eye (maximum eye width (UI) within a BER = 1E - 12 contour) that needs to be obtained by looping back the BERT output to itself and measuring the eye with a CDR clock or the forwarded clock looped back to itself. All the input conditions imposed are under similar conditions as the VRx-input.

10. **VRx-input and TRx-input**: These can be effectively calibrated with the help of the TRx-input: Keysight J-BERT N4903B eye contour measurement.

More requirements stated by the standard and provided by J-BERT N4903B:

- The standalone receiver characterization requires a BERT with previously defined requirements. The BERT should have a capacity of minimum 12 Gb/s signaling due to likely future requirements, including its CDR and jitter, and noise injection capabilities.
- Generate an appropriately divided reference clock from the main forwarded clock which can be supplied to the receiver.
- A versatile CDR loop to receive the looped back transmitter data. The bandwidth of the CDR must be high enough to integrate most of the noise added in the internal loopback path after the data receiver amplifier.
- Capability to generate user-controlled delay between the data and the forwarded clock outputs with fine granularity (100 fs).
Testing the Rx of the Forward Clocking Topology:
Generic Considerations

As previously discussed, a minimum forward clocking topology consist of data lanes and a dedicated clock lane running at half the frequency than that of the data rate applied to the data lanes.

The Rx jitter tolerance test in general adds SSC, ISI, PJ, RJ, and SI to the data lanes and DCD to the clock lane. HT3 add HF jitter (phase-shifted PJ) and SI to the clock lane.

Test patterns required for Rx jitter testing are long pseudo random binary sequence (PRBS) sequences (like $2^{23}-1$ or $2^{31}-1$), which are a common pattern for the J-BERT N4903B.

The J-BERT N4903B (Figure 4) comes with all the required features for Rx testing:
- Half rate clock with variable duty cycle on the generator
- Fully calibrated jitter sources RJ, PJ, SJ, SSC, and residual SSC on data; SSC and phase shifted PJ on clock
- ISI traces and SI with common/differential mode on data
- BER and jitter tolerance measurement, and more high-level measurements for Rx and Tx
- Generation of de-embedded signals with help of the N4916A

Figure 4. J-BERT N4903B together with the N4916B De-Emphasis Signal Converter for testing a forward clocking topology
Testing the Rx of the Forward Clocking Topology: Generic Considerations (continued)

Figures 5 to 7 depict the various editors of the J-BERT N4903B that can be used to setup the parameters. Figure 5 shows the editor for data outputs, which contains the level parameters, the termination parameters, the output state parameters, and the delay parameter of the data and clock timing. The parameters can be edited by numerical entry or, by selecting a specific digit, the value can be dialed in using the instrument’s knob or the arrow keys.

Figure 6 shows the editor for the clock/trigger output. It contains the level parameters, the termination parameters (the half rate clock selection and the duty cycle (Dcyc)) adjust.

The graphics to the left in both output editors provide a rough indication of timing and level reference.

Figure 7 shows the editor for jitter setup. The first entry is made in the configuration field with help of the radio buttons for:

- The selection between sinusoidal jitter (SJ), SSC, or residual SSC
- The selection of spectrally-distributed random jitter (sRJ), or combined random and bounded uncorrelated jitter (RJ, BUJ)

Jitter Rx tolerance testing of forward clocking topology uses basically SSC and periodic jitter as depicted in the figure 7. With help of the delay programming between data delay line and clock delay line, a phase shifted PJ may be applied to the clock signal.

All the pre-calibrated jitter parameters can be set using the dials on the J-BERT N4903B. If there is a need to verify the jitter values as noted in Reference [5], the use of the Keysight Infiniium 86100C DCA-J is recommended for performing jitter analysis.
Testing the Rx of a Forward Clocking Topology: Specific Considerations

Some Forward clocking standards require to add ISI jitter. Sometimes it is specified in terms of amplitude reduction for high frequency signals vs low frequency signals. The J-BERT N4903B-020 provides a set of PC board traces to add such ISI. For example, at a data rate of 6.4Gb/s with trace 2 and a PRBS 2^23-1 pattern, an amplitude ratio of 1:4 can be obtained as shown in Figure 8. The single bit is down in reference to several consecutive bits (marker reading 62 mV / 246 mV = 1/4.) Such ISI creates a timing jitter of 67 ps (equivalent to 430 mUI) as shown in Figure 9. This timing jitter has to be taken into account when adding further jitter components for a typical eye closure total of 0.5. Consequently, there is just room for 70 mUI of sinusoidal jitter to be added as shown in Figure 7.

Practically, the fixtures holding the DUT are made from FR4 material so there may be a significant amount of ISI already built in, which can create the need to compensate for, rather than add, ISI. In this case, the use of the N4916B De-emphasis Signal Converter is recommended. For details see Reference [6].

It may additionally be required to have jitter and/or SI on the forwarded clock.

The test setup to address this requirement is shown in Figure 10. In this example, the J-BERT N4903B is used together with the N4916A De-emphasized Signal Converter and the Keysight 81150A Pulsar.

If the RX uses a Decision Feedback Equalizer (DFE), then the test requires a large variation of the amplitude ratio (transitional bit versus de-emphasized bit.) As shown in Figure 11, combining the connections of the N4916B De-emphasized Signal Converter with the J-BERT N4903B and the ISI traces in the interference channel module is recommended. The data generated runs first through the N4916A de-emphasized signal converter and then through the ISI trace. The ISI trace is selected for the maximum amplitude ratio needed, and can then be reduced by dialing in the de-emphasis ratio. The output of the interference module connects to the data input of the DUT.

The stressed clock can be achieved with help of the following methods:

- Adding a differential external source (such as the 81150A pulse function arbitrary noise generator) See Figure 12.
- Using the J-BERT N4903B’s embedded PJ jitter source on the data and clock with a phase shift (delay between delay lines), see Figure 7.

The stressed clock setup, as shown in Figure 12, uses transition time converters (N4915A-001) to slow down the edge speed, and power dividers (Keysight 11636B) to combine the data signal and the modulating signal. When differentially adding the modulating signal creates DCD type of jitter, it is important to monitor the modulated data signal for the minimum differential eye height. In general, this kind of external modulation provides more flexibility, and is the more complex and expensive solution. (For more details on jitter modulation, see References [8], [9], and [10].)

When using the delayed PJ on the clock as depicted in Figure 7, the amount of clock jitter results from the phase shift of the PJ signal between data and clock signal.
Summary

As microprocessors and chipsets continue to advance, forward clocking topology is also evolving. Intel’s QPI is designed to allow uninhibited performance of its future generations of multi-core processors.

These types of events challenge the traditional approaches to Rx jitter tolerance testing. Keysight offers a number of products to help efficiently fulfill compliance and characterization testing. The feature-rich Keysight J-BERT N4903B high-performance serial BERT with complete jitter tolerance testing provides all jitters as calibrated dials, and eliminates the need to perform custom calibration. For testing needs such as de-emphasized signals/variable ISI signals Keysight offers the N4916A de-emphasis signal converter. Other Keysight equipment such as Infiniium scopes, arbitrary noise generators and power dividers complement the J-BERT N4903B, providing complete jitter testing solutions for virtually all requirements.

Setup of N4903B for Forward Clocking Topology with disturbed clock

![Diagram of Setup of N4903B for Forward Clocking Topology with disturbed clock]

Figure 16. Setup of N4903B for Forward Clocking Topology with disturbed clock

![Diagram of Variable ISI setup]

Figure 17. Variable ISI setup

![Diagram of Stressed clock setup]

Figure 18. Stressed clock setup
Related Products

- J-BERT N4903A High-Performance Serial BERT with complete jitter tolerance testing
- N4916A Industry-first De-Emphasis Signal Converter
- Infiniium 86100C DCA-J wideband oscilloscope
- Infiniium DSA91304A High Performance Oscilloscope: 13GHz
- 81150A Pulse Function Arbitrary Noise Generator
- 1636B Power Divider, DC to 26.5 GHz

Glossary

BER  Bit error ratio
BERT  Bit error ratio tester
BUJ  Bounded uncorrelated jitter
CDR  Clock-data recovery
CLK  Clock
CSI  Common system interface
Dcyc  Duty cycle
DCD  Duty cycle distortion
DFE  Decision feedback equalizer
DJ  Deterministic jitter
DLL  Delay-locked loop
DDR  Double data rate
FR4  PC board material
GDDR  Graphics double data rate
ISI  Inter-symbol interference
LVDS  Low voltage differential signaling
PLL  Phase-locked loop
PJ  Periodic jitter
PRBS  Pseudo random binary sequence
QPI  Quick path interconnect
RJ  Random jitter
Rx  Receiver or receive
SI  Signal integrity
SJ  Sinusoidal jitter
SSC  Spread spectrum clocking
SFI-5  Serdes framer interface Level 5
sRJ  Spectrally-distributed random jitter
Tx  Transmitter or transmit
UI  Unit interval
VCO  Voltage controlled oscillator
VDL  Variable delay line

Related Literature

J-BERT N4903B High-Performance Serial BERT Data Sheet
5990-3217EN

Second Generation PCI EXPRESS® Testing with the J-BERT N4903A High-Performance Application Note
5989-4087EN

81150A Pulse Function Arbitrary Noise Generator Data Sheet
Version 1.05 Data Sheet
5989-6433EN

Infiniium DCA-J Wide-Bandwidth Oscilloscope - Mainframe & Module Technical Specs Data Sheet
5989-0278EN

Keysight Technologies Infiniium DSO/DSA 90000A Series Real-Time Oscilloscope Data Sheet
5989-7819EN

References

[1] Xilinx Clock Management Application Notes:
www.xilinx.com/support/documentation/application_notes/xapp174.pdf and
[3] Designing and Validating High-Speed Memory Buses, Application Note, 1382-2 Literature number 5988-4497EN
[6] The Keysight N4916B De-emphasis Signal Converter, Data Sheet, Literature number 5990-4630EN
[8] Flexible Signal Conditioning with the Help of the Keysight 81134A Pulse Pattern Generator, Application Note, Literature number 5989-8094EN
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