Keysight Technologies
Limited Access Tools to Improve Test Coverage

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Published in USA, July 31, 2014
5990-6765EN
www.keysight.com

KEYSIGHT TECHNOLOGIES

Limited Access Tools to Improve Test Coverage

Smaller test pads are overwhelming the best probing techniques.

THE TREND OF shrinking electronics, coupled with added complexity and capability packed into the board assembly, is a manifestation of Moore's Law at a level beyond the silicon realm. We see this trend in our daily lives, and it has become more apparent in consumer products like cellphones, notebooks and gaming products, to name just a few.

The implications of this trend on the assembly level are profound if one looks at the test access on the assembled board and how that has changed over the years. Gone are the days when 0.100″ test pads were in abundance. That evolved to 0.075″ test pads, which then progressively shrank to 0.050″, then 0.035″ and so on. Fixture vendors now get customer requests to accommodate 0.018″ test pads.

In the past, one could mitigate this trend through more precise probing. However, due to escalating and prohibitive costs, this is becoming increasingly difficult, and the test pads themselves are diminishing.

Despite this, the manufacturing industry still needs a way to electrically test assemblies amid an environment of reduced access. The good news: There are several ways to go about doing just that on in-circuit testers.

Categorically, the tools available can be placed into five groups:

1. IEEE 1149.x boundary scan tools. Boundary scan is becoming more important as test access diminishes. Complementing the gain in prominence of boundary scan is the fact that putting extra silicon on the die real estate to enable boundary scan is less of a barrier now compared to five years ago. In fact, this may no longer even be an issue, because this extra investment in silicon is infinitesimal compared to the silicon occupied by the core logic itself.

To those unfamiliar with boundary scan, it simply can be described as follows: A boundary-scan compliant IC would have at each of its pins a boundary scan cell, which, depending on its type, would be capable of driving signals or receiving signals or both, if it is a bidirectional cell. These boundary scan cells can be controlled through four pins on the IC called the Test Access Port (TAP), and they are governed by the IEEE 1149.x standard. So essentially having test access to the four TAP pins will enable the I/O control of the rest of the pins on the IC, which could be in the hundreds or even thousands.

Three boundary scan tools come to mind. First, and chief among them, is that related to the IEEE 1149.1 standard. This is the most popular form of IEEE 1149.x. Having a "chain" of ICs conforming to this standard permits testing of the interconnect nodes between ICs. This is done through inputting a predefined pattern of bits into the interconnect nodes. A short or open on those nodes will alter this pattern, and as it exits the chain, the defect then can be diagnosed. As shown in FIGURE 1, no physical test access is required from these interconnect nodes.

Boundary scan tools can use IEEE 1149.1 not only to test the interconnect nodes, but also between the interconnect nodes and other nodes that have test access, but are not part of the boundary scan chain. This is the advantage of boundary scan on ICT, which has access to a bed-of-nails fixture. However, IEEE 1149.1 is not equipped to handle AC-coupled differential signals. For this type of architecture, use IEEE 1149.6.

One derivative of boundary scan is when it is used to test non-boundary scan devices. Again, think of the boundary scan cells mentioned earlier for which their I/O capabilities can be controlled. We can use that to drive or receive a non-boundary scan IC to perform various digital tests.

2. Vectorless test. Vectorless test is a popular misnomer for a test methodology involving parasitic capacitance coupling. One such solution involves the use of a capacitive coupling plate resting on the device-under-test (DUT) to pick stimulus signals injected via test pads.

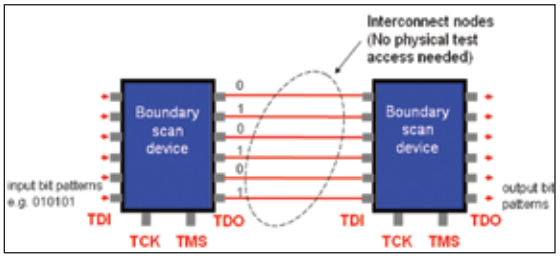

FIGURE 1. A simple chain of boundary scan ICs.

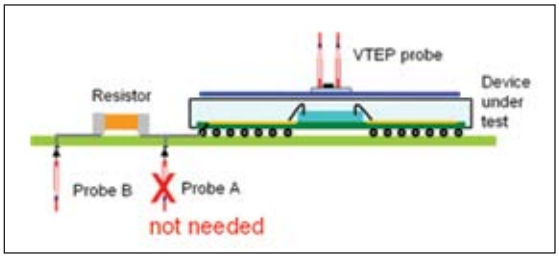

FIGURE 2. DriveThru injects a stimulus signal through a passive component directed toward the DUT.

ANDREW TEK is a product marketing engineer at Keysight Technologies (keysight.com); Andrew-ck_tek@keysight.com

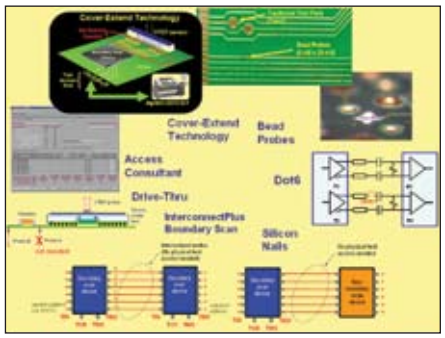

FIGURE 3. Various limited-access tools at the disposal of test engineers today.

But this is to imply that VTEP *per se* is not a limited access tool, as it still requires physical test access for the user to inject this stimulus signal. However, a novel variant of VTEP, on the other hand, is. DriveThru works the same way as VTEP, but unlike VTEP, the stimulus signal is injected one-passive-component-away from the DUT (**FIGURE 2**). This permits the user not only to test the DUT, but also the passive component, as it is now made part of the signal propagation path. If there is an open in the path (e.g., a missing resistor), the test will fail. The advantage is that the user does not need to assign test pads to both sides of the passive component. Just one will do.

3. Boundary scan/vectorless test hybrid. A recent product to the market is a hybrid between boundary scan and vectorless test. As you would recall, vectorless test requires a stimulus signal, and this is typically injected into the DUT through a test pad. This hybrid technique eliminates the need for this test pad. Instead, the stimulus signal now comes from a boundary scan device.

4. Bead probes. Bead probes are basically lumps of solder sitting on an exposed part of a signal trace or microvia on the assembly. In the case of the signal trace, they are only as wide as the signal traces themselves. Compared to a traditional 0.035˝ test pad, which may be seven times wider than the trace that it serves, bead probe is a boon to board designers, as it does not disrupt the layout of signal traces and therefore simplifies the design process. Also, studies have shown that bead probes do not degrade signal integrity any more than a virgin trace does, even up to a 20 GHz level. Bead probes provide direct physical test access in places where it would normally be difficult to do so, either due to physical space constraint or because of the high-speed signals the trace is intended to carry.

5. Analysis software. Strictly speaking, this category is not one that will directly provide test coverage in a limited-access environment, but rather, it serves as a productivity tool to increase the effectiveness of those limited-access solutions at our disposal. A case study performed on two different assemblies showed that the first, a 3312-node network switch product, had the opportunity to reduce its test pad population by 42.8%, while the analysis on the second, a high-volume consumer product, came up with a reduction of 166 test pads from a total of 479 before the analysis. A reduction of test pads would naturally also translate into a reduction of test probes needed to test them on a fixture, bearing with it cost savings in tow. **CA**

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area for recoating. Good parts are packed and the job order closed out.

Assumptions Before Simulation

During the manufacturing simulation, educated assumptions were made regarding the resource, equipment layout, equipment availability and process flow. Some important assumptions included:

- Double-sided, hybrid PWBs will flow through the kitting area, automated area, the first manual area, coating area, and the second manual area. Individual PWBs are on a 2 x 2′ panel.
- PWBs are transferred between different areas in batches of 16 PWBs.
- Six operators will be needed in these positions: kitting, placement, inspection, assembly, test and coating.
- Assembly time used in the simulation is based on previous experience.
- Equipment resource was assumed to be dedicated to PWB assembly with no conflicts in resources. It is assumed that machine utilization is 100% with no downtime. Resource utilization (manpower) is 70%.
- Processes such as solder paste printability, component placement, solder reflow, and conformal coating are assumed to be 98% defect-free.

Simulation report and analysis. We ran 95 iterations to get a 95% confidence level in the simulation model. The time spent in each area and manpower utilization was calculated. The average time spent to assemble a batch of 16 PWBs was determined to be 26 hrs. The most time is spent in the first manual area, where connectors hand-soldering and PWB cleaning took place.

Based on statistical analysis, with 95% confidence we can state that:

- The time spent in the manual area accounts for approximately 50% of the total manufacturing time.
- The assembly operator is the most utilized resource at 34% utilization, more than twice any other resource.
- The system is underutilized, with most of the resources utilized less than 20% of capacity.

It can be concluded that with the current input parameters, the system is underutilized. Steps taken included:

- The biggest bottleneck was hand soldering. With operator cross-training and additional hand-soldering stations, this bottleneck was eliminated and manpower utilization improved to 50%.
- Equipment layout was modeled using simulation software to optimize product flow with minimal handling, thus saving unnecessary installation and moving costs.
- Operator movement around the machines and workbenches was modeled to provide ergonomically designed workcells.
- *Kan ban* storage for replenishing components and floor stock was strategically placed to optimize production flow.
- The kitting operator was trained and certified to perform conformal coating. After optimizing the production line resource to five operators instead of six, the simulation was recalculated and showed an additional 10% improvement in manpower utilization. **CA**