

Keysight Technologies

Solutions for Emerging 4G and WLAN Communication Systems

Making Digital Pre-Distortion with Memory Effects
Fast and Practical for all Engineers

Application Note

Abstract

The ongoing migration of today's cellular telecommunication networks to 3.9G, and even 4G technologies like LTE-Advanced and 802.16m WirelessMAN-Advanced, brings with it many challenges. The same can be said for the evolution of the Wireless Local Area Network (WLAN) family of standards to its latest variants, 802.11ac and 802.11ad. In each case, these emerging standards must support increasingly higher data rates and are employing a number of key enhancements and technologies to accomplish that goal. The net result are standards that are much more complex, and in turn, much more difficult to design and test than their predecessors. Added to this, the standards are continually evolving.



Introduction

One particularly critical area of concern when it comes to design and test of devices based on emerging 3.9 and 4G standards is the power amplifier (PA). Because smart phones and other advanced wireless devices rely so heavily on battery power, getting the most efficiency out of a design is critical. PAs contribute significantly to power consumption, and in turn, overall system performance—directly impacting device hardware and its requirements for 4G operation. As a result, one of the biggest challenges today's engineers face is choosing/designing the right PA to meet design goals at the lowest possible cost.

Problem

The PA is an essential component in the overall performance and throughput of wireless communications systems and, as an active device, is inherently nonlinear. That nonlinearity generates spectral regrowth, which leads to adjacent channel interference and violations of the out-of-band emissions standards mandated by regulatory bodies. It also causes in-band distortion, which degrades the bit-error-rate and data throughput of the communications system. Operating the PA at a lower power is one way to reduce this nonlinearity. However, this reduces the service area and increases both the capital and operating expenses of the service provider. Linearization enables the PA to be operated in its high power-added-efficiency (PAE) region, near saturation and without significant signal distortion, thus reducing expenses.

Digital Pre-Distortion (DPD) is today the most popular technique for linearizing a PA. It accomplishes this task using the real-world signal, which is complex and time varying, created in the baseband using sophisticated signal processing. Additional signal processing is then employed to modify the signal to counter the nonlinear effects of the PA. While DPD provides a cost-effective means of PA linearization, it often requires a highly specialized skill set for modeling and implementation. Additionally, to achieve the most efficient and linear PA output performance, memory effects must be included in the DPD process.

Solution

Engineers migrating to 4G require a solution that makes implementing DPD fast and practical for 4G communications systems—one that can be used by engineers at all levels of expertise and requires minimal equipment. The tool set should be accurate, avoid dependence on a vendor-specific chipset or hardware implementation for the initial modeling and able to absorb custom DPD into the rest of the baseband processing, preserving a lower bill-of-materials. To ensure an optimal level of accuracy, it should also be able to account for memory effects in the PA, as well as, nonlinearity. Moreover, it must support connectivity with a range of other tools for hardware verification.

One solution that meets this criterion is the Keysight Technologies SystemVue platform with its W1716 DPD Builder add-on personality (Figure 1). The utility helps users quickly model and correct common sources of nonlinearities and memory effects in both low and high-power 4G PAs, transceiver ICs and automatic gain control modules. It contains several sophisticated crest-factor reduction (CFR), DPD, signal generation, and instrument control capabilities rolled into a single, easy-to-use, wizard-based user interface, and features 4 pre-distorter models and extraction methodologies (Memory Polynomial, Volterra, Look-up Table (LUT), and user-defined .m math algorithms). It supports proprietary DPD models, extraction intellectual property and test vectors, as well as, creation of a custom graphical user interface. Additionally, it provides links to the latest wideband test equipment (up to 800 MHz), including arbitrary waveform generators and digitizers; simulators like Keysight's Advanced Design System (ADS); and the M9381A vector signal generator and M9391A vector signal analyzer PXI modular instruments.

System architects and RF component designers can use the W1716 DPD Builder to quickly assess and improve link-level performance, partitioning and component selection, while baseband algorithm developers, RF architects and RF compo-

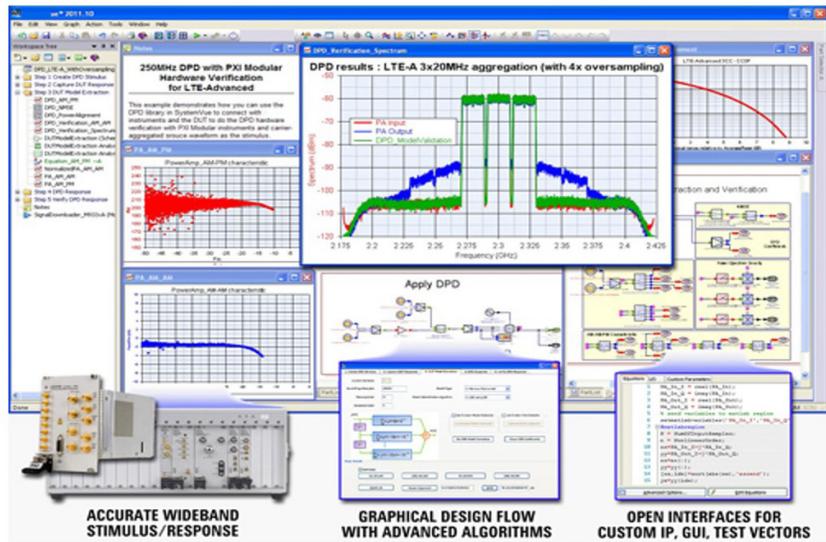


FIGURE 1. The W1716 DPD Builder's LUT DPD is widely used for high-volume PA applications, such as mobile handsets, femtocells and WLAN infrastructure. It accepts custom intellectual property and test waveforms, which allows researchers to control proprietary model and extraction algorithms but still use a supported, commercial modeling platform.

nent designers can use it to accelerate the actual implementation of linearization networks. It is particularly useful for wireless system architects conducting early R&D architecture and component studies using common, off-the-shelf test equipment found in the test lab. Using the W1716 DPD Builder allows them to assess, in minutes, how "linearizable" a component will be, while still retaining ultimate hardware flexibility and full 4G measurement confidence. Users have a choice of verification (e.g., swept EVM and ACP verification), with or without automated power back-off. In contrast, proprietary DPD solutions force a number of premature implementation decisions to even perform a 4G feasibility study.

CFR is a technique that supplements and improves the effectiveness of DPD. For modern communication systems, spectrally efficient wideband RF signals have a peak-to-average power ratio (PAPR) as high as 13 dB. CFR preconditions the signal to reduce signal peaks without significant signal distortion. By reducing PAPR, CFR allows the PA to operate more efficiently. It also enables the signal to better comply with spectral mask and EVM specifications.

With its built-in CFR capabilities, the W1716 DPD Builder can correct for wider bandwidths, higher dynamic range and a variety of amplifier topologies. It performs this initial design inside SystemVue—a full baseband/DSP design environment—which allows the architect to transition the pure DPD algorithms into a custom hardware implementation, or to absorb the DPD algorithms into an existing FPGA or ASIC to maintain a small bill-of-materials. The W1716 DPD Builder's high-performance CFR algorithms work with virtually any modulation or standard, in addition to standards-specific CFR blocks for WCDMA, LTE and LTE-A.

Unlike other task-specific, chipset-specific or measurement-specific approaches to DPD, Keysight's SystemVue with W1716 DPD Builder takes the designer's perspective, featuring flexible, built-in links to instruments like Keysight's MXG signal generator and PXA spectrum analyzer for hardware verification (Figure 2). The MXG's high-performance internal calibration of wideband RF output makes it ideal for DPD applications. Its performance reduces the residual errors of an RF signal generator, which improves device characterization. The PXA's high-performance internal

calibration of wideband intermediate frequency also makes it ideal for DPD applications. It combines a wideband, high dynamic range with excellent phase and amplitude flatness performance and linearity, enabling better response measurements of devices.

Utilizing the setup shown in Figure 2, along with the W1716 DPD Builder, the DPD process can be implemented in six basic steps. These steps are identified in Figure 3.

Essentially, the DPD stimulus waveform (e.g., LTE, 802.11ac or user defined) is created and downloaded via the W1716 DPD Builder wizard into the vector signal generator. The waveform is then applied to the PA hardware or a model of the PA. Next, the PA's response (both input and output) is captured from the vector signal analyzer using VSA software. The PA output signal is captured by inserting the PA hardware between the vector signal generator and analyzer with appropriate signal calibration, including any signal padding with attenuators. It can also be obtained from simulation of a PA model. The W1716 DPD Builder compares the captured output waveform to a desired undistorted passthrough waveform. Based on this, the DPD model is extracted and verified. Next, the DPD+PA response is captured by applying stimulus to the extracted DPD model and downloading the DPD output waveform into the vector signal generator. The PA output waveform is then captured from the vector signal analyzer using VSA software. Finally, the DPD+PA response is verified, and the performance improvements possible with DPD can be shown. An example of the results of this DPD process on a commercial PA is shown in Figure 4.

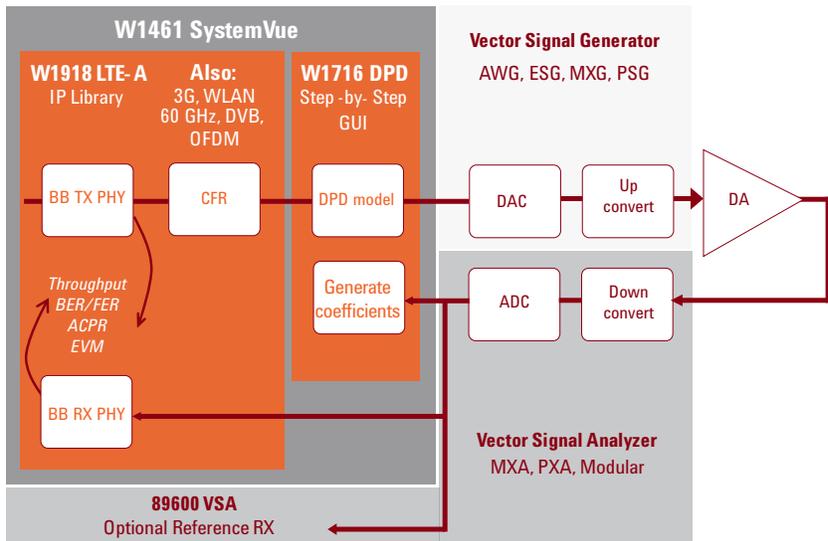


FIGURE 2. In this measurement-based DPD modeling platform, the vector signal generator (e.g., EXG, MXG or PSG) provides the standard-based signals required for component test, while the vector signal analyzer (e.g., MXA, PXA or modular PXI) running Keysight's embedded Vector Signal Analysis (VSA) software captures the signal in order to measure the PA's nonlinearities. Using SystemVue with the vector signal generator and analyzer automates and controls the entire DPD design flow process.



FIGURE 3. Using the setup in Figure 2, the DPD modeling flow is a 6-step process

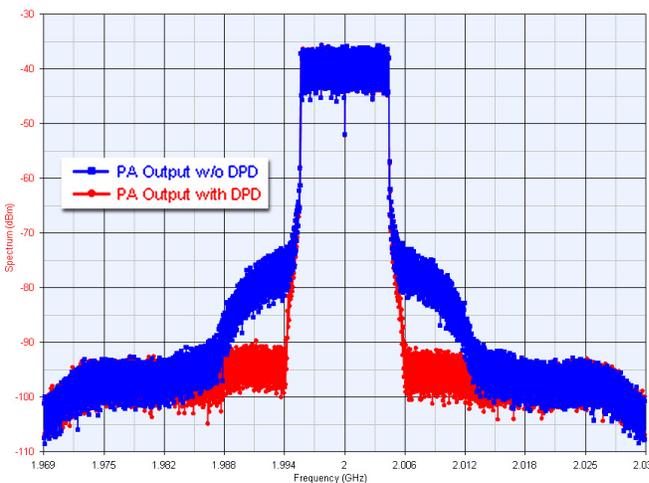


FIGURE 4. This example DPD extraction takes place at RF power = -2.9dbm. The original raw data is displayed in blue, while the DPD +PA output is shown in red.

Including Memory Effects in the DPD Process

An important feature of any PA is memory. The instantaneous output from the PA may depend not only on current samples, but also on past samples. Consequently, the DPD algorithm must account for this behavior, as well as, any nonlinearity. Typically, the memory of a PA is interpreted from the intermodulation levels at the output or by plotting the AM-AM and AM-PM curves.

As previously noted, the input and output waveforms of the PA can be obtained either through laboratory measurement of the actual PA hardware or from simulation of a PA model. If the DPD process is performed on PA hardware in the lab using measurement instruments, the true behavior of the PA (nonlinear behavior and memory effects) is captured. The one drawback, however, is that imperfections from the measurement system (e.g., instruments, cables and adapters) can manifest as memory effects, so care must be taken to isolate any measurement effects from those of the PA.

If the DPD process is performed in simulation, two possible approaches are followed (Figure 5):

- A model of the PA is first created and then the DPD process is applied.
- The actual circuit of the PA in the analog world is co-simulated with the DPD algorithm in the digital world.

When modeling the PA, a number of different modeling approaches can be considered. A polynomial fit model, for example, describes harmonic nonlinearities quite well, but does not fully account for certain RF impairments (e.g., the large signal input and output termination mismatch effects at the fundamental and harmonic frequencies), or capture the PA's memory effects. More complex and advanced PA modeling techniques exist (e.g., the Volterra series, Hammerstein polynomials, Weiner-Hamerstein polynomials, and nonlinear complex envelope impulse response models) to account for PA memory effects. But when well fitted, these advanced models can result in highly complicated poly-

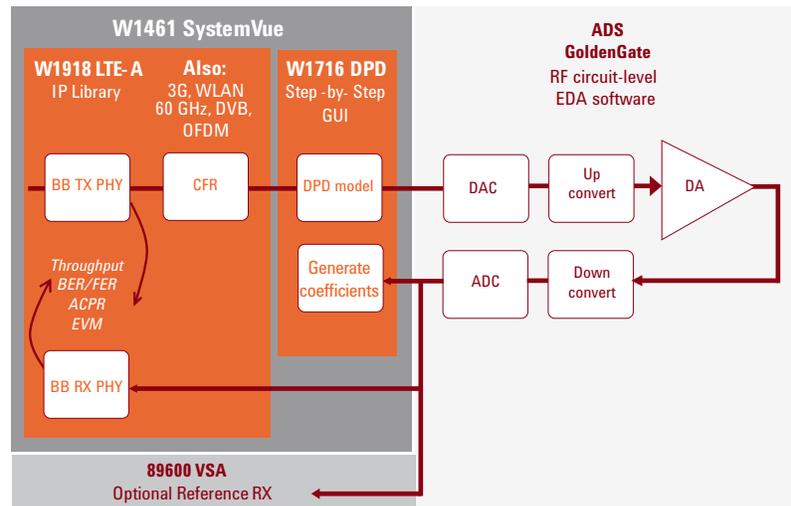


FIGURE 5. With Keysight's simulation-based DPD modeling process, users can look at the simulated PA performance using ADS and Golden Gate circuit envelope simulators even though a hardware PA prototype is not yet available.

nomials with an excessively large number of terms—both of which may negatively impact simulation speed and robust convergence.

A behavioral model of the PA can be created using measurement-based X-parameters*. This type of model offers a highly accurate, modern, stable, transportable, and robustly convergent nonlinear measurement-based representation of the PA's nonlinear behavior. To cover the scope of the model's measurement needs in multiple dimensions (e.g., frequencies, power levels, bias supplies, and input and output load conditions), however, large amounts of data must be collected. And, the model's accuracy is dependent on the number of harmonics covered in measurement. Also, while static memory effects due to PA bias modulation are accounted for, the current implementation of X-parameter measurement-based models is unable to account for longer-term dynamic memory effects.

Another approach, Fast Circuit Envelope (FCE) models, are extracted using the Envelope Transient solver available in Keysight's GoldenGate RF simulation environment, and result in a high fidelity PA model that accounts for both nonlinearities and memory effects. This approach is commonly applied to RFIC designs. The designer simply configures multiple simula-

tions in the dimensions-of-interest, such as power, frequency, bias, source, and load impedances, or any other parameter that can be controlled in the RFIC fabrication or measurement process. This method provides a highly accurate, very quick and robust design and analysis flow for integrating the FCE simulation-based behavioral model within the DPD process. Although, the designer may have to perform a large (one time) number of simulations to capture the required behavior of the PA over the various dimensionalities-of-interest. Also, if it is determined that the scope of the FCE model has to be widened during the DPD process, the entire model extraction process must be repeated.

An optimal means of capturing the complete memory effects in the process of DPD amplifier linearization involves co-simulation with a native RF analog circuit-based model described by the ADS RF analog circuit simulator. ADS features the Circuit Envelope (CE) solver, which incorporates the best features and benefits from both Harmonic Balance (HB) and SPICE solvers. It is ideal for time varying (non-steady state) nonlinear analysis of circuits having both a high frequency (carrier) content and a lower frequency time variation (modulation), such as analog and digitally modulated complex format signals, including wireless standards compliant waveforms.

The main advantage of the CE solver is its efficiency or speed increase over traditional SPICE simulation. Additionally, it features an Automatic Verification Modeling (AVM) or “fast co-sim” option that extracts the nonlinear PA model with only the instantaneous response, neglecting any history and memory effects. Using AVM significantly increases simulation speed and enables much quicker study/analysis of first-order nonlinear PA effects. As an example, Figure 6 shows the AM-AM curves of a co-simulation with a direct, native circuit-level model, with and without AVM.

Summary of Results

As engineers migrate to 4G, choosing/designing the right PA to meet design goals at the lowest possible cost becomes an extremely challenging task, both for PAs in base stations and mobile devices. Because DPD enables the PA to be operated in its high PAE region, near saturation and without significant signal distortion, it provides a viable means for engineers to address many base station/mobile device PA design challenges.

The SystemVue platform with W1716 DPD utility, along with Keysight’s MXG, PXA and PXI modular instruments, provide a way for engineers, at all levels of expertise, to quickly, easily and cost effectively implement DPD in 4G and WLAN communications systems. To fully account for memory effects in the DPD process, the DPD should be performed on PA hardware in the lab using measurement instruments. When hardware is not available, the next most optimal method is to build a DPD algorithm by co-simulating with a circuit-level PA. This method offers both flexibility and accuracy. The DPD architect will understand the margins and limits of the DPD algorithm, while the RF PA engineer will understand how the PA design margins and limits can be improved or modified to achieve more efficient and linear PA output performance.

The Power to Accelerate Wireless Design and Test

Keysight is a leader in wireless test, focused on the highest-performance design and test of wireless devices and networks, with application-focused platforms optimized for existing and emerging standards. Add to this optimal R&D and field support, Keysight allows engineers to better understand the intricacies of the continuously evolving wireless industry so you can accelerate your development of products.

To learn more about Keysight’s suite of test and measurement products please visit: www.keysight.com/find/powerofx

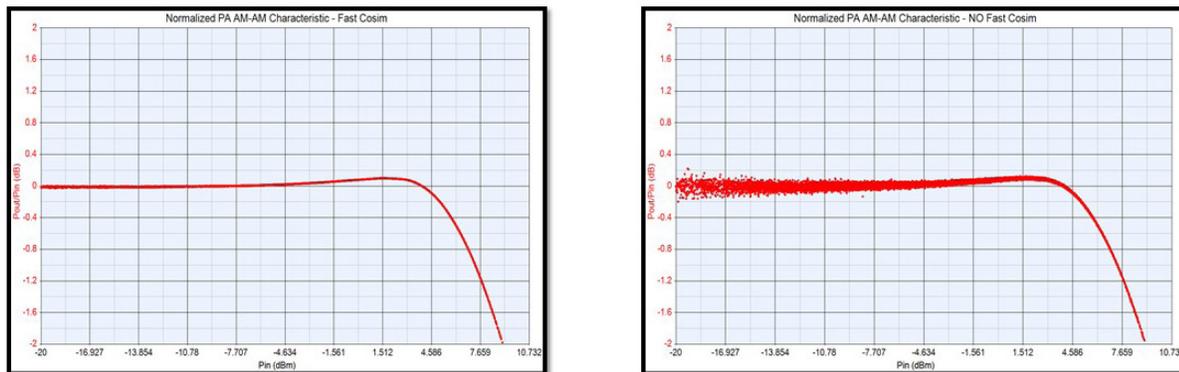


FIGURE 6. The graph on the left shows the AM-AM curve with AVM option on. Note that the model does not capture memory effects. On the right is the AM-AM curve with AVM option off. Note that here, the model does capture memory effects.

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Related Applications

- Wireless base station transmitters
- Handset and mobility chipsets
- Satellite communication links
- Point-to-point terrestrial microwave links
- Military backhaul communication repeaters
- Narrowband radar

Related Keysight Products

- Advanced Design System
- GoldenGate
- Signal Studio
- VSA 89600
- W1461BP SystemVue Comms Architect
- W1716 DPD Builder (SystemVue)
- W1917 WLAN Baseband Verification Library (SystemVue)
- W1918 LTE-Advanced Baseband Verification Library (SystemVue)
- N5182B MXG Vector Signal Generator
- N9030A PXA Signal Analyzer
- M9381A PXI Vector Signal Generator
- M9391A PXI Vector Signal Analyzer

