

Keysight Technologies

Test Coverage:

What Does It Mean when a Board Test Passes?

Article Reprint

Abstract

Characterizing board test coverage as a percentage of devices or nodes having tests does not accurately portray coverage, especially in a limited access testing environment that today includes a variety of diverse testing approaches from visual and penetrative inspection to classical In-Circuit test. A better depiction of test coverage is achieved by developing a list of potential defects referred to as the defect universe, where the capabilities of the chosen test strategy are not considered in development of this defect list. Coverage is measured by grading the capabilities of each test process against the defect universe. The defect universe is defined to be meaningful to the bulk of the electronics industry and to provide a consistent framework for coverage metrics and comparisons.

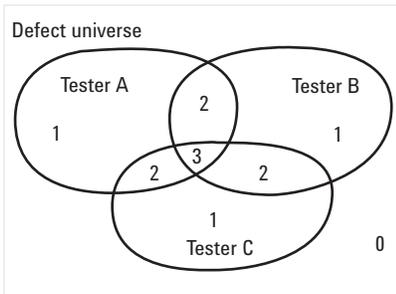


Figure 1. Venn diagram of a defect universe and how 3 different test technologies may cover it. The number of testers that may test a given defect are shown.

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1. Introduction

In the past, relatively few In-Circuit test (ICT) technologies were available for testing boards but the boards had “full” nodal access, typically between 95-100%. This allowed coverage to be intrinsically measured by noting the percentage of board devices that have working tests. Similarly, shorts coverage was simply measured by the percentage of accessible nodes.

$$\text{Device coverage} = \frac{\# \text{ Devices with tests}}{\text{Total \# of devices}}$$

$$\text{Shorts coverage} = \frac{\# \text{ Accessible nodes}}{\text{Total \# of nodes}}$$

This view of coverage had some holes that were simply accepted. For example, a generic resistor tested via an analog measurement was considered well tested. However a digital device was tested with manually derived test vectors, many of which could be discarded due to topological constraints. How good a test was this? There was no guarantee that these vectors actually tested anything.¹ Indeed, real-world studies on thousands of boards (see [Schl87]) have shown how a passing suite of tests does not guarantee a board’s goodness. Other examples of coverage loopholes include:

- Redundant power and ground pins, which are invisible to electrical test methods [Tege96].
- Parallel bypass capacitors, which are also invisible to electrical test methods.
- Open solder joints, which were not specifically tested until the advent of testing techniques such as Unpowered Opens Testing [Park96] and Boundary-Scan [IEEE01].

Over the last decade we saw the advent of limited access boards and limited-access testing technologies designed to regain coverage lost due to lack of access. Now we are seeing boards with much higher access restriction and anticipate that boards with <20% access could be common.

Finally, we are seeing new and radically different approaches to testing boards based on visual and penetrative inspection (AOI² and AXI³). No one approach covers all testing needs, so we need to consider combinations of testing technologies as represented in Figure 1. All of this causes a need to re-examine how test coverage is measured.

1. Sometimes this was addressed by hardware simulation of stuck-at defects on digital inputs and seeing if the test failed. This time-consuming process could only be done after a ‘golden’ board became available.
2. Automated Optical Inspection, a tool that uses visible light.
3. Automated X-Ray Inspection, a tool that uses x-ray radiation.

2. Basic definitions

2.1 Defects and the defect universe

A defect is an unacceptable deviation from a norm. A defect is therefore undesirable and cause for some remedial action, from discarding the board to repairing it. Some examples of defects are:

- An open solder joint.
- A solder joint with insufficient, excess, or malformed solder. There may be no electrical manifestation of this defect.
- A short caused by excess solder, bent pins, device misregistration.
- A dead device. For example, an ESD-damaged IC or a cracked resistor.
- The placement of an incorrect device.
- A missing device.
- A polarized device rotated 180 degrees.
- A misaligned device (typically laterally displaced).

All defects can be enumerated by examining the structural information of the board, typically the bill of materials, netlist and XY position data. This enumeration is called the defect universe. Notice that no assumption of how testing will be conducted is used in developing this list of defects. This is at variance with past practice, where the capabilities of the target test system were considered in this enumeration, as if those untestable defects could not occur.

As soon as a defect universe is proposed, it is possible to postulate defects not included in this set. The goal here with these definitions is to define a defect universe that will be meaningful to the bulk of the electronics industry and provide a consistent framework for coverage metrics and comparisons.

2.2 Test

A test is an experiment of arbitrary complexity that will pass if the *tested properties* of a device (or set of devices) and associated connections are *all* acceptable, and may fail if *any* tested property is *not* acceptable. A simple test might measure the value of a single resistor. A complex test might test thousands of connections among many devices. A typical board test is made up of many simple and complex tests, the collection of which is intended to test as many potential defects as possible. This is called board test coverage (see section 4).

At first it may seem appropriate to ask, “What does it mean when a test fails?” but this question can often be clouded by interactions with unanticipated defects or even the robustness of the test itself. For example, when testing a simple digital device with an In-Circuit test, it could fail for many reasons. Among these are: it’s the wrong device, there is an open solder joint on one or more pins, the device is dead, some upstream device is not properly disabled due to a defect on it, etc.

It is far more meaningful to ask, “What does it mean when a test passes?” For example, if a simple generic resistor measurement passes, we know that a resistor must be present, functioning, in the correct resistance range and that its connections are not open or shorted together.

3. Board test coverage

Board Test Coverage (or simply “coverage”) is defined as a numeric indicator of the quality of a test. This is broken down at the top level into Device Coverage and Connection Coverage yielding two measures for a board.

3.1 Fundamental and qualitative properties

Device Coverage and Connection Coverage can each be broken down into two groups of properties, Fundamental and Qualitative. Fundamental properties directly impact the proper operation of a board. Qualitative properties may not directly or immediately impact board operation, but have the potential to do so at a later time (latent defects), or are indicative of manufacturing process problems that should be addressed before these problems degenerate to the point of impacting fundamental properties.

All properties are judged as “untested,” “partially tested” or “fully tested”. In the untested state, we know nothing about a property. In the partially tested state, we have some confidence that the property exists. In the fully tested state, we have high confidence in the property.

3.2 Device coverage

A device may be *any component* placed on the board, such as a passive component (resistor, inductor, etc.), an IC, a connector, heat sink, mechanical extractor, barcode label, RFI shield, MCM, resistor pack, etc. Basically a device is anything in the bill of materials. Note that the internal elements of an MCM or a resistor pack are not included in this enumeration for coverage. The concept of “intangible devices” is added to this (see section 4.4) to include items like FLASH or CPLD downloads and functional tests of device clusters.

3.2.1

Fundamental properties of devices

The most fundamental property of a device is Presence. Then there is the Correct property, the Orientation property and the Live property. Presence is critical, since the other three properties cannot be measured if the device is missing.

Presence

A test can determine if a device is present. Note that this does *not* always imply that it is the correct device, only that some device is there. For example, a resistor test can verify the existence of a resistor by measuring its value, but it cannot tell from this value if it is a carbon composition resistor or a wire-wound resistor, 10 watts or 0.1 watt. This distinction could have an impact on board performance.

Presence can be judged “partially tested” when there is not complete certainty that the device is there. For example, a pull-up resistor may be connected between VCC and a digital input pin. A Boundary-Scan test may verify the pin is held high, but because this may *also* occur if the pin is open and floating, we cannot be certain the resistor is there.

A variation on presence occurs when it is desired to verify that a device is *not* present, due to a loading option. This is not a new property, but simply an interpretation on presence, the test *fails* when the device is present, instead of passing. Thus a passing test means the device is not present, but that is still a presence property.

Correct

A test can determine if the correct device is present after presence has been determined. For example, an AO system can read the ID number printed on a device, or a Boundary-Scan test can read out the 32-bit ID code inside an IC.

Correctness may be judged “partially tested” when correctness is not assured. Again considering a generic resistor, if its value is correct, we are not completely certain it is the correct device since there are many types of resistors.

Orientation

A test can determine if a device is correctly oriented. Orientation considers rotations of some multiple of 90 degrees that may be possible during device placement. For example, an AOI system can look for the registration notch on an IC. An AXI system can look for the orientation of polarized chip capacitors. An ICT system can verify the polarity of a diode. (Contrast with “alignment” in 4.2.2.)

Live

The concept of “live” (synonym: “alive”) is used in a limited way. Being alive does not mean that all operational and performance characteristics of a device are proven but rather that the device appears to be grossly functional. For example, if a Boundary-Scan interconnect test passes, then the devices that participated must be reasonably alive (their TAPs are good, the TAP controllers work, the I/O pins work, etc.). When one NAND gate in a 7400 quad-NAND passes a test, the IC is rated “live”. If a resistor’s value has been successfully measured, then we feel good that the resistor is alive and is not, for example, cracked or internally shorted or open.

3.2.2

Qualitative properties of devices

We identify only one qualitative device property, Alignment. A device may be displaced laterally by a small distance, rotated by a few degrees (which should not be confused with orientation, which considers multiples of 90 degrees), or ‘bill-boarded’, where the

device is soldered in place but is on its side rather than flush with the board. This displacement may not cause an electrical malfunction but is indicative of a degenerative process problem or future reliability problem.

We use the nomenclature “PCOLA” for the device properties of Presence, Correct, Orientation, Live and Alignment.

3.3

Connection coverage

Connections are (typically) how a device is electrically connected to a board. Connections are formed between device pins and board node pads. (The word “pin” is used even when the device has leads, balls, columns, or other contacts intended to provide connectivity.) Typically this includes solder and press-fit connections. A device may have zero or more connections to the board. For example, a resistor has two connections, and an IC may have hundreds and a heat sink may have none.

A special case of a connection is a photonic connection between a light sensitive device and a photonic connector or cable. While not an electrical connection, the connection is used to transmit a signal. We are beginning to see optical signal paths on boards made up of an optoelectronic transmitter and receiver connected by a fiber optic cable. The cable would be a device, and its two ends would be connections. The connections would be susceptible to opens. There would be no instance of a short in this context except the case where a cable is fastened to the wrong connector.

3.3.1 Fundamental properties of connections

The fundamental properties of connections are whether they are open (no continuity) or shorted (undesired connectivity) to one or more pins or vias on a board. A good connection is *not open* and is *not shorted*. A fundamental assumption here is that bare boards are known-good before valuable devices are mounted on them. Thus there are no node trace defects (shorts and opens, or qualitative items like improper characteristic impedance) intrinsic to the board at the time devices are placed.

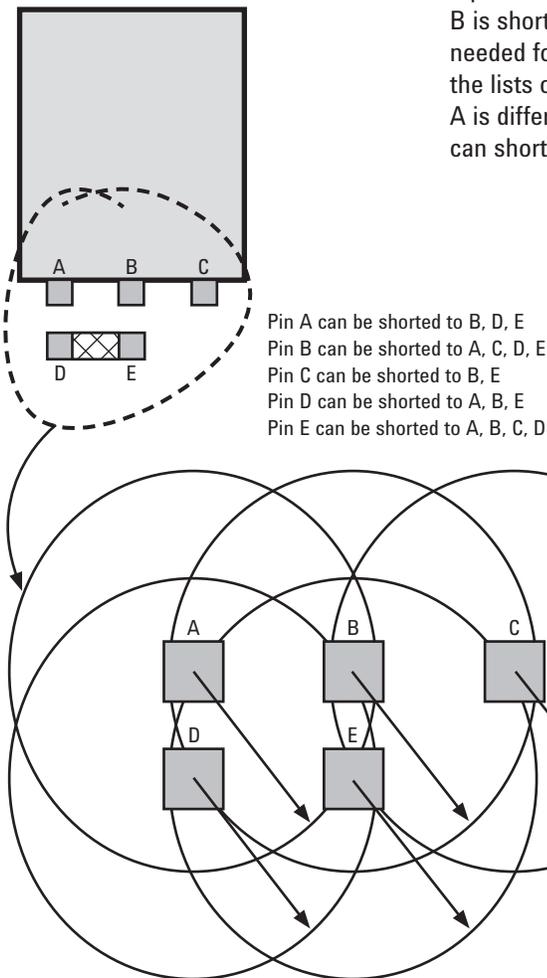


Figure 2. Five pins on two devices and their shorting properties for a given shorting radius.

1. This assumes the nodes are electrically independent. However some devices such as jumpers, closed switches, small inductors, etc. will create a dependency between nodes, that is, an “expected short”.

Shorts

The primary causes of shorts are defects in the attachments, typically bent pins and excess solder. This leads us to a proximity-based model of shorts. If two pins are within a specified “shorting radius” then there is an opportunity for them to be improperly connected and we include these pins in our enumeration of potential shorts that a test should cover. (See Figure 2.) This enumeration is best done with knowledge of the XY location of each pin and the side (top or bottom) the device resides on, and whether it is surface mount or through-hole. A short is a reflexive property of two pins. That is, if pin A is shorted to pin B, then pin B is shorted to pin A. Only one test is needed for the two pins. Do note that the lists of pins that can short to pin A is different than the list of pins that can short to pin B.

Two pins within a shorting radius may be connected to the same node by the board layout. Thus a bent pin or excess solder between these two pins will be electrically invisible. However our enumeration approach will still consider this a potential short that must be covered. Clearly only some form of inspection will see this, and its occurrence, though (usually) electrically benign, still warns of a process problem.

In the past when an electrical tester had full nodal access, the test for shorts merely tested each node for electrical independence from all other nodes.¹ It did not consider physical adjacency and thus it tested for many potential shorts that were essentially impossible in any practical sense. Now that electrical access may be severely limited, there is a collection of more newly developed electrical technologies for detecting shorts. Each technology addresses some subset of board nodes and these subsets are typically disjoint. This causes the question: what potential shorts using the proximity-based model are covered by these tests? The proximity model allows us to measure shorts coverage when disjoint node sets are tested with different technologies. This is done by computing, for each tested node pair, which adjacent pin pairs associated with these nodes are tested.

Open

A pin may not be connected to its board node pad. This is an open condition. Typically an open is complete – there is an infinite DC impedance between the node and pin. There is a class of “resistive” connections that are not truly open and yet may be electrically invisible (to test). These are lumped into the qualitative measure of joints (see next section).

3.3.2 Qualitative properties of connections

The only qualitative property of a connection is the concept of joint quality or simply “quality”. Joint quality encompasses qualitative measures such as excess solder insufficient solder, poor wetting, voids, etc. Typically these defects do not cause an open or short, but indicate process problems that should be flagged. For example, an insufficient solder joint could result in an open joint later in the product’s life. Excessive solder on adjacent IC pads may increase the capacitance between pins, to the detriment of their high-speed signaling characteristics. Improper wetting or voids may cause resistive connections. Certain qualitative defects such as a properly formed but cracked joint are very difficult to test since there may be enough ohmic contact to provide connectivity, yet this connectivity may fail later after corrosion or mechanical flexing. They are typically invisible to any inspection technique.

We use the nomenclature “SOQ” for the connection properties of Short, Open and Quality.

3.4 Intangible devices

A device on a board may have additional features we want to assure are covered, but these may not be, per se, “tested properties”. For example, a board customer may mandate that a FLASH RAM or CPLD have a particular download of bits installed. Thus from the customer’s point of view it is not sufficient to test for device PCOLA and connection SOQ, but s/he may want to assure the presence and correctness of the download bits too. Since these device properties (Presence and Correctness of the download) are intangible, we invent the concept of an “Intangible Device” that must be included in coverage calculations.

This intangible device is related to the actual device by the addition of more activities. In this example, the activities are On-Board Programming processes that install bits and verify their correctness. Once identified, intangible devices and their relevant properties are treated as part of the device space and counted in the coverage, complete with weighting (see 5.4.3). Again using our example of a FLASH download, we would want to test for its presence and correctness. However, orientation, liveness, alignment and also the SOQ properties would be meaningless (weighted at zero).

3.5 Coverage details

At the top level we have device and connection coverage. Drilling down one level, each is composed of fundamental and qualitative factors. Below this we get an explosion of detail. For each device we have five properties and each joint has three. Further, since a pin may be adjacent to several other pins, there may be several potential shorts to cover. This organization is summarized in Figure 3.

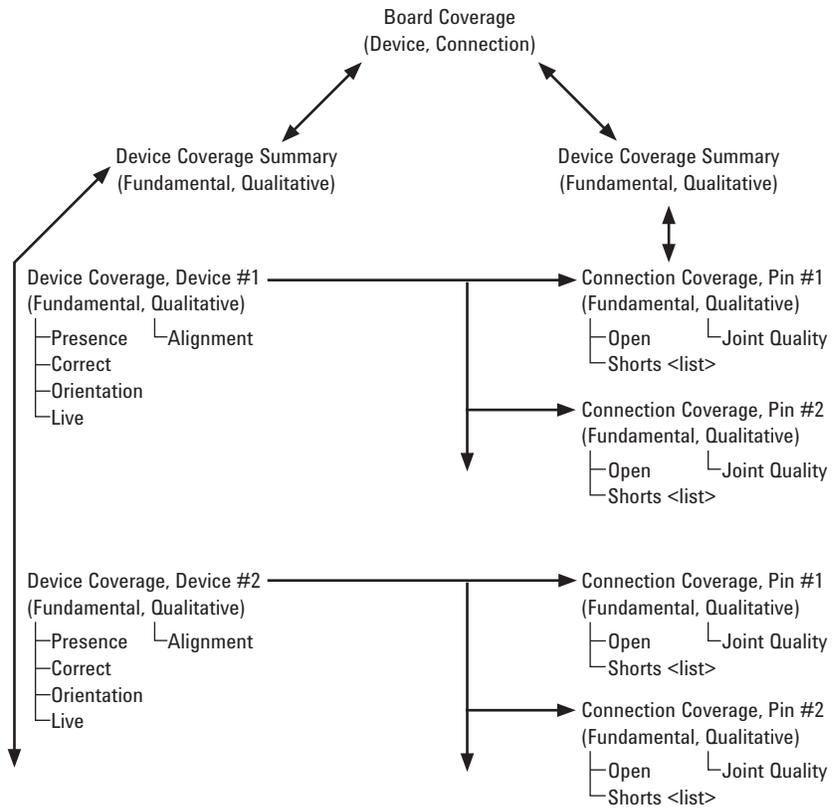


Figure 3. Coverage details and their summarization.

4. A coverage metric

4.1

What Is measured?

A coverage metric should include contributions from every device and connection. This is at variance with past metrics where coverage was measured against “what was possible” to test. Further, every property of a device or connection should contribute to coverage unless it is irrelevant. (An example of an irrelevant property would be the orientation of a non-polarized device like a resistor.) A device is fully tested only when its presence, orientation, correctness, liveness and alignment are all fully tested, and only when, for every pin, there is full coverage for shorts, opens and joint quality. This is an exacting standard.

4.2

Metric scale

It is desired that coverage be scaled such that boards can be meaningfully compared to each other. If a large board possesses thousands of components and many thousands of connections, then each device or connection tested contributes only a small amount of coverage (weighting is discussed later). We choose a large number **Range** = 100,000 for the range (0-**Range**) for two reasons. First, it’s not a single percentage as used in the past. Second, each element of coverage isn’t too small, for example, much less than 1.

4.3

The board score

The board score is a pair of numbers, the first representing device coverage and the second connection coverage: BS = (BDS, BCS). A board would have a pair of numbers for the device and connection score, for example, (76445, 80991), each out of a possible 100,000. A perfect board coverage score would be (100000, 100000). An untested board has (0,0) coverage.

4.4

Device metrics

We want to “score” each device’s tests cumulatively. For example, a device may have its presence tested by more than one test. Say one test gives a “partially tested” score while another scores it as “fully tested”. We take the max() function of these two scores, “fully tested”. If both were partial results, they do not add to a full score. Some tests may not score certain properties at all. Figure 4 shows how a device could be covered by two tests.

4.4.1

Device property weights

The properties of devices can be weighted to place more or less importance between the properties. This weighting can be organized by type of device (e.g., resistors), different from another device type (e.g., ICs). Individual weighting (e.g., per device) is possible if desired.

For a given device type, we assign PCOLA property weights as five fractions that must sum to 1.0. This weighting may vary for other device types. For example, the orientation

weight for a resistor is 0.0 since there is no polarity on a resistor. Thus the other four weights increase in relative importance. The opposite is true for a diode where orientation is important.

An example of how weights might be assigned for an ICT system is shown in Table 1. Note that the qualitative property “Alignment” is given 10% of the weight. Since ICT cannot test for alignment, this means that of the 100,000 score for devices on a board, at most 90,000 can be achieved by ICT and a visual test (probably AOI) is needed to target the remaining score of 10,000. Note that visual test can also achieve scoring for presence, correctness and orientation, but will not get any credit for the live property.

Note also that the rest of the weight (0.9) for fundamental properties is distributed equally across the relevant properties based on whether orientation is important. For non-polarized, symmetric devices like SMT resistors, the orientation property is given no weight at all. For the other devices, orientation shares in the distribution of weight.

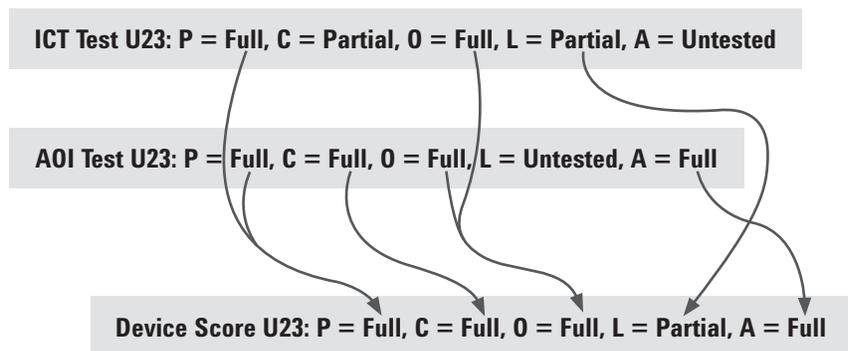


Figure 4. Device property coverage scored by two tests of differing capabilities.

4.4.2

Device property scoring

A test will score against a device PCOLA property as “untested”, “partially tested” and “fully tested”. Assign a value of 0, 0.5 and 1.0 to these respectively. Then the PCOLA device property score for device d is written as:

dps(P), dps(C), dps(O), dps(L) and dps(A) respectively.

Raw device score

For device d the raw device score

RDS(d) is:

$$\mathbf{dps(P)*dpw(P) + dps(C)*dpw(C) + dps(O)*dpw(O) + dps(L)*dpw(L) + dps(A)*dpw(A)}$$

4.4.3

Device type weights

The device types can also be weighted with device type weights. This allows a given device type to be more or less “important” for device coverage. For example, say you are making a board using 1000 surface-mount resistors that have a failure rate of 100 PPM and 100 digital components (average pin count 500) with 5000 PPM failures. You probably are more worried about bad ICs than bad resistors, even though there are ten times as many resistors. Thus weighting the ICs more heavily will cause a test that marginally tests the ICs to look worse than a test that tests ICs thoroughly. Conversely, not weighing the ICs more heavily will cause a board test that thoroughly tests the resistors to look better than it “really is”. In essence, you can weigh the most worrisome components more highly than those you trust. One algorithm for doing this is to normalize the device type failure Pareto diagram onto a unit (1.0) of weight. Another approach would be to use a uniform distribution when no failure history is available.

Device type	Presence dpw(P)	Correct dpw(C)	Orientation dpw(O)	Live dpw(L)	Alignment dpw(A)
Resistor	0.3	0.3	0	0.3	0.1
Capacitor(non-polar)	0.3	0.3	0	0.3	0.1
Capacitor(polarized)	0.225	0.225	0.225	0.225	0.1
Diode	0.225	0.225	0.225	0.225	0.1
Digital IC	0.225	0.225	0.225	0.225	0.1
Etc...					0.1

Table 1. PCOLA device property weights (dpw) for device types for an In-Circuit test system.

4.4.4

Population adjusted device type weights

Next we adjust each device weight to reflect its population on a given board. Say you have 1000 resistors, 100 digital ICs, 200 capacitors and no other device types

Then the weights normally assigned to the other device types can never contribute to the coverage score, meaning a perfect score would be well under 100,000. To redistribute the weight with respect to population do the following:

1. Let N be the total number of devices.
2. Let $n(t)$ be the population of device type t (ranging from 0 to N).
3. Let $dw(t)$ be the device type weight of device type t . Note the sum of all $dw(t)$ is 1.0.
4. Then for all t , $\text{Sum } [n(t) * dw(t) / N]$ and call this the device weight adjuster A .

4.4.5

The board device score

For a given device d , the device score $DS(d)$ is derived from the raw device score, the chosen range and the device weight adjuster A .

$$\mathbf{DS(d) = RDS(d) * Range * dw(t) / (A * N)}$$

Then the board device score BDS is simply calculated as a sum of the device scores:

$$\mathbf{BDS = \text{for all devices } d, \text{ Sum } DS(d)}$$

The value of DS will range from 0 (no devices have any property scores) to $Range$ (all devices have perfect property scores).

4.4.6

Maximum achievable device score

A maximum device property score for an arbitrary device **d** is the **dps(P)**, **dps(C)**, **dps(O)**, **dps(L)**, and **dps(A)** scores that can be theoretically achieved with a given tester. Examples are given in Table 2 and Table 3 for a resistor and a digital device.

This table is filled out very simply, by rating a property “Full” or “Partial” if there is *any* way a given tester can ever score full or partial coverage of that property of that device type. This is independent of considerations such as the testability of a low-valued capacitor in parallel with a large-valued capacitor, or whether a given IC has a readable label but could have a heat sink mounted over it. (This is why it is called “theoretical”.)

Similar to scoring a board with coverage measures derived from an actual test, the maximum possible scores for each device can be plugged into the board device score equations to find out what the best score you can expect for a given tester is. This aids in answering the question, “how good is this tester doing” or “where can I profitably spend time improving coverage”? Because of practical limits (parallel devices, heat sinks, etc) this number is likely to be an asymptote.

Test type	P	C	O	L	A
In-Circuit	Full	Partial	(NA)	Full	Not tested
AOI	Full	Full	(NA)	Not tested	Full
AXI	Full	Not tested	(NA)	Not tested	Full

Table 2. Maximum theoretical device PCOLA scores versus test technology for an arbitrary resistor.

Test type	P	C	O	L	A
In-Circuit	Full	Partial	Full	Full	Not tested
AOI	Full	Full	Full	Not tested	Full
AXI	Full	Not tested	Full	Not tested	Full

Table 3. Maximum theoretical device PCOLA scores versus test technology for a digital device.

Property	Short, cpw(S)	Open, cpw(O)	Quality, cpw(Q)
Weight (s=0)	0.0	0.9	0.1
Weight (s>0)	0.4/s	0.5	0.1

Table 4. Connection property weights.

4.5

Connection metrics

We want to “score” each connection’s tests cumulatively. For example, a connection **c** may have an open tested by more than one test. Say one test gives a “partially tested” score while another scores it as “fully tested”. We take the $\max()$ function of these two scores, “fully tested”. If both were partial results, they do not add to a full score. Some tests may not score certain properties at all.

4.5.1

Connection property weights

A connection **c** may be open, shorted to zero or more adjacent pins, or have a quality problem. We choose weights for each property that reflect their importance. In today’s common SMT technology, we know opens are often more prevalent than shorts so we can weigh opens more heavily.

However note that zero or more shorts may exist for a given connection. We have to adjust the weights appropriately with the population for that connection. This is done by taking the weight we would assign to a single short (0.4 in this case) and in the case of no shorts, adding the weight to the open property. If one or more shorts could exist on a pin, then distribute the weight for shorts among them by dividing by the number of shorts **s**. The SOQ connection property weights **cpw(S)**, **cpw(O)** and **cpw(Q)** are shown in Table 4. The sum of the weights must be 1.0. Ten percent of the connection property weight is given to qualitative issues, so a “fundamental” tester like ICT will at most be able to test 90% of the total possible connection property score.

4.5.2

Connection property scoring

A test will score against a connection joint SOQ property as “untested”, “partially tested” and “fully tested”. Assign a value of 0, 0.5, and 1.0 to these respectively. Then a connection property score for connection **c** is written as **cps(JS)**, **cps(JO)**, and **cps(JQ)** respectively.

A connection score for a given connection **c** called **CS(c)** is the weighted sum of the joint SOQ property scores:

$$\mathbf{CS(c)} = \mathbf{cps(JS)*cpw(JS)} + \mathbf{cps(JO)*cpw(JO)} + \mathbf{cps(JQ)*cpw(JQ)}$$

4.5.3

The Board Connection Score

Given the connection scores for all connections the board connection score is:

$$\mathbf{BCS} = \mathbf{Sum\ for\ all\ c\ of\ CS(c)}$$

4.6

Maximum achievable connection score

The theoretical maximum achievable connection score versus technology is given in Table 5. This can be used to measure the amount of coverage a given test technology is providing versus its theoretical best possible case. Again this does not take into account practical limitations such as parallel power connections on ICs (undetectable by ICT) or joints hidden under BGAs that are invisible to AOI.

Test type	Short, cpw(S)	Open, cpw(O)	Quality, cpw(Q)
In-Circuit	Full	Full	Not tested
AOI	Full	Full	Full
AXI	Full	Full	Full

Table 5. Maximum theoretical connection scores versus test technology

4.7

Deriving scores from tests

The device scores and connection scores are derived from examination of each test. For each test we examine what devices and connections are tested and how well each device property and connection property is tested. Three examples are given below for a digital IC In-Circuit test, a parallel capacitor test, and TestJet test on an In-Circuit tester, where Alignment and Joint Quality cannot be tested. Note that all properties are assumed to be “Untested” until a test scores that property either “Partial” or “Full”. A “max” function is used when more than one test scores a given property, meaning the higher score takes precedent.

4.7.1

Digital in-circuit (excludes Boundary-Scan)

These tests are extracted from prepared libraries of test vectors and often modified based on circuit topology.

Presence (P): if (pin_outputs_toggled > 0) then P = Full.

Note: pin_outputs_toggled is the number of outputs (or bidirectional) pins tested for both output high and low as determined from the test.

Correct(C): if (pin_outputs_toggled > 0) then C=Partial

Live(L): if (pin_outputs_toggled > 0) then L=Full

Orientation(O): if (pin_outputs_toggled > 0) then O=Full

Joint Opens(JO): if (pin_is_output) and (pin_toggled) then JO=Full, else if ((pin_outputs_toggled > 0) and (pin_is_input) and (pin_toggled)) then JO=Partial

Note: input pin opens are never scored better than Partial since:

- fault simulated patterns are extremely rare,
- some test vectors may have been discarded due to topological conflicts (for example, tied pins).

4.7.2

Capacitor test in a parallel network

For capacitors in a parallel network where the equivalent capacitance is the sum of the device values, each capacitor is evaluated as:

Presence (P): if $((\text{test_high_limit} - \text{device_high_limit}) < (\text{test_low_limit}))$
then P=Full

Note: test_high_limit is the higher limit of the accumulated tolerances of the capacitors along with the expected measurement errors of the test system itself. (Similarly for test_low_limit.) The device_high_limit is the positive tolerance of the device being tested added to its nominal value.

Joint Shorts (JS): if $(P > \text{Untested})$ then Mark_Shorts_Coverage
(Node_A, Node_B)

Note: Node_A and Node_B are those nodes on the capacitor pins.
The "Mark_Shorts_Coverage" routine marks *any* adjacent pins on these two nodes as fully covered. This includes pin pairs on devices *other* than the target capacitor(s).

Joint Opens (JO): if $(P > \text{Untested})$ then both connections score JO=Full

Only those capacitors determined as tested for Presence are eligible for Joint Shorts and Joint Opens coverage. Parallel capacitors are not eligible for the remaining properties Correct, Live and Orientation.

The implication of this rule for bypass capacitors is that only the large, low-frequency bypass capacitors will receive a grade for Presence. The smaller, high frequency capacitors will score Untested for Presence. Consider two cases:

1. C1 = 500 nF in parallel with C2 = 100 nF. Both capacitors are 10% tolerance.

C1: $660 - 550 = 110 < 540$ so P = Full

C2: $660 - 110 = 550 > 540$ so P = Untested

In this case only the 500 nF would be graded.

2. Six 100 nF capacitors in parallel, all 10% tolerance.

Cx: $660 - 110 = 550 > 540$ so P = Untested

None of these capacitors would be graded.

4.7.3

TestJet

TestJet tests measure, for each pin on a device, the capacitance between the pin and a sensor plate placed over the device package. Some of the pins of the device can be omitted from testing. TestJet tests are scored for each tested device as:

Presence (P): if $(\text{at_least_one_pin_tested})$ then P = Full

Joint Opens (JO): all tested pins score
JO = Full

In some cases, due to limited access, a TestJet measurement is made through a series resistor connected directly to the device under test. Consequently, properties of the series resistors are implicitly tested. The TestJet pin measurement can only pass if the series resistor is present and connected. Thus the Presence of the series resistor inherits the Joint Open score of the tested pin.

Presence (P): P = JO score of tested pin

Likewise the opens property for each pin of that resistor is implicitly tested by the test of that pin. The Joint Open score for the series component also inherits the JO score of the tested device joint.

Joint Opens (JO): JO = JO score of tested pin

Thus, in a limited access environment, properties of devices not traditionally thought of as test targets may be tested as well. Again, it pays to ask, "What does it mean when a test passes?"

5. Conclusion

This paper has introduced an exacting and testtechnology-independent method for enumerating defects on printed circuit boards and has provided a metric for measuring the coverage of a test or set of tests. This methodology allows for meaningful comparisons of test coverage and can be used to measure the combined effectiveness of complementary test technologies. The use of such a metric can also point out where incremental test generation investment will give the best payoff. This new analysis of coverage is needed to overcome the shortcomings of the "old way" that have evolved, particularly due to limited access test approaches and newer visual inspection technologies.

6. References

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