Defect Coverage of Boundary-Scan Tests: What Does It Mean When a Boundary-Scan Test Passes?

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Abstract

A new coverage definition and metric, called the "PCOLA/SOQ" model, introduced in 2002 [Hird02], has great utility in allowing the test coverage of defects on boards to be measured and compared rationally. This paper discusses the general topic of measuring test coverage of Boundary-Scan tests within this framework. A conclusion is that Boundary-Scan tests offer a large amount of test coverage when Boundary-Scan is implemented on a board, even if that implementation is partial. However, coverage is not perfect for certain defects in the PCOLA/SOQ model, as shown by example.

1 Introduction

The reporting of defect coverage for board tests has previously lacked rigor and usefulness. A new process and metric was introduced at the 2002 International Test Conference [Hird02]. This paper was very positively received at ITC and subsequent venues, suggesting the concepts it defined were long overdue. However that paper, due to space limitations, did not give a comprehensive treatment to Boundary-Scan test coverage. Since Boundary-Scan testing is becoming pervasive, it is the object of this paper to fulfill this need.

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2 Basic Definitions

Some definitions from [Hird02] are repeated here for background.

2.1 Defects and the Defect Universe

A defect is an unacceptable deviation from a norm. A defect is therefore undesirable and cause for some remedial action, from discarding the board, or repairing it, or at the very least, fixing the process step responsible for it. Some examples of defects are:

- An open solder joint.
- A solder joint with insufficient, excess, or malformed solder. There may be no electrical manifestation of this defect.
- A short caused by excess solder, bent pins, device misregistration.
- A dead device. For example, an ESD-damaged IC or a cracked resistor.
- The placement of an incorrect device.
- A missing device.
- A polarized device rotated 180 degrees.
- A misaligned device (typically laterally displaced).

All of these defects can be enumerated by examining the structural information of the board, typically the bill of materials and XY position data. This enumeration is called the defect universe. Notice that no assumption of how testing will be conducted is used in developing this list of defects. This is at variance with past practice, where the capabilities of the target test system were considered in this enumeration, as if those untestable defects could not occur.

2.1.1 Properties of Devices

A device may be *any component* placed on the board, such as a passive component (resistor, inductor, etc.), an IC, a connector, heat sink, mechanical extractor, barcode label, RFI shield, MCM[1], resistor pack, etc. Basically a device is *anything* in the bill of materials. Note that the internal elements of an MCM or a resistor pack are *not* included in this enumeration for coverage. The concept of "intangible devices" is added to this to include items like FLASH or CPLD downloads and functional tests of device clusters. Devices have properties that are tested during production.

The most fundamental property of a device is Presence. Then there is the Correct property, the Orientation property and the Live property. A qualitative property is that of Alignment. Presence is critical, since the other four properties cannot be measured if the device is missing.

1. *Multi-Chip Module, an example of a packaging hierarchy. Another example is a resistor pack containing several resistors. It is a single device, but it may be tested by testing its "child" components.*

2 Basic Definitions

2.1.1 Properties of Devices *(continued)*

Presence

A test can determine if a device is present. Note that this does *not* always imply that it is the correct device, only that some device is there. For example, a resistor test can verify the existence of a resistor by measuring its value, but it cannot tell from this value if it is a carbon composition resistor or a wire-wound resistor, 10 watts or 0.1 watt. This distinction could have an impact on board performance.

Presence can be judged "partially tested" when there is not complete certainty that the device is there. For example, a pull-up resistor may be connected between VCC and a digital input pin. A Boundary-Scan test may verify the pin is held high, but because this may *also* occur if the pin is open and floating, we cannot be certain the resistor is there.

A variation on presence occurs when it is desired to verify that a device is *not* present, due to a loading option. This is not a new property, but simply an interpretation on presence, the test *fails* when the device is present, instead of passing. Thus a passing test means the device is not present, but that is still a presence property.

Correct

A test can determine if the correct device is present after presence has been determined. For example, an AOI system can read the ID number printed on a device, or a Boundary-Scan test can read out the 32-bit ID code inside an IC.

Correctness may be judged "partially tested" when correctness is not assured. Again considering a generic resistor, if its value is correct, we are not completely certain it is the correct device since there are many types of resistors that have the same measured value.

Orientation

A test can determine if a device is correctly oriented, for those devices where this matters. Orientation considers rotations of some multiple of 90 degrees that may be possible during device placement. For example, an AOI[2] system can look for the registration notch on a square IC. An AXI system can look for the orientation of polarized chip capacitors. An ICT system can verify the polarity of a diode. (Contrast with "alignment" below.)

Live

The concept of "live" (synonym: "alive") is used in a limited way. Being alive does *not* mean that all operational and performance characteristics of a device are proven but rather that the device appears to be grossly functional. For example, if a Boundary-Scan interconnect test passes, then the devices that participated must be reasonably alive (their TAPs are good, the TAP controllers work, the I/O pins work, etc.). When one NAND gate in a 7400 quad-NAND passes a test, the IC is rated "live". If a resistor's value has been successfully measured, then we feel good that the resistor is alive and is not, for example, cracked or internally shorted or open.

2. AXI stands for "Automated X-ray Inspection". AOI stands for "Automated Optical Inspection". ICT stands for In-Circuit Test.

2 Basic Definitions

2.1.1 Properties of Devices *(continued)*

Alignment

We identify only one qualitative device property, Alignment. A device may be displaced laterally by a small distance, rotated by a few degrees (which should not be confused with orientation, which considers multiples of 90 degrees), or 'bill-boarded', where the device is soldered in place but is on its side rather than flush with the board. This displacement may not cause an electrical malfunction but is indicative of a degenerative process problem or future reliability problem.

We use the nomenclature "**PCOLA**" for the device properties of Presence, Correct, Orientation, Live and Alignment.

2.1.2 Properties of Connections

Connections are (typically) how a device is *electrically connected* to a board. Connections are formed between device pins and board node pads. (The word "pin" is used here even when the device has leads, balls, columns, or other contacts intended to provide connectivity.) Typically this includes solder and press-fit connections. A device may have zero or more connections to the board. For example, a resistor has two connections, and an IC may have hundreds and a heat sink may have none.

Notice that the purpose of a connection is not considered. For example, the fact that a connection is for power or ground does *not* exempt it from consideration. This also is at variance with the past.

The fundamental properties of connections are whether they are open (no continuity) or shorted (undesired connectivity) to one or more pins or vias on a board. A good connection is *not open* and is *not shorted*. A qualitative property of connections is simply called quality.

A fundamental assumption here is that bare boards are known-good before valuable devices are mounted on them. Thus there are no node trace defects (shorts and opens, or qualitative items like improper characteristic impedance) intrinsic to the board at the time devices are placed.

Shorts

The primary causes of shorts are defects in the attachments, typically bent pins and excess solder. This leads us to a proximity-based model of shorts. If two pins are within a specified "shorting radius" then there is an opportunity for them to be improperly connected and we include these pins in our enumeration of potential shorts that a test should cover. (See Figure 1.) This enumeration is best done with knowledge of the XY location of each pin and the side (top or bottom) the device resides on, and whether it is surface mount or through-hole. A short is a reflexive property of two pins. That is, if pin A is shorted to pin B, then pin B is shorted to pin A. Only one test is needed for the two pins. Do note that the lists of pins that can short to pin A is different than the list of pins that can short to pin B.

2.1.2 Properties of Connections *(continued)*

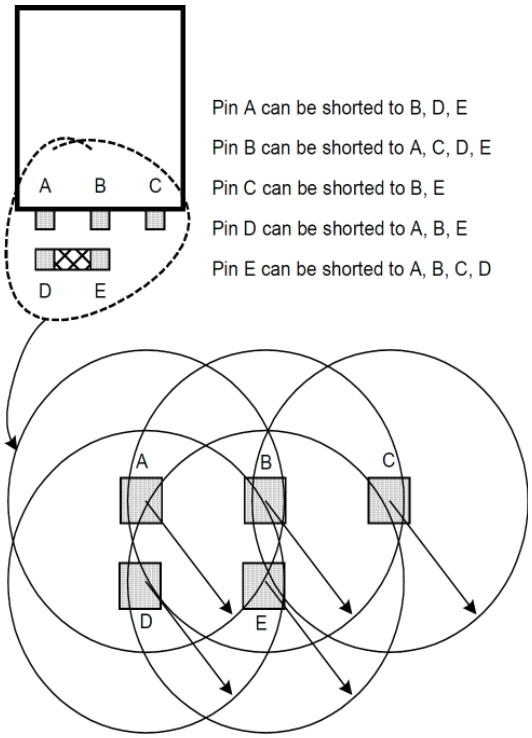

Figure 1. Five pins on two devices and their shorting properties for a given shorting radius.

Two pins within a shorting radius may be connected to the same node by the board layout. Thus a bent pin or excess solder between these two pins will be electrically invisible. However our enumeration approach will still consider this a potential short that must be covered. Clearly only some form of inspection will see this, and its occurrence, though (usually) electrically benign, still warns of a process problem.

In the past when an electrical tester had full nodal access, the test for shorts merely tested each node for electrical independence from all other nodes.[3] It did *not* consider physical adjacency and thus it tested for many potential shorts that were essentially impossible in any practical sense. Now that electrical access may be severely limited, there is a collection of more newly developed electrical technologies for detecting shorts. Each technology addresses some subset of board nodes and these subsets are typically but not always disjoint. This causes the question: what potential shorts using the proximity-based model are covered by these tests? The proximity model allows us to measure shorts coverage when disjoint node sets are tested with different technologies. This is done by computing, for each tested node pair, which adjacent pin pairs associated with these nodes are tested.

3. This assumes the nodes are electrically independent. However some devices such as jumpers, closed switches, tiny inductors, etc. will create connectivity that prevents an electrical test for shorts between two nodes.

2 Basic Definitions

2.1.2 Properties of Connections *(continued)*

Opens

A pin may not be connected to its board node pad. This is an open condition. Typically an open is complete – there is an infinite DC impedance between the node and pin. There is a class of "resistive" connections that are not truly open and yet may be electrically invisible (to test). These are lumped into the qualitative measure of joints (see next definition).

Quality

The only qualitative property of a connection is the concept of joint quality or simply "quality". Joint quality encompasses qualitative measures such as excess solder, insufficient solder, poor wetting, voids, etc. Typically these defects do not cause an open or short, but indicate process problems that should be flagged. For example, an insufficient solder joint could result in an open joint later in the product's life. Excessive solder on adjacent IC pads may increase the capacitance between pins, to the detriment of their high-speed signaling characteristics. Improper wetting or voids may cause resistive connections. Certain qualitative defects such as a properly formed but cracked joint are very difficult to test since there may be enough ohmic contact to provide connectivity, yet this connectivity may fail later after corrosion or mechanical flexing. They are typically invisible to any inspection technique.

We use the nomenclature "SOQ" for the connection properties of Shorts, Opens and Quality. Together, the device properties and connection properties that make up the defect universe are called the PCOLA/SOQ model.

2.2 Tests

The meaning of the word "test" is heavily overloaded in our industry. Here, a test is an indivisible operation that yields (at a minimum) a pass/fail result about the goodness of some portion (large or small) of the component and connection properties of a board. For example, an In-Circuit tester may measure the value of a single resistor on a board. When this test passes, we know the resistor is present, possibly correct, alive and its pins cannot be open or shorted together. (The correct property is "possible" rather than certain because of the wide variety of resistor types we cannot differentiate by value measurement.) In another example, an In-Circuit tester may execute a Boundary-Scan Interconnect test on 100 complex digital devices in concert with thousands of interconnections. Such a test could validate hundreds of device properties and thousands of connection properties.

3 Grading Boundary-Scan Tests

Boundary-Scan tests have the potential to test a large number of properties of devices and device connections. It helps to break down "Boundary-Scan Testing" into a set of constituent activities, and look at each separately. In each case, we ask "what does it mean when this test passes?"

3.1 Infrastructure testing

Infrastructure testing is often referred to as "chain integrity" testing. But it may imply more. The simplest integrity test manipulates the "chain TAP" signals (at a minimum, the TCK, TMS, TDI and TDO signals) and it passes if a series of actions performed while the chain is in mission mode all result in proper data being observed at the chain TDO pin. Many people think of a Boundary-Scan chain as the simple structure seen in Figure 2.

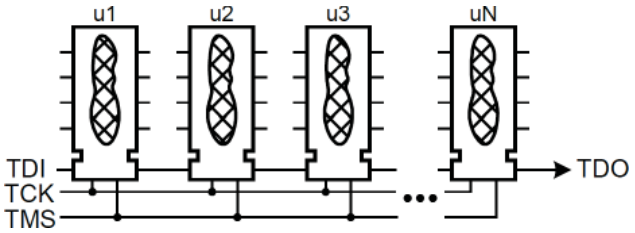

Figure 2. Simple Boundary-Scan chain.

When a well-constructed integrity test [Park03] runs, it manipulates the TAP signals to read out Instruction register capture bits, IDCODE bits and bypass register bits, etc. If all these bits come out as predicted, the test passes. What does this say about the defects that could occur? For each of the ICs, the passing integrity test tells us this:

- It is present (fully tested).
- It is correct (fully tested if IDCODE is read, partially otherwise).
- It is properly oriented (fully tested).
- It is live (partially tested, only the TAP is used).
- Alignment is untested.
- Shorts between its TAP signal pins are fully tested.
- Opens on all its TAP pins are fully tested.
- Joint quality is untested.

Thus a passing integrity test tells us a lot about the fundamental properties of each device in the chain, and all the device TAP pins (but nothing about the qualitative properties). Note we only award full coverage to device correctness if the device contains an IDCODE we can read out. Otherwise, it might with some probability be a similarly pinned device (e.g, the 74bct8374 versus the 74bct8373). We also take a hard line that because the TAP pins constitute a small fraction of the device's pins, the 'Live' property is only partially tested.

3 Grading Boundary-Scan Tests

3.1 Infrastructure testing *(continued)*

On "real" boards, some chain TAP signals are likely only to be accessible on the upstream side of distribution buffers. There will be some ICs with TRST* signals, and some may have compliance enable pins that must be conditioned for the chain to work. (See Figure 3. Note only the labeled nets have tester access.) The TRST* and Enable lines must be held constant during testing, so they are not being tested themselves, but if the test passes, we can know some things about them, but not other things. For example, the TRST* line *might* be open or maybe not. It depends on how it floats. It could be shorted to a logic 1, but the tester would not be certain to see this. Thus, we could declare the TRST* pin partially covered for opens and some shorts. (Ditto for the Enable line.)

The two buffer chips, b1 and b2 must be free of opens, or the test could not work. However, quite a few potential shorts would not be detected. Further, since b1 and b2 may be more than just simple buffers, tester software might not be able to determine what defects among them potentially could be present.

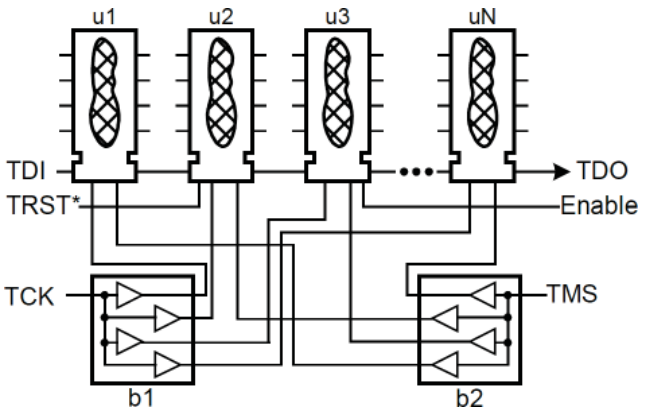

Figure 3: A "real" chain.

Buffers b1 and b2 also can be graded for PCOLA similar to the Boundary-Scan ICs. Thus quite a bit of "extra" coverage can be claimed for this very simple integrity test. But there is more. If between each buffered output of b1 and b2 there were a series termination resistor to dampen reflections, what would be the PCOLA/SOQ scoring for them? For each such resistor the passing integrity test would tell us this:

- It is present (fully tested).
- Nothing can be said about correctness.
- Nothing can be said, or matters, about orientation.
- It is live.
- Alignment is untested.
- Shorts between each resistor's pin pair are untested.
- Opens on either pin are fully tested.
- Joint quality is untested.

3 Grading Boundary-Scan Tests

3.1 Infrastructure testing *(continued)*

Thus implicit coverage of many resistor properties would be gained from this Boundary-Scan integrity test. Integrity testing of Boundary-Scan devices is almost always a default activity of any other more aggressive Boundary-Scan test. Some testers break out the integrity test as a stand-alone test unit for better diagnosis, but nearly any defect that would fail an integrity test would also cause any other Boundary-Scan test to fail as well. This is not "redundant" testing, but rather, a strategy for better diagnostic resolution.

3.2 Interconnection Tests

Next consider a Boundary-Scan Interconnect test, one that tests signal pathways between Boundary-Scan ICs. See the simple example in Figure 4. Note the infrastructure is simplified, and assumed here to be tested by a separate integrity test.

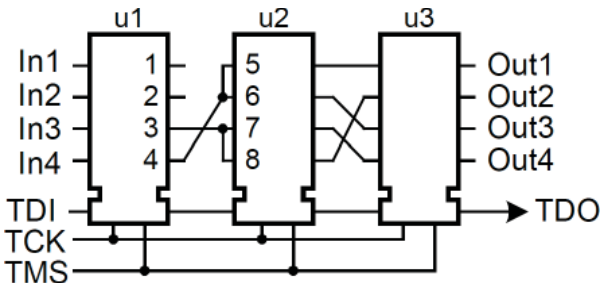

Figure 4. Interconnect testing.

The nature of "interconnect" test [Park03] is to focus on wire paths between Boundary-Scan ICs. For example, simple point-to-point wiring between u2 and u3 is tested for both opens and shorts between any pair of pins on either IC, regardless of their relative proximity. But the wiring between u1 and u2 requires a bit more analysis. For example, there is a wire between pin u1.3 and u2 pins 7 and 8. Those pins will be completely tested for opens. However, a potential short between u2 pins 7 and 8 will not be tested.[4] The PCOLA/SOQ model counts this as a potential defect. The fact that Boundary-Scan cannot test this case does not make it less of a defect. (Note an X-ray or vision system would detect it.)

Similarly, what about a short between u1, pins 1 and 2, or pins 2 and 3? Detection of these will be a function of the Boundary-Scan implementation of pins 1 and 2. If they are output pins only, then the short from 1 to 2 will be undetectable. A short from 2 to 3 might be detected if pin 2 can disrupt data on pin 3. If the Boundary Register cells on u1 pins 1 and 2 are self-monitoring, then we can detect these two shorts.

We cannot tell if u1 pins 1 and 2 are open with Boundary-Scan. While there is no electrical consequence to either of these opens, they are still defects. It is easy to imagine how mechanically unsecured IC leads could be bent and cause shorts at some later time.

4. *In these discussions, sequentially numbered pins (like 7 and 8) are assumed be physically adjacent and thus able to short.*

3.2 Interconnection Tests *(continued)*

If the signals In1 through In4 and Out1 through Out4 are controlled and observed by an ATE system, then opens and shorts on them will be tested.[5] Note the shorts may be tested by an unpowered shorts test done between the tester's access probes before power is turned on.

With respect to PCOLA attributes on u1, u2 and u3, the infrastructure test left us with only partial coverage for the "Live" property. By virtue of a passing interconnect test we award full coverage to "Live" for all the ICs, since a significant fraction of their signal pins (beyond the TAP pins) have been shown to work. Thus we see in this simple example, that Boundary-Scan can give powerful defect coverage, but it may not be perfect.

Most logical depictions of Boundary-Scan circuitry omit the power and ground connections. However, Boundary-Scan interconnection tests will also detect shorts between such pins and the set of interconnection nets being tested as seen in Figure 5. Since power and ground pins have become a large fraction of *all* pins on digital devices [Tege96] this coverage is very significant. In this example, shorts between u1 pins 1 and 2, 2 and 3, 3 and 4 and 4 and 5 are detected. Similarly the shorts between u2 pins 8 and 9, 9 and 10, 10 and 11, and 11 and 12 are detected. Note that u1 pins 4 and 5 plus u2 pins 11 and 12 are shorts that affect the infrastructure and would cause integrity failures as well.

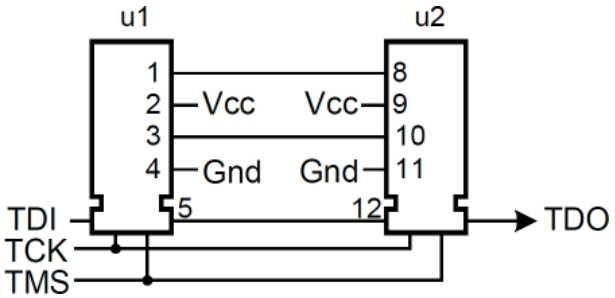

Figure 5. Interconnect tests also detect shorts between Boundary-Scan signals and power pins.

5. 5 Some testers integrate the testing of board I/O with the general interconnect test algorithm. Others break this type of testing out as a separate test activity. Some testers (typically the "4-wire" types) have no test for these signals with subsequent loss of coverage. Here we consider it as one integrated test.

3.2 Interconnection Tests *(continued)*

Figure 6 (where only the TAP signals are accessible) shows some more situations where grading coverage may be "interesting".

Two digital devices with Boundary-Scan are connected, but there are some resistors there too. The net from u1, pins 1 and 2 (both are drivers) and u2.5 also has a pullup resistor (r1) to Vcc. Any opens on the IC pins will be detected by Boundary-Scan. The question is, what happens if there are opens on the resistor r1's pins? This depends on whether r1 is part of the "logic" of the net's behavior. For example, if the two outputs on u1 are both open-collector-type outputs, then the high state of the net is actually provided by r1 when u1 is not pulling the net low. In this case, opens on r1 are detectable. However, if r1 is there to establish a logic high when u1's drivers are disabled to a high impedance state, then we can't say with certainty that any opens on r1 would be detected. This is because the receiver may interpret a "High-Z" on its input as a logic 1 with some probability.

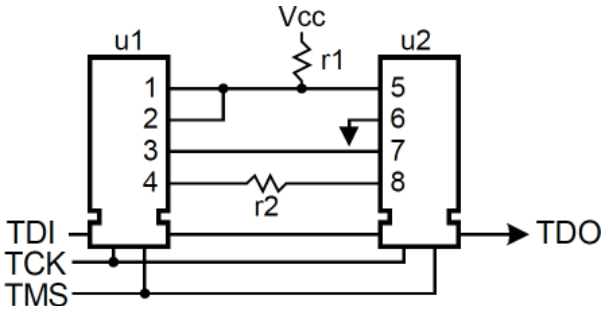

Figure 6. More interconnections for testing.

Continuing with Figure 6, an open on input signal u2.6, which is tied to ground, might not be detectable if the input interprets a dangling input as a logic 0 with some probability. Often times, these interpretations are a function of unspecified parameters such as input leakage currents, which over time may establish a logic state as perceived by the receiver. In these cases where we cannot know with certainty that a defect would be detected, we award only a "partial" coverage value to the opens in question. Note that power and ground pins on any of these ICs that are adjacent to Boundary-Scan-tested nets will cause the test to fail if there is a short between them.

Next in Figure 6 notice that there is a series resistor r2 between u1.4 and u2.8. When the Boundary-Scan interconnect test passes, then r2 must have been present, and its pins could not have been open. However, r2 could be the incorrect value without the test failing, and a short across r2 would most likely be invisible. So we get "full" coverage for Presence and Opens, but no coverage of Correct and Shorts properties. We can "fill in" coverage for correctness by using other techniques, notably a "coupon test" where other identical resistors are measured for their correctness (this could be done with an In-Circuit resistance measurement). By agreement with the pick-and-place engineers, the resistors measured would be the first and last resistors of that type placed on the board, to assure the correct reel(s) of resistors was used throughout placement.

3 Grading Boundary-Scan Tests

3.2 Interconnection Tests *(continued)*

Finally in Figure 6 we may have been hasty in declaring opens coverage for u1 pins 1 and 2. To declare either open covered, the test must have enabled one pin to drive the net while the other was disabled, and both logic states driven and received. But this might not be possible if the Boundary-Scan implementation of u1 creates a masking condition [Park03]. Masking occurs when a single output driver enable control cell fans out to both drivers (pins 1 and 2). It is not then possible to enable one pin exclusive of the other. If both must be enabled simultaneously, then a well-constructed Boundary-Scan test must match the data in the two driver data cells to avoid driver conflicts. Thus either open would not be detectable.

Note that if r1 is shorted, this will prevent the net from achieving a logic low state and this defect would be covered. Similarly, if u2 pin 6 (tied directly to ground) is shorted to either of its neighbors, this would be detected too by virtue of their nets not being able to achieve a logic high state. Again, Boundary-Scan can provide impressive coverage of defects, even for seemingly "unaddressed" devices (like the resistors in Figure 6), but this cannot be accurately measured without some circuit analysis.

3.3 Coverage of Cluster Tests

A Boundary-Scan "cluster" test is a test of a non-Boundary-Scan device conducted with some collection of Boundary-Scan and conventional ATE resources. In the most extreme case, the non-Boundary-Scan device is tested with Boundary-Scan resources alone, and no other resources. See conventional device d1 in a configuration to be tested by Boundary-Scan devices u1 and u2 shown in Figure 7.

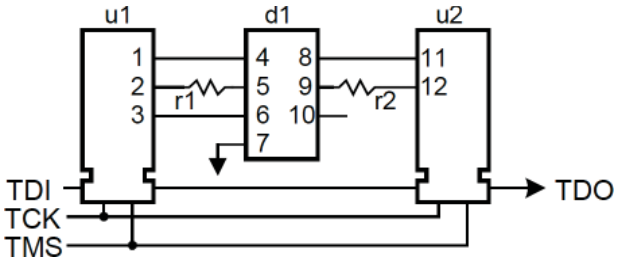

Figure 7. A conventional device (d1) surrounded by Boundary-Scan resources.

3.3 Coverage of Cluster Tests *(continued)*

We start by looking at device d1, the target of this test. If we were using a conventional In-Circuit tester, we would have test probe access to the seven pins of d1. We would also have a previously prepared set of test vectors for d1 that were guaranteed to exercise some of the logic of d1, and also to propagate the effects of defects (like simple opens) from *any* pin to some tester receiver. This includes defects on inputs (pins 4-7) as well as defects on outputs (pins 8-10). When such a conventional test was graded against PCOLA/SOQ, we would get:

	Device d1	
P	Full	
C	Full*	
O	Full	
L	Full	
A	Untested	
	d1 Inputs	d1 Outputs
S	Full **	Full **
O	Full ***	Full ***
Q	Untested	Untested

* *Full coverage of correctness, due to similar devices with identical pinouts having vectors to discriminate between them. Consider the '373 and '374 registers as examples.*

** *Shorts tested by virtue of probe access using unpowered shorts testing. See discussion.*

*** *Pin opens tested by virtue of the guaranteed defect coverage of the test vectors.*

This is a very high quality test (mainly due to the guarantee of high-quality vectors) that gets maximal In-Circuit test coverage for the device. Such tests in reality are rare for a number of reasons, from lack of documentation (such as a simulation model) of the device, to lack of time to produce such a detailed test. But even if such a test did exist, it would have to be modified in the case where one of d1's inputs was tied to ground (as in Figure 7) and one of its outputs being inaccessible for test. The modified test (assume the modifications are done with far less information[6] than the original author had) still has to work for good devices. The result is some loss (we assume here a partial loss) in potential coverage:

6. *Indeed, at least one ATE system performs these modifications automatically with no knowledge of the device function. It does this by deleting logical, independent sectors of the test, and by ignoring expected states for inaccessible outputs.*

3.3 Coverage of Cluster Tests *(continued)*

	Device d1	
P	Full	
C	Partial	
O	Full	
L	Full	
A	Untested	
	d1 Inputs	d1 Outputs
S	Full *	Full *
O	Partial **	Full/Partial ***
Q	Untested	Untested

* *Shorts tested by virtue of probe access using unpowered shorts testing. See discussion.*

** *Input pin opens partially covered on inputs because we have lost the propagation guarantee.*

*** *Output pin opens fully covered only if the remaining test drives an output to both states. Note, inaccessible outputs are untested.*

Note that shorted pins have been covered by other means, but they could have also been covered by the guaranteed test if for every shorted pin pair, the effects of the short were known to propagate to a tester receiver. In the case of the modified test, this guarantee is lost.

To continue the example in Figure 7, we now have the same device, with one input grounded and one inaccessible output, tested with only Boundary-Scan resources. We will assume the Boundary-Scan drivers are not self-monitoring for now, so they cannot monitor for shorts between input pins on d1. Thus, all conventional shorts testing is no longer possible due to lack of access.

With these conditions, we now ask what defect coverage for d1 would be possible. This is summarized as:

	Device d1	
P	Full	
C	Partial	
O	Full	
L	Full	
A	Untested	
	d1 Inputs	d1 Outputs
S	Untested/Partial *	Untested/Full **
O	Partial ***	Full/Partial ****
Q	Untested	Untested

* *Shorts untested if adjacent pins never reach differing states. Partially tested only if they do reach different states, but no guarantee they will be propagated.*

** *Output shorts only detected on the observed outputs, if they drive differing states.*

*** *Input pin opens partially covered on inputs because we have lost the propagation guarantee.*

**** *Output pin opens fully covered only if the remaining test drives an output to both states. Note, inaccessible outputs are untested.*

3.3 Coverage of Cluster Tests *(continued)*

From these charts we see that some defects will lose degrees of coverage depending on test constraints imposed on the original test vectors by topological restrictions (tied/inaccessible pins). We have assumed here that the restrictions are not fatal to the entire test, but invalidate (and hence discard) only a portion of it. Since we typically can no longer know the exact coverage of the remainder, we have to back off on coverage expectations.

We also see some degradation of test coverage because the In-Circuit tester no longer has access to device pins on d1. With this access missing, some degree of shorts coverage is no longer possible. Some of this shorts coverage could be restored if the driver IC u1 had self-monitoring output drivers. If a short occurred that caused these drivers to conflict with each other, that could be detected. Again, that is a function of the quality of the remaindered test vectors.

Note also in this example, there are two series resistors. If a short occurred on the u1 output side of the resistor r1, we have a better chance of detecting it since it would cause a drive conflict in u1 that could be observed with self-monitoring outputs. If a short occurred on the inputs to d1, then they may *not* cause an observable conflict. Thus, some IC pin shorts may or may not be detectable due to the series resistor. Of course, a short across r1 will be undetected, but an open on either of its pins would "inherit" the coverage of d1 pin 5.

Inherited coverage allows us to claim some coverage on both u1 and u2. If we believe that d1.6 is covered for opens, then u2.11 is given an equivalent coverage for opens. Similarly, if d1.6 is partially covered for opens, then u1.3 is too. If d1.9 is covered for opens, then r1's pins and u2.12 are also similarly covered.

Again, we see a lot of good defect coverage comes from Boundary-Scan cluster tests, but it's not perfect and cannot be completely or accurately evaluated without some analysis of the circuit topology.

4 Coverage Comparisons

Consider three boards: 1) a board with complete nodal access but no Boundary-Scan; 2) a board with 50% nodal access and no Boundary-Scan; and 3) a board with 25% nodal access, and 50% of the ICs contain Boundary-Scan. Except for these noted differences, these boards are otherwise similar, containing a mixture of analog and digital circuits. In each case, the boards are tested with a full-featured In-Circuit tester. We also assume that a reasonable effort has been made to optimize coverage, that is, there was no other schedule or budgetary reason to reduce coverage. What might be the coverage implications attributable to their differences?

4.1 Board 1

This board is exemplary of boards that existed around 1990, before Boundary-Scan became available and while complete nodal access was still achievable. Due to full In-Circuit access, all components are testable[7] to some degree. In general, the PCOLA-SOQ scores for devices will be near maximal for PCOL (no score for A) and SO (no score for Q). Correctness of digital components could be scored at "Partial" since no concept of an ID Code inside a device is available. We also expect to see coverage missing for opens on IC power and ground pins, which in 1990 were a relatively small percentage of all pins, but are an important category now. There is also a lack of PCOLA coverage on certain parallel devices, notably, bypass capacitors connected across power and ground planes. This occurs because the accumulated uncertainty of the summed capacitor values will usually greatly exceed the individual values of the smaller (RF) capacitors. On these devices, we get almost no score, except for shorts coverage across their pins. Any of these devices could be completely missing without the test failing. Except for these few, focused points, this board has a very good overall PCOLA-SOQ score, near the maximum possible for ICT by itself.

4.2 Board 2

This board might have been prevalent in 1995, before Boundary-Scan acceptance had really taken hold, but access was in serious decline. Now, full-featured ICT machines were struggling to maintain coverage. New technologies like capacitive lead-frame testing[8] were developed to try to fill in coverage. Such technologies were somewhat more forgiving of access restrictions and are categorized as "limited access test" technologies (as is Boundary-Scan). Critical access analysis became important in board design, so that "every probe counts" to best effect.

Digital and analog IC tests are particularly sensitive to access restrictions. If you have a marvelous digital test for a device, but can get access to all but one of its inputs, the test most likely cannot be executed in full, or likely, even in a partial, reduced form either. Thus entire IC tests may be invalidated. In the Machiavellian worst case, you'd lose 100% of your IC tests due to these access restrictions.

7. *Here we assume that all analog components are testable, that is, no extreme-valued components exist, for example, picofarad capacitors or nanohenry inductors.*
8. *This technique, popularly known as "TestJet" ® is focused on testing for opens on IC pins. It is an unpowered technology, that doesn't care if the IC under test is digital, analog or mixed signal. If some IC signal pins are inaccessible, the technique will still work on those that are left. It cannot test for opens on power and ground pins.*

4 Coverage Comparisons

4.2 Board 2 *(continued)*

Similarly, if a simple resistor test requires probes on both terminal nets, there is a significant chance that many analog devices will no longer be testable. Let's say that 25% are now untested. Finally, shorts testing is done by a process that works on probed nets only. Thus 50% of the nets can no longer participate for another serious coverage hit. Board 2 will have a severe loss of coverage, even if critical access analysis is performed during design.

4.3 Board 3

Now we move to the year 2000. We have even less access now, but 50% of the ICs contain Boundary-Scan. We have seen now Boundary-Scan can test device properties (even the "Correct" property to "fully tested" when ID Codes are implemented) and a multitude of connection properties on the Boundary-Scan devices. But the foregoing discussion also shows how non-Boundary-Scan devices, even resistors also can gain significant coverage from Boundary-Scan tests, with no probes at all. Knowing this, we can improve our critical access analysis to focus on those defects that Boundary-Scan truly cannot help with. It is quite possible to then approach coverage levels that we saw in 1990 on Board 1.

4.4 Future Boards

This analysis can be extended to future boards where we expect to see even less nodal access (say, 10%) but more adherence to limited access test technologies such as Boundary-Scan. As access declines, simple, digital Boundary-Scan will suffer coverage losses for boards with significant analog and mixed signal content. This can be redressed with the application of IEEE Std 1149.4 and 1149.6 [IEEE99], [IEEE03], [Park03], or by making sure that whatever access is still available is concentrated in areas where digital Boundary-Scan coverage is weak. This requires an accurate assessment of test coverage, as supplied by the PCOLA/SOQ model [Hird02].

5 Conclusion

Boundary-Scan testing can offer a great deal of high quality defect coverage as measured by the PCOLA/SOQ model [Hird02], including cases where the board has non-Boundary-Scan components being tested as clusters, or inherently tested as for passive devices in series connections, or in pull up/down connections. Measuring this coverage does take care so as to not over/under state it, and this involves some degree of circuit analysis. However we can conclude that as board access declines, Boundary-Scan will hold coverage levels to much higher levels than almost any other electrical technique available. However, we can also see how poor DFT in a design can cost us dearly, if it impedes our ability to use the Boundary-Scan toolset.

6 References

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