Testing DDR Memory; How On-Chip DFT Helps

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Testing DDR Memory; How On-Chip DFT Helps

John Pendlebury
970-679-5703 Agilent Technologies
900 S. Taft Ave
Loveland, CO, 80537
john_pendlebury@agilent.com

Testing DDR memories on Printed Circuit Boards has steadily gotten more difficult. Most such memories do not have any on-chip Design-for-Test features. Adequate test access is a disappearing luxury. It is a challenge to present these memories with the critically timed protocols they require to work at all, and, to participate in their test. While Boundary Scan technology (in the memory controller devices) can assist with the access problem, it is increasingly difficult to achieve the required protocols in the serialized environment of Boundary Scan.

DDR memory vendors have been loath to provide on-chip test assistance (DFT), but one example of a graphical RAM with DFT does exist. There is also a newly published IEEE Standard 1581 that offers a way to add DFT to RAM devices, with or without adding new pins to the device. These capabilities dramatically reduce the difficulty in creating stable, reliable, repeatable tests for DDR memories at board test.

The presentation will include a discussion of the DDR memory challenges we see today, and how the adoption of DFT capabilities pays off in higher test coverage, better diagnostics and reduced programming/support time.

Paper Outline

DDR Basics

In order to appreciate the benefits that can be gained by adopting DFT facilities on DDR Rams it is first necessary to understand some of the issues that In-circuit test engineers face when trying to develop tests for these devices. We shall look at the theory of operation of DDR memories in order to understand their complexity and then highlight some of the challenges that this complexity creates for both In-circuit and Boundary Scan testing. We shall then draw a comparison with the relative ease with which a test can be developed for a DDR memory with DFT, specifically a Graphics DDR3 memory with a JEDEC approved test mode.

DDR Operation

In order to test a DDR memory using conventional vector based test methods then a complex initialization sequence and command structure must be followed. A simplified operation state diagram for a DDR3 is shown below.

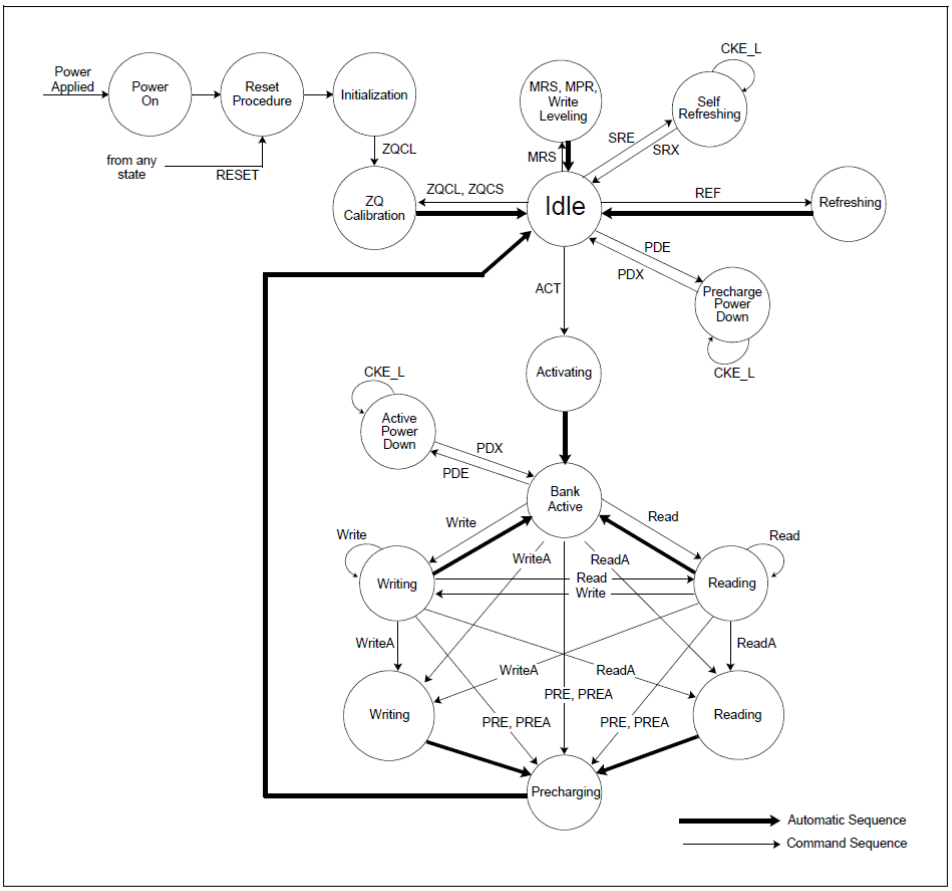


Figure 1. Simplified State Diagram

In order to successfully read from a DDR memory a lengthy initialization sequence involving the programming of the device's mode registers must be done, data can then be written to the device and only then can a read instruction be executed which is the first time in the test sequence that the test engineer will be able to validate that the preceding initialization sequence and write commands have in fact executed successfully.

Devices must be programmed in 'bursts' of 2, 4, or 8 address locations at a time, the cross point (Vix) of the positive and negative clock inputs must also be closely controlled in order to successfully test the device. This cross point setting is illustrated in the following diagram:-

4.4 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) must meet the requirements in Table 22. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS

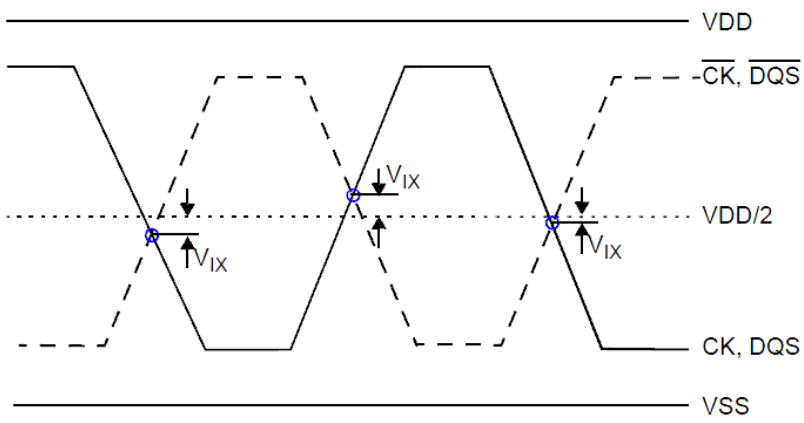


Figure 90. Vix Definition

Table 22. Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	DDR3-800, 1066, 1333, & 1600		Unit	Notes
		Min	Max		
V_{IX}	Differential Input Cross Point Voltage relative to VDD/2 for CK, $\overline{CK}$	-150	150	mV	
		-175	175	mV	1
V_{IX}	Differential Input Cross Point Voltage relative to VDD/2 for DQS, $\overline{DQS}$	-150	150	mV	

Notes:

This level of complexity creates a number of challenges when trying to develop tests for these devices which we shall now look into.

Challenges for In-circuit test.

DDR memories typically have a minimum data rate or clock speed that far exceeds the capabilities of In-circuit testers or indeed of Boundary Scan test systems, this minimum data rate can be addressed by operating the device under test in “DLL off” mode, which allows for much lower clock speeds which are well within the capabilities of In-circuit or Boundary Scan test systems. However running a DDR memory in “DLL Off” mode makes significant changes to the way in which the device responds to the latency parameters (CAS Latency & Additive Latency) programmed into its mode registers. It is also an optional feature for DDR memories and may or may not be supported by your chosen manufacturer or on your chosen device. If a “DLL Off” mode cannot be selected then testing the DDR memory at low speed can cause unpredictable behavior, resulting in unreliable tests.

In-circuit test fixture noise pickup must also be considered. More and more printed circuit boards are using switched mode voltage regulators rather than linear regulators. If these regulator circuits have test access and are probed in the test fixture then noise can be picked up on these probes and transmitted to the digital drivers and receivers used to test the DDR memory. Because of the relatively long vector sequences then this can cause DDR tests to fail intermittently. Resolving this issue may involve the use of dual stage test fixtures or the removal of test probes from the voltage regulator circuits with a resulting reduction in test coverage.

It may also be problematic to create a single test that accommodates all the various memory vendors that are used on any given circuit board. While memories from different vendors must meet the same JEDEC specification there is considerable leeway in how these specifications are applied and therefore it cannot be guaranteed that one vendors chip will operate in an identical way to another’s.

Challenges for Boundary Scan test

When writing to a DDR memory cell we are effectively charging that cell, and all programmed cells on a DDR memory must be recharged periodically. If this is not done then the programmed cells will discharge and the memory will "forget" what has been written to it. For a typical DDR3 device a Refresh command should be issued every 8us or less. This means that a test which runs successfully on a conventional in-circuit test system, with full access to the device under test, could fail when run through a Boundary Scan test system. This failure is caused by the very low effective data rate that is typically provided by a Boundary Scan test. For example if the Boundary Scan chain used to test the DDR memory consists of 1000 Boundary Scan cells then at a Boundary Scan TCLK rate of 50MHz the maximum clock rate that can be generated on any given Boundary Scan cell output is :

$$(50Mhz/2)/1000 = 25kHz$$

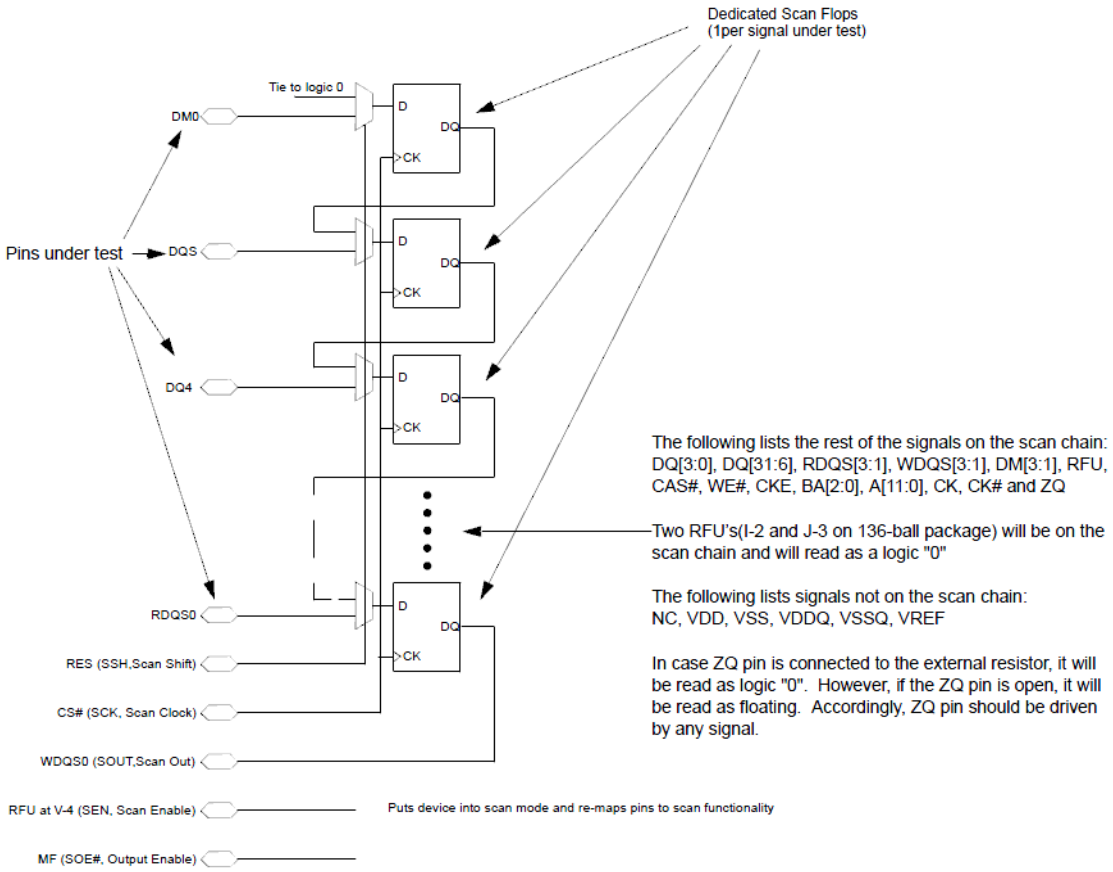
This very low effective data rate means that many more Refresh commands are needed compared to a conventional in-circuit test, this means that for any given device the test must be tailored for the specific test methodology.

The corollary to this low effective data rate is a similar increase in the number of test vectors needed to test the device. For example the development of a DDR3 memory test writing to and reading from 15 address locations, resulted in a Boundary Scan test containing in excess of 1.5million test vectors. This can result in long test execution times and also long compile times for the device test, resulting in reduced productivity when trying to complete test development. Given a TCK speed of 25MHz this would result in an overall test time for just one DDR memory of 120ms.

Devices With DFT Features

Now let us consider the testing of a GDDR3 memory with the "Scan Test" mode defined by JEDEC. These devices have one additional pin, SEN or Scan Enable. When asserted the memory is placed in a test mode where it becomes a parallel in, serial out shift register. Three of the memories pins become control pins for the shift register function, a 4th pin becomes the shift register output, all the remaining digital I/O pins on the memory become inputs to the shift register.

Figure 1. Internal Block Diagram (Reference Only)



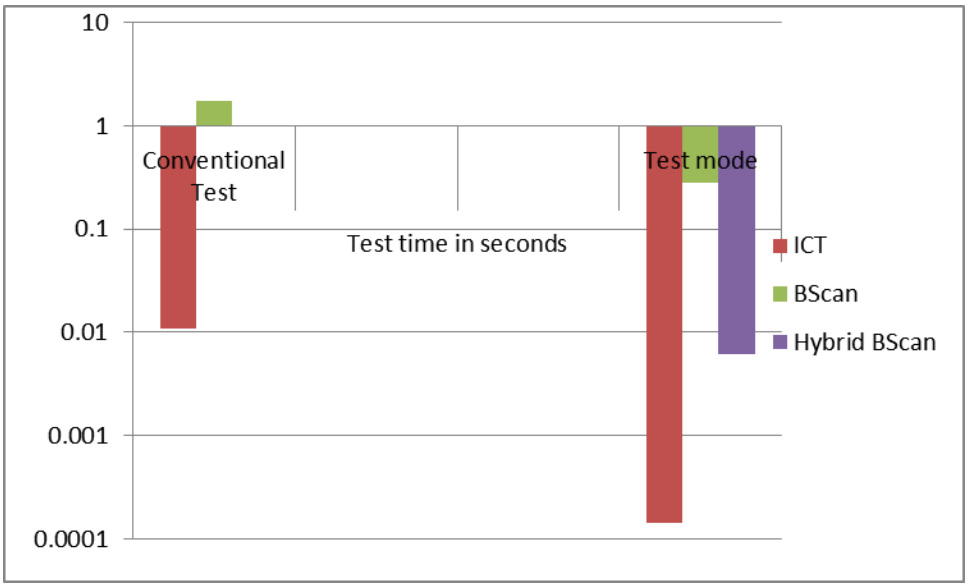
Testing at ICT

This DFT functionality allows us to create a simple test for this device. In this case , Samsung 512M GDDR3, there are 67 device pins which become parallel inputs to the shift register once the test mode is invoked by asserting the SEN pin (V-4). Initialization can be accomplished in just 4 test vectors and a test to check for open circuits requires just 282 test vectors. This is considerably simpler than a conventional DDR test which would require more than 4000 test vectors just to initialize the device. This small number of test vectors plus the clearly defined mode of operation makes testing of these devices very straight forward and greatly simplifies the effort needed to get a test up and running. In addition this test mode is supported by multiple memory vendors with no variation of test mode implementation; this allows the test engineer to create a single test to support any memory vendor whose chips might be used on the board under test.

Testing with Boundary Scan

If these devices have limited or no access then they can be tested via a Boundary Scan device chain. Again, because of the small number of test vectors needed then a Boundary Scan test will remain quite small and manageable. For a 1000 cell chain then around 500k vectors will be needed to test the device. This means that test compile times will remain short, whereas with a conventional test running via a Boundary Scan chain, test compile times can become excessive. A conventional test containing 20000 test vectors would require in excess of 40million Boundary Scan test vectors if run through a 1000 cell chain, giving rise to long compile times and long test times. At a TCK speed of 25MHz this test would take 1.5 seconds to execute, compared to a test execution time of around 250msecs for a device with this test mode, if running at an ICT vector execution rate of 2MHz. If the target test system supports a hybrid use model, where both Bed of Nails probes and boundary scan resources can be used, then test times can be further reduced. In one example, again using a 1000 cell boundary can chain, but with probes on the Scan Clock and Scan Output pins of the device, test times were reduced to just 6msecs as only 12k vectors were being executed.

Comparison of Conventional vs Test mode test times. (Logarithmic scale)



Noise should not be an issue as we will be relying on the Boundary Scan device to provide the test stimulus and response rather than using the ICT test hardware via a bed of nails.

One other significant benefit of testing these devices with their test mode is that diagnostic messages can be added to the test to indict a suspected open input pin in addition to the failing output. As each cell of the shift register is shifted then the corresponding input pin can be indicted if a failure occurs. This isn't possible with a conventional test as all the IO pins are tested simultaneously; this problem with a conventional test is compounded when the test is executed via a Boundary Scan chain.

In addition to this existing test mode the IEEE 1581 standard was recently approved. This a new set of DFT features which can be added to DDR memories to simplify test development and debug. With IEEE 1581 no additional pins need be reserved to place the memory into a test mode as the standard includes a Transparent Test Mode function where the test mode is entered as a result of the test engineer performing a "non-standard" operation on the device. The test modes supported by the IEEE 1581 standard are all versions of XOR tree test modes and thus offer very similar benefits to the existing JEDEC test mode described earlier, but because the test logic is now entirely combinatorial rather than sequential test times will be reduced even further. Again the use of an XOR tree allows for the added benefit of pin level diagnostics.

Conclusion.

Testing of DDR memories that support DFT features such as those outlined above is far simpler and more efficient than testing memories in the conventional way. The number of test vectors needed is vastly reduced, resulting in tests that can be executed quickly and reliably compared to conventional tests. Diagnostics are improved and tests can be deployed in production with a minimum of support. In addition the variability between memory vendors is eliminated allowing a single test to be developed regardless of the memory vendor being used.

As memories become ever faster and more complex the challenges facing the test community become ever greater. Hopefully this paper has helped to demonstrate how the use of DFT features in DDR memory designs can greatly simplify the challenges facing test engineers today.

Testing DDR Memory

How On-chip DFT helps

Testing DDR Memory

What’s the problem?

Testing DDR Memory

What's the problem?

Testing DDR's at ICT is hard.

Testing DDR Memory

What's the problem?

Testing DDR's at ICT is hard.

It's very, very hard.

Testing DDR Memory

What's the problem?

Testing DDR's at ICT is hard.

It's very, very hard.

It verges on the impossible.

Testing DDR Memory

Complex Initialization

Minimum data rates

Test fixture noise

Memory vendor variance

Testing DDR Memory

hynix DDR3L Device Operation

1. Functional Description

1.1 Simplified State Diagram

This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

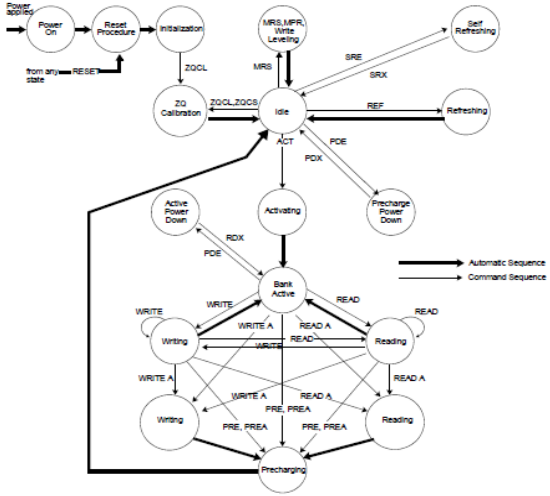


Figure 1. Simplified State Diagram

Table 1. State Diagram Command Definitions

Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Active	Read	RD, RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	Precharge All	Write	WR, WRS4, WRS8	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA, WRAS4, WRAS8	SRX	Self-Refresh exit
RDF	Refresh	RESET	Start RESET Procedure	MPR	Multi-Purpose Register
ZQCL	ZQ Calibration Long	ZQCS	ZQ Calibration Short	-	-

Note: See "Command Truth Table" on page 20 for more details.

Testing DDR Memory

K4J52324QE **512M GDDR3 SDRAM**

9.6 AC CHARACTERISTICS (I-I)

Parameter		Sym-bol	-BJ1A		-BJ11		Unit	Note
			Min	Max	Min	Max		
DQS out access time from CK		t_{DQSCK}	-0.20	+0.20	-0.22	+0.22	ns	
CK high-level width		t_{CH}	0.45	0.55	0.45	0.55	tCK	
CK low-level width		t_{CL}	0.45	0.55	0.45	0.55	tCK	
CK cycle time	CL=12	t_{CK}	1.0	3.3	-	3.3	ns	
	CL=11		1.1/1.25		1.1			
	CL=10		1.4		1.4			
WRITE Latency		t_{WL}	1,2,3,7	-	1,2,3,7	-	tCK	1
DQ and DM input hold time relative to DQS		t_{DH}	0.13	-	0.15	-	ns	
DQ and DM input setup time relative to DQS		t_{DS}	0.13	-	0.15	-	ns	
Active termination setup time		t_{ATS}	10	-	10	-	ns	
Active termination hold time		t_{ATH}	10	-	10	-	ns	
DQS input high pulse width		t_{DQSH}	0.48	0.52	0.48	0.52	tCK	
DQS input low pulse widthl		t_{DQSL}	0.48	0.52	0.48	0.52	tCK	

CK cycle time, max = 3.3ns

CK Minimum Frequency = 300MHz

Testing DDR Memory

Device has been setup
BUT no testing has been done.

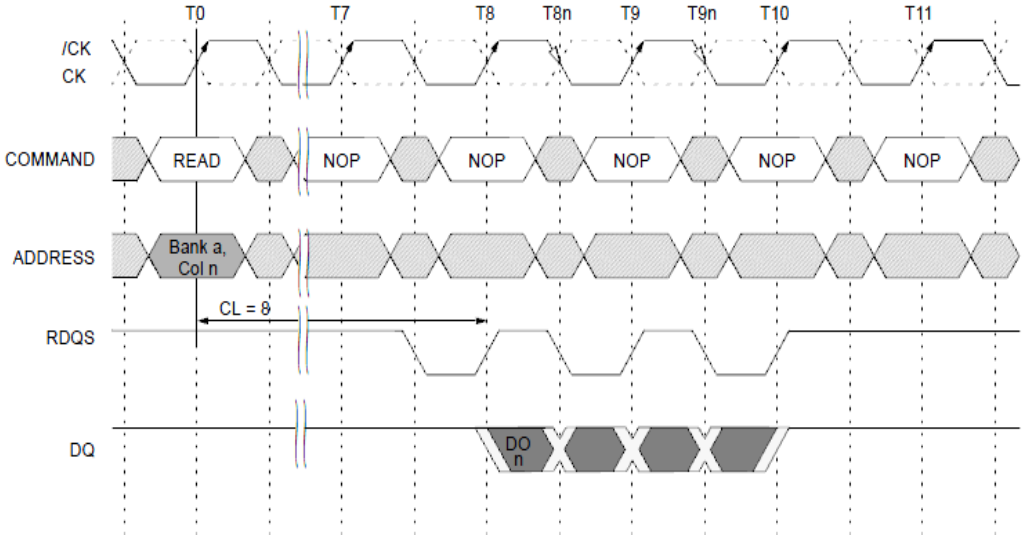
Successfully execute a READ Cycle

Or successfully execute a WRITE
Followed by a READ

Testing DDR Memory

K4J52324QE **512M GDDR3 SDRAM**

READ Burst



Testing DDR Memory

For a device with 100% ICT test access.

20000 test vectors would not be unusual.

For a Boundary Scan test, multiply
by the number of cells in the Scan Chain

For tests of this length test, fixture noise
becomes an issue.

Testing DDR Memory

How does DFT help?

Testing DDR Memory

512MBit GDDR3 with Scan

Jedec 21-C

Testing DDR Memory

Simple Initialization

Small number of test vectors

No vendor variance

Improved diagnostics

Testing DDR Memory

67 Bit Parallel In Serial Out Shift register.

Just 282 test vectors are needed

Diagnose a failure on a single input pin.

Testing DDR Memory

Test time without DFT using a 1000 cell Scan Chain & running TCK at 25MHz

1.5 seconds per device

Testing DDR Memory

Test time with DFT using
a 1000 cell Scan Chain
& running TCK at 2MHz

250msecs per device

Testing DDR Memory

Test time with DFT using
a 1000 cell Scan Chain
& running TCK at 2MHz

If Scan Clock and
Scan Out can be accessed
directly

6msecs per device

Testing DDR Memory

How On-Chip DFT helps