Evolved Testing Methods to Achieve DDR4 Compliance
Overview

With an ever-growing demand to go faster and use less power within a reduced footprint, double data rate (DDR) memory technology has evolved significantly in the past five years.

DDR4 is the fourth-generation of double data rate SDRAM memory. DDR4 enables significantly higher bandwidth for data transfer than DDR3 and offers evolutionary improvements in speed, density and power over previous generation memory. These advances subsequently promote higher performance and energy efficiency for enterprise, micro-server, and tablet applications—allowing designers to build devices with smaller chip footprints, that consume less power, and generate less heat.

<table>
<thead>
<tr>
<th>DDR4</th>
<th>DDR3</th>
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</thead>
<tbody>
<tr>
<td>Data rate</td>
<td>3.2 GT/s</td>
</tr>
<tr>
<td>Power efficiency</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Density</td>
<td>16 Gb</td>
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DDR4 memory architecture combines key features of DDR3 (bidirectional DQS) and a data bus similar to GDDR5 (CRC and data error detection capability). But DDR4 signals do exhibit a few significant behavioral differences from previous-generation DDR solutions. These key differences are driving the creation of a new testing methodology.

Problem

Signal integrity is crucial for reliable operation of memory systems. Testing signal integrity starts with the physical layer, where the data is transferred on both the rising and falling clock edges. Testing the physical layer of DDR4 memory presents some new challenges.

The Joint Electronic Devices Engineering Council (JEDEC) standards require both input and output measurements for electrical, timing, and eye diagram tests, which makes for an extensive list of testing operations to ensure the memory system functions correctly and stays error free. DDR4’s increased speeds also require AC timing parameters to be measured by separating read and write cycles.

Another consequence of increasing memory speeds is an upsurge of random jitter. DDR4 is the first DRAM fast enough to necessitate a requirement for control of jitter within the specification. More jitter will cause the data valid window to decrease, therefore DDR4’s data valid window must be clearly defined.

Another concern for DDR4-based developers is interoperability. The ultimate goal is to ensure the memory system’s universal functionality, while improving efficiency and productivity. A clear understanding of the DDR4 specification test requirements (e.g., memory timing, eye measurement, and jitter) and testing processes (e.g., correct probing and simulation protocols) enables you to recover margin—which in turn can expedite chip/system design cycles, lower costs, and accelerate speed-to-market. The ultimate goal is ensure the memory system’s universal functionality while improving efficiency and productivity.

What is Jitter?

Jitter is the deviation of a timing event of a signal from its ideal position.
Test Requirements

Memory timing specifications for previous generations of DDR had been based on risky assumptions—the biggest of these being that data capture was assumed to be perfect as long as the data setup and hold time met the specification. With slower data rate and larger margin, DDR2 and DDR3 specifications assumed that random jitter was negligible and that the bit error rate (BER) was zero. Of course, it wasn’t actually zero. On a clock jitter, measurements of 10,000 cycles error rate would be 1e-4, so it was close enough to be considered zero. Lower data transfer speeds in DDR2 and DDR3 have been able to work with these assumptions, as there is still enough margin before the system would see a failure.

With DDR4’s faster data rates, the margins decrease and random jitter can quickly close a data eye, which means error rates increase. Left unchecked, this would cause significant system reliability issues and increased design times—slowing your time-to-market and increasing the cost of your design cycle. DDR4 test requirements, however, address these issues head-on to assure reliability and lower cost.

Displaying captured waveform data as a real time eye (RTE) offers an insightful view of jitter within serial data signals. The eye diagram is basically an overlay of digitized bits that shows when bits are valid (high or low). This provides a composite picture of the quality of a system’s physical layer characteristics and offers you a concrete visual of peak-to-peak edge jitter and noise.

A real-time eye diagram test provides eye height and eye width measurements to check signal integrity and estimate the data valid window. Simply measuring the data eye, however, does not offer full insight into the data valid window or expectations of bit failure rate. Measuring the worst-case margin of timing (tDIVW) and voltage (vDIVW) is the current approach for signal integrity applied to DDR4 specifications.

Eye-diagram mask testing is one of the most important physical layer measurements that you can use to test overall signal integrity. The margin is calculated for the minimum time and minimum voltage in relation to an eye-diagram mask, which is derived from the total jitter. A direct measurement can be done if the defined BER is large (or if there is a small population of data). When a low BER is to be tested, it would be too time consuming to measure trillions of unit intervals (UI).

Eye-diagram mask testing ensures that the data eye diagram does not violate the bounds of the mask, where jitter (and errors) can occur. In addition to that, the smallest margin (four timing points at the four corners of the mask) is reported as tDIVV measurement result (Figure 1).

**Eye diagram test**

- Allows measurement of data eye height and eye width
- User can also define own eye-diagram mask as per device specification
- Compliance app reports Fail status if eye diagram violates mask

![Image](image.png)

Figure 1. Eye diagram mask testing ensures that signals are not violating the bounds of the mask, where jitter and errors can occur.
Test Requirements continued

The DDR4 specification takes into account the critical role that jitter and BER play. It is important to make jitter BER measurements to form a statistical measurement of total jitter (deterministic jitter + random jitter) to understand the design’s data valid window result and to properly understand the rate at which one can expect an error within the design.

Beyond the specification tests correct application of testing processes and methodologies is also critical. For example, correct placement of the oscilloscope probes is crucial for passing compliance, as well as to accurately characterize and test the margins of designs. For the JEDEC specification, the optimal probing is located at the ball of the DRAM package (not on the transmission line or channel, and not on the memory controller).

Simulation is another important step in the testing process, though it is often neglected. As bus speeds increase and the need to gain as much margin as possible rises, the simulation process helps significantly in terms of reducing design cycles and cost.

For example, simulation helps ensure that the system can tolerate the loading of an interposer. This step evaluates the bandwidth/frequency response of the measurement and ensures that the interposer doesn’t break the bus.

Finally, Keysight works closely with the JEDEC organization to maintain the highest levels of consistency between Keysight’s test and measurement solutions and the JEDEC standards’ test and measurement specifications.

Technology insight: Calculating total jitter

Deterministic jitter (DJ) is generally bounded and predictable and can be correlated to the data stream, such as inter symbol interference and duty cycle distortion. Random jitter (RJ) is defined as Gaussian and is unbounded. As with any Gaussian distribution, as a population increases, so does the peak-to-peak value of the distribution. Therefore, total jitter (TJ) is DJ plus a BER multiplier of RJ. Understanding the components and sources of jitter can enable designers to reduce its incidence in their designs and ensure better data performance.

Compliance test application test inputs

| Simulation | Software in the design phase |
| Real world | Oscilloscope connected to prototype |

Figure 2. The simulated design with appropriate loading can then be compared to the actual scans of the prototype to ensure the system is working as expected.
For DDR4-based computer system designs, there are several ways to gain access to the memory system for testing via probing. This first probing option is for users working on a computer system where a memory slot/connector is available to plug in a DIMM or a SODIMM. For this type of configuration, the easiest way to access the signals is to use a slot interposer (Figure 3).

The slot interposer routes out all command signals to a cable that connects directly to the input of a mixed-signal oscilloscope (MSO), in place of an MSO cable. To access the data strobe signal (DQS) and output data (DQ), a probe head can be soldered to the slot interposer and connected to the analog channels (Figure 4). Doing so enables a view of 16 digital channels from the SODIMM as well as the DQS and DQ signals through the analog channels.

DDR4 BGA probing is a different option for testing embedded systems (or for DIMM configuration). For DDR4 specifically, the BGA interposer is designed to provide access to all signals to allow maximum flexibility in terms of characterizing all signals -- data, address, control, command, strobe and clock. In this approach, the BGA interposer is soldered between the DRAM and the board. Soldering points for connection to the oscilloscope are available at the top of the BGA (Figure 5).

For tight spaces (especially in a DIMM configuration), a riser may be required to elevate the interposer from the board so that it does not interfere with any adjacent components (Figure 6). In this case, the riser would be soldered at the bottom of the interposer.

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Custom interposer

If you need an interposer for which we do not have an existing design, our design team can work with you to create a custom solution. Please work with your local Keysight representative to initiate the process or visit www.keysight.com/find/contactus.

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Three steps for accurate testing:

1. Choose the right probe and place it correctly
2. Pick the oscilloscope with the right analysis for your application
3. Use automated compliance test application for JEDEC standards

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Figure 3. SODIMM slot interposer.

Figure 4. Use solder-in probe heads to access DQS and DQ signals routed to the analog channels of your oscilloscope. In this example, the probe head used is the E2677A.

Figure 5. Keysight DDR BGA Interposers. The signals are accessed through the oscilloscope pad points at the stop around the interposer.

Figure 6. DDR BGA interposer fitted with a riser to elevate the interposer for smaller surface areas.
Selection of testing equipment is the next key consideration after probing protocol. Although BER specification in memory technology is new, this sort of testing is well established in high-speed design and is well-supported by measurement tools, like oscilloscopes. It is exceptionally important to use an oscilloscope with advanced measurement analysis capabilities including de-embedding and real-time eye diagram measurement, as well as the ability to mix analog and digital signals and cross reference to your simulated design.

An MSO is an oscilloscope that combines digital and analog signals in one instrument. An advantage that an MSO offers is the ability to separate read and write data. Users can connect the command bus, Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE), Chip Select (CS), and clock signal to the digital channel and have the oscilloscope trigger on the read or write command of any or a combination of these signals. The corresponding data will be separated and electrical and timing tests can be performed. MSOs also let testers view the flow of the command protocols, which helps with detection of protocol violations.

When selecting an oscilloscope, it is critical to understand how it integrates with the rest of your design and test tools. Keysight leverages a unique position as being the world’s leading electronic measurement company that builds both EDA (software simulation) tools and oscilloscopes. When it comes to running traditional electrical and timing specifications at the end of the DDR4 design phase, Keysight’s toolset offers the unique benefit of utilizing the exact same compliance tests on both the simulated waveforms in the release candidate and the measured waveforms of the physical prototype. In other words, the simulated waveforms can be imported into the oscilloscope, and waveforms from the physical prototype can be compared to the original simulation.

The simulation process helps to significantly reduce the number of design cycles and cost. Every time you probe, additional load is placed on the system. Simulating that load can ensure that the interposer doesn’t break the bus or cause any unknown loading. Keysight’s W2351 DDR4 compliance test bench can be used to simulate this loading, generate de-embedding files to remove the probing effects, and measure it with your oscilloscope (read more about de-embedding in step 3 on the next page), giving you a true comparison of your simulated design to your prototype.

Questions to ask your oscilloscope vendor:
- Can I cross-trigger and measure digital and analog channels?
- Does the scope have de-embedding capability?
- Does it have real-time eye diagram measurement capability?
- Can I cross-reference it to my simulated design?
Software is the final piece of the testing solution. A DDR4 compliance test application (such as Keysight’s N6462A DDR4 electrical compliance test software) allows the same oscilloscope you use for everyday debugging to perform automated memory testing and margin analysis based on JEDEC specifications. The application will automatically configure the oscilloscope for each test and provide informative results. It should also include margin analysis, indicating how close your device comes to passing or failing the test for each specification.

Your compliance application should also feature some sort of “Custom” mode to cover crucial measurements such as eye-diagram analysis, mask testing, and ringing, which are critical for characterizing DDR4 devices.

Keysight’s DDR4 compliance test application covers clock, electrical and timing parameters of the JEDEC SDRAM specifications. The application helps you test all DDR4 and LPDDR4 (low power) devices for compliance, while using a Keysight Infiniium oscilloscope.

Keysight’s application also provides a detailed report, which includes the worst-case value with a screenshot, as well as the pass/fail status of your measurement according to the specification. It will also compute the margin before the specification is failed. If users want to collect more data for statistical analysis, they can increase the number of runs. A statistical report will show the minimum, maximum, and standard deviation of the tests. This data is especially useful when comparing results between DRAM vendors or different customers.

Keysight DDR4 electrical compliance test software report includes:

1. Worst-case value with screenshot
2. Pass/fail status with margin
3. Multiple trial run results
4. Statistical report of minimum, maximum, and standard deviation

Technology insight: InfiniSiM

Keysight’s InfiniSiM waveform transformation toolset provides the most flexible and accurate means to render waveforms anywhere in a digital serial data link. The highly configurable system modeling enables you to remove the deleterious effects of unwanted channel elements, simulate waveforms with channel models inserted, view waveforms in physically improbable locations, compensate for loading of probes and other circuit elements, and do so simply and quickly. The ultimate goal is to gain more margin when testing against a specification or when doing characterization work.

Keysight DDR4 electrical compliance test software advantages:

- Keysight is active in the JEDEC organization- key contributor to DDR4/LPDDR4 BER test methodology
- More test coverage than competitors
- One-stop-shop for DDR4 compliance solution (software + BGA interposer)
- Cross-reference to simulated runs via W2351 compliance test bench software
- InfiniSiM waveform transformation toolset
Summary

DDR4 speeds require key AC timing parameters (such as timing and voltage of data input valid window) to be defined and measured in new ways. Probing analysis tools available with oscilloscopes, in combination with automated compliance tests, ensure repeatability and reliability of test results.

Designers who want to reduce the learning curve and accelerate mastery of next-generation testing and measuring protocols should strongly consider working with tool vendors that are active in the JEDEC standard committee. Close collaboration and communication offers designers access to the latest and greatest solutions for compliance testing. This is especially important for newly released technologies where discussion on the specification and measurement methodology can still be in-process.

Keysight’s DDR4 eye contour test methodology is currently being adopted by JEDEC for DDR4 standardization. Keysight is also the only test and measurement company that offers hardware and software solutions across all stages of DDR chip development. From simulation to debug, from validation to compliance.

Anyone doing DDR memory design remains under constant pressure to go faster, use less power, and work within an ever-shrinking footprint. Gaining insight to your designs early in the design cycle offers the opportunity to take corrective action quickly to make sure you meet product quality, interoperability, and time-to-market goals. Success depends on efficiency and reduced design cycles to control costs. Fortunately today, there are many tools out there that can help you achieve this.

Keysight gets involved, you benefit

Keysight’s solutions for digital applications are driven and supported by Keysight experts that are involved in the various international standard committees. We call it the Keysight Digital Test Standards Program. Our experts are active in the Joint Electronic Devices Engineering Council (JEDEC), PCI Special Interest Group (PCI-SIG®), Video Electronics Standards Association (VESA), Serial ATA International Organization (SATA-IO), USB-Implementers Forum (USB-IF), Mobile Industry Processor Interface (MIPI) Alliance, and many others. Our involvement in these standards groups and their related workshops, plugfests, and seminars enables Keysight to bring the right solutions to the market when our customers need them.
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