Keysight Technologies
Advanced Design System Simulation: A New Methodology for Next-Generation DDR4

Application Note
Overview

DDR memory designers are under constant pressure to go faster, use less power, and work within an ever-shrinking footprint. Gaining design insight early in the design cycle offers the opportunity to take corrective action quickly to make sure product quality, interoperability, and time-to-market goals are met. Success depends on efficiency and reduced design cycles to control costs.

DDR4, the most recent generation of Double Data Rate SDRAM memory, enables significantly higher bandwidth for data transfer than DDR3, along with evolutionary improvements in density and power. Designers are embracing the latest DDR4 memory technologies to increase system data rates beyond 2400 Mb/s and push designs to record speeds of up to 3200 MT/s. However, while DDR4’s higher data rates offer distinct performance advances, they also present new challenges in defining appropriate specifications and effective simulation techniques for developers to assure compliance.

An overwhelming concern for DDR4-based developers is interoperability. The ultimate goal is to ensure the memory system’s universal functionality, while improving efficiency and productivity. A clear understanding of the latest DDR4 specification test methodologies throughout the development process can help expedite chip/system design cycles, lower costs, and accelerate speed-to-market.

The first task in the design phase is called design space exploration. Very early in the design process, developers sweep through various parameters and find the optimum location in the design space. The next step, pre-fabrication sign-off compliance, takes place just before the build-out of the PCB or chip, when developers do a full compliance run on the simulated design to maximize the chance of the prototype coming back functional. The final step is post-fabrication compliance of the hardware prototype, as part of a lab test bench where developers use an oscilloscope to actually measure the prototype. This application note addresses the first two steps of the process, as well as how to ensure that post-fab compliance meets the pre-fab sign-off compliance.

The design process for any high speed digital design, including DDR, can be summarized in these three steps.
1. Design space exploration
2. Pre-fabrication sign-off compliance
3. Post-fabrication compliance
Problem

A few critical specifications were introduced with DDR4 one of which is the new BER contour specification. This is in addition to the traditional electrical and timing specifications that date back to first-generation DDR releases. Because it is so new, many designers are wary of the BER contour spec, however Keysight’s close work with industry leaders like Xilinx has shown it to be a golden opportunity and not an added burden.

Performing electrical and timing compliance tests before fabrication involves running a transient simulation on IBIS models or SPICE models of the controller, the memory, and the channel. Designers can collect waveforms of just a few thousand bits to do the electrical and timing specification testing, so in earlier (and slower) generations of DDR it was not too prohibitive in terms of simulation time. They could then measure the set-up and hold time and a few other critical figures from the waveforms. Afterward, they could run the full compliance test to verify the final design and then compare those to the measured oscilloscope waveforms of the prototype after fabrication.

These essential electrical and timing compliance specification tests pose some challenges however, when it comes to the faster speeds and new BER contour specification of DDR4. First, even a short transient (SPICE-like) simulation can take an hour or so to run. With a short waveform, it’s very difficult to account for bit-to-bit variation due to random jitter (RJ). In the simulation world, it would be prohibitively expensive to do a simulation that runs enough of these waveform segments to build up a comprehensive picture of the random jitter and other effects.

Jitter can be divided into various categories and various sources. Categories include deterministic vs. non-deterministic, and bounded vs. unbounded. Sources include reflections at impedance discontinuities, crosstalk, and phase noise in the clock generator. Running a simulation of all of these would take an excessively long time. With previous generations of DDR memory, these jitter effects were small compared to the clock period, so an estimate and a little guard-banding was sufficient. But when moving to the faster data rates in DDR4, the effects become a significant fraction of the clock period and guard-banding leads to a non-optimal design.

The higher the data rate, the more the margin is overestimated using a smaller number of bits. RJ contributes to uncertainty because it is no longer negligible at these small UIs. Uncertainty grows with the data rate because the channel cut-off frequency causes so-called jitter amplification and non-Gaussian RJ, which cannot be accurately modeled with conventional methods.

New design challenges at higher speeds:

- Higher data rate means unit interval (UI) is much smaller
- Smaller timing margins due to erosion by Inter-Symbol Interference (ISI) & random jitter (RJ)—padding no longer effective
- Output stage drain power voltage (VDDQ) reduced for power consumption, which creates more amplitude noise

1. For more information about Keysight’s work with Xilinx, please see our joint paper for DesignCon 2015 Ultrascale DDR4 De-emphasis and CTLE Feature Optimization with Statistical Engine for BER Specification. www.keysight.com/find/UltrascaleDDR4
Test Requirements-
BER contour specification and measurement

Prior to the introduction of DDR4, designers added padding in order to get a very low error rate capable of achieving specification compliance. Because this method no longer works with DDR4, Keysight developed a new methodology for faster bus speeds like DDR4 to allow designers to explore the design space and find the optimum BER contour eye opening with respect to the eye mask given in the DDR4 specification. This new test methodology allows memory developers to skip specification tests during the design space exploration and instead run the full suite once or twice towards the end of the design phase, at sign-off of the release candidate.

This approach is based on the statistical eye method, borrowed from the SerDes (serializer/deserializer) space, which has been around for a number of years. It offers an extremely fast way of measuring BER contour. With this method, an arbitrarily low BER contour – like the 1E-16 contour in the JEDEC DDR4 specification – can be obtained in seconds.

With the statistical eye approach, design simulators can account for many different waveforms and overlay them to form an eye diagram. The inter-symbol interference is accounted for by applying the peak distortion analysis method to the impulse responses, and the other forms of jitter are then added using statistical techniques. This creates a visual representation of how much variance there is bit-to-bit, without ever having to run a bit pattern. In fact, the eye is based on the stochastic properties of a conceptually infinite, non-repeating bit pattern, and yet the simulation runs in a few seconds. In short, statistical eye measurement offers a new methodology where design space exploration is actually BER-centric. It uses these rigorous statistical calculations to measure the BER probabilities down to an arbitrarily low BER.

Figure 1: Keysight’s new methodology involves BER-centric design space exploration. This methodology computes the trace probability distribution using an Rx mask that includes jitter and then directly compares the mask with the BER contour calculated by the statistical eye.

With this approach, developers can see the trace probability distribution ("density plot"), and use an Rx mask, rather than a BER contour, as a new design guideline. This mask accounts for both deterministic and random jitter. Developers can then have a direct visual comparison of the mask with the BER contour that is calculated by the statistical eye. It also automatically accounts for cross-talk between the signal lines.
Keysight’s Advanced Design System (ADS) W2309 DDR bus simulator implements the statistical eye approach for measuring the BER contour spec. It provides a $10^{-16}$ contour much more quickly and accurately than any other simulator on the market today.

The ADS DDR bus simulator enables BER-centric statistical eye measurement

- Computes trace probability distribution
- Uses Rx mask as new design guideline (includes DJ, RJ, and noise)
- Ensures error probability inside a setup-hold mask $< \text{target bit error rate} \ (10^{-16})$
- Avoids excessive guard-banding
- Assures reliability, interoperability

Figure 2. The simulated design with appropriate loading can then be compared to the actual scans of the prototype to ensure the system is working as expected.

Keysight’s ADS DDR bus simulator probes the channel, the transmitter, and the receiver using a very short SPICE simulation, equal to the impulse response of the channel. Then instead of trying to apply a very long sequence of bits to figure out the bathtub curve or the BER contours, it takes the impulse response and applies statistical techniques to the stochastic properties of the bit pattern. It does not use the bit pattern itself, so it won’t have to run a long $10^9$, $10^6$, $10^7$ sequence of bits through the impulse response. Instead, it can actually calculate the bathtub curves and the eye diagram BER contours directly from the impulse response and these stochastic properties of the bit pattern.
Within the ADS DDR bus simulator there are built-in models for DQ and DQS transmitters or drivers. While adding signal processing is cost prohibitive on the DRAM side, signal processing functions are more possible on the controller side. Keysight includes a de-emphasis capability as part of the model. Because the DQ is single-ended, asymmetry between rising and falling edges is accounted for. It also features a physical jitter model in which transitions in the stimulus are shifted by the Tx jitter model.

On the receiver side, the DRAM doesn’t generally have any signal processing, but the controllers sometimes do. Adding a continuous time equalizer on a receiver model is an available option. Additionally, developers may want to work with IC models from a specific vendor (e.g., for a particular controller or DRAM model).

Because it can generate a comprehensive data set in just seconds, Keysight’s DDR bus simulator becomes an ideal tool for design space exploration. Developers no longer have to run long SPICE simulations because they can get BER contours directly in just seconds.

Beyond using the built-in design models in ADS, some developers like to use external design tools. In support of this, Keysight lets developers export results into a spreadsheet for external use.

As a sign-off before committing to the expensive and time-consuming prototype build-and-test cycle, Keysight’s Electronic Design Automation (EDA) software is paired with Keysight’s Infiniium oscilloscopes to offer a unique solution.

Figure 3. These more detailed results show that there are margins around the corners of the mask and the nearest part of the red BER contour. All the byte lanes are plotted in one simulation, as well as the strobe.
Solutions for DDR4 compliance testing continued

Keysight leverages a unique position as both the world’s leading electronic measurement company, as well as the only provider of both EDA tools and oscilloscopes. This means that when it comes to running the traditional electrical and timing specification tests for DDR4 at the end of the design phase, Keysight’s toolset offers the unique benefit of utilizing the exact same compliance test applications on both the simulated waveforms in the release candidate and on the measured waveforms of the physical prototype.

The Keysight Infiniium oscilloscope uses the same compliance application that the W2351 DDR4 compliance test bench uses:
- Run the same Keysight compliance app on both simulation and hardware prototype
- ADS “Waveform Bridge” script writes in a file format that the scope’s compliance app understands
- Design and simulate, then fabricate with confidence

DDR developers design and simulate with ADS using a waveform bridge script to write the file format that the Keysight Infiniium oscilloscope compliance test application can parse. That file is then loaded and read using the offline/remote mode of the oscilloscope compliance software to see how close it will be to the JEDEC requirements for DDR4 compliance.

And after the physical prototype comes back, it can be measured on the oscilloscope’s test bench with the exact same compliance application. Because the compliance application is identical in both cases, any problems that occur must be between the design and prototype phases. There’s no possibility of there being any problems as a result of different applications being used by the EDA and scope vendors.
Summary

In designing and simulating DDR memory prior to DDR4, designers could add a small amount of padding to their simulations and get a very low error rate that achieved specification compliance. But DDR4’s faster data rates require new specifications and testing. Statistical eye measurement creates a fast visual tool in the form of an eye diagram for validating DDR4, including the new BER contour spec. Electrical and timings specs are still essential for sign-off.

Keysight’s solution includes the ADS DDR bus simulator to make a statistical eye measurement and DDR4 compliance test bench software for electrical and timing compliance. These software tools, in combination with a Keysight Infinium oscilloscope and its on-scope and offline compliance application, offer a way to simulate and test your DDR4 design. Because Keysight uses an identical compliance application for design and physical prototype phases, potential production delays and cost overruns resulting from disparities in different EDA and oscilloscope vendors’ applications are eliminated.

Keysight helps memory developers expedite bringing new DDR4-based products to market. From design space exploration, to pre-fabrication sign-off, to post-fabrication compliance testing of a hardware prototype, Keysight solutions offer seamless continuity that helps developers meet the reliability and interoperability expectations of their customers.

Keysight gets involved, you benefit

Keysight’s solutions for digital applications are driven and supported by Keysight experts that are involved in the various international standard committees. We call it the Keysight Digital Test Standards Program. Our experts are active in the Joint Electronic Devices Engineering Council (JEDEC), PCI Special Interest Group (PCI-SIG®), Video Electronics Standards Association (VESA), Serial ATA International Organization (SATA-IO), USB-Implementers Forum (USB-IF), Mobile Industry Processor Interface (MIPI) Alliance, and many others. Our involvement in these standards groups and their related workshops, plugfests, and seminars enables Keysight to bring the right solutions to the market when our customers need them.
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