Introduction

Let’s start with a brief preface into the ‘why’ and ‘what’ of Boundary Scan and later delve into the crux of this paper of Board Design for Testability (DFT) guidelines.

Boundary Scan is also known as IEEE standard 1149.1. This standard was formalized in 1990 by a group called Joint Test Action Group (JTAG). This came into existence due to the increasing complexities in validating the IC design rules and testing on printed circuit board assemblies (PCBAs). Advancements in IC technology and device packaging led to miniaturization of chips. With massive miniaturization, the access to chip for its testing became limited. Convergence led to having multiple chips (with minimal access) on the same PCB. All these aspects posed:

- Lots of challenges in validating the IC design rules
- Extreme difficulty in testing these PCBs

Testing such PCBAs could only be attacked by ad-hoc testing. A group of concerned engineers got together to examine the problems of testing complex PCBAs and their testability, and, standardized an approach to test PCBAs in a well-structured manner that software could easily solve to overcome the above-mentioned challenges. This standardized approach was IEEE standard 1149.1 (boundary scan).

In this document, DFT will be looked at more closely for PCBA designs utilizing boundary scan tools in particular.
**Principle of Boundary Scan**

IEEE 1149.1 described devices to be testable by the implementation of a test access port (TAP), with inputs and outputs of the device supplemented with memory elements residing at the periphery of the chip (near the input/output pad of the chip). Hence these were called ‘boundary scan’ cells and the programming as ‘boundary scan program’.

These cells can be interconnected and data can be shifted into these cells thereby enabling testing of the chip. Multiple boundary scan chips on the board could all be daisy-chained and the entire chain of devices could be tested. With this, we could drive and sense data across the boundary scan devices on the board. This would reduce the burden of extracting test pins for all these chips enabling flexible test strategies.

**Board DFT Guidelines**

Daisy-chaining the boundary scan devices based on some guidelines could enable stable behavior of the devices during testing and, to enhance test coverage of the PCB. ‘DFT’ which stands for ‘Design For Testability’ (as the name implies) enables the test engineer to achieve this objective.

**Generic guidelines**

- Daisy-chaining of boundary scan devices is to connect the TDI of the board boundary scan Test header to the first device and connecting the TDO of the device to the next boundary scan device’s TDI. Connect all the boundary scan devices in this manner with the last boundary scan device’s TDO connected to the TDO of the board boundary scan test header.

- It is a better if all boundary scan devices are connected in one single daisy chain.

- It is advisable to connect the TDI boundary scan Test header to the first device’s TDI through a 22 ohm series resistor. This resistor could make a direct connection between the header and the boundary scan device or an indirect connection through a buffer whereby, the resistor could be connected from the header to the input of the buffer. In a similar fashion, TDO of the last device could be connected directly or indirectly to the header with a 22 ohm series resistor.
While daisy chaining the devices, it is preferred to have an option to bypass boundary scan device with a resistor or jumper stuffing option across the device’s TDI and TDO in a manner to keep the integrity of the chain. This can be enabled during debugging the boundary scan program when encountering issues on a device. It is also suitable to have one bypass option across multiple boundary scan devices of the same type – for example, memories, same ASICs, etc. The below depiction is an example. The same can also be achieved by multiple ways by having logic circuits like mux and switches.

1. Uninstall the series TDO-TDI connections

2. Install the device bypass connections

While choosing the devices in the design phase, it is preferable to opt for a device which is IEEE 1149.1 compliant. The more boundary scan devices there are, the better is the test coverage. Also, higher boundary scan test coverage results in cost effective implementation of the overall test strategy.

TCK, TMS and optional TRST signals are distributed directly or indirectly through buffers with a preferred fan-out of less than 8 per output node.
- TDI, TMS, and TDO signals on the boundary scan header are recommended to be pulled-up with any value between 1K ohms to 4.7K ohms. TCK and TRST signals are recommended to be pulled-down with any value between 1K ohms to 4.7K ohms. This is needed to keep the TAP signals to a known state and to have the board set into default functional state.

- Buffering of input signals should be close to the boundary scan header, to reduce noise and to minimize skew between the TCK and the other signals.

- For designs needing long traces of TAP signals, choose buffers with strong drive strength.

- It is recommended to have a provision of about 2 or 3 pins on the PCB for GPIO control of compliance pins or chip enables to the TAP signal buffers. These pins could be part of a boundary scan header.

1. GPIOs for compliance pin control
2. JTAG_ENABLE control for buffers
3. MUX enable to use same header for JTAG test and FPGA programming
- Chain the devices with similar logic voltage together by interfacing with the others appropriately with voltage translators.

- Group the programmable devices together in one section and keep them at the beginning or at the end of the chain. This would facilitate using a common header for boundary scan and for device programming.

- In complex designs where certain programmable devices or custom ASICs are built purely for power management, it is preferred to not chain this device as it could affect the stability of the board during the test.
- Based on the length of the number of boundary scan devices and the length of the traces, choose the distribution of TMS, TCK and TRST appropriately. Please ensure that the distribution is kept to less than 8 per buffer.

- Treat the routing for TMS and TCK as system clock signals.

- Ensure all compliance pins of boundary scan devices are at the appropriate logic while running the boundary scan test.  
  - For FPGAs, please ensure the Program signals and INIT signals are in non-programming state.  
  - For Xilinx FPGAs, PROG and INIT are to be held HIGH. And, for Altera FPGAs, it would be the CONFIG signal that needs to be held HIGH.

- While testing new devices, clarify the compliance pins and its states from the vendor. For new chips which are in development phase, the specs would still be evolving based on the issues encountered on the silicon. So, it is advisable to cross-check with the vendor on the same and also, on the internal pull-up or pull-down on the compliance pins.

- It is a good design practice to control compliance pins via the GPIO controls during the entry of the PCB into boundary scan mode which could be coupled with a boundary scan header.

**Modular partitioning of long chains**

- When the board has 20 or more devices involving several logic levels, it is preferred to use a scan path linker like Lattice Semiconductors Scan Path Linkers or Texas Instruments SCANSTA112. This would reduce the real estate usage for boundary scan implementation and provides better management on boundary scan chain. When designs involve several logical circuits in a chain; e.g. CPU block, Data Processing block, IO management, Memories, etc. a Scan Path for each circuit would help control all the TAP signals independently. If say, CPU block is desired to be kept out of testing for a debug, the appropriate port on the linker can be disabled thereby ensuring that none of the TAP signals on that logic are toggled.
Memory Test

- To test non-boundary scan memories, ensure that the 'address', 'data', and 'control' signals are controlled through boundary scan devices.

- It is preferred to have boundary scan control on the clocks of memory circuits or on the select pins of clock PLLs.

- Ensure to avoid bus contention issues on memories.

- Ensure that the memory device can disabled on its chip select signal thought boundary scan control.

Multi-board configuration

- Primary boundary scan header would be located on the main board with the TAP signals for other boards spanning through board-to-board (BTB) connectors.

- For system-level boundary scan implementation involving multiple board configurations, please make sure that the boundary scan chain is dynamically configurable by the presence of the board in the system.
- The daughter boards could have individual boundary scan headers which could enable the test of the boards individually. For system-level boundary scan implementation, these TAP signals could be muxed with the signals coming from the main board BTB connector.

- Any compliance signal for the daughter board should have a control from the main board’s boundary scan header.

- Having a multiplexed logic onto the main board and daughter board to detect the presence of each board in the system to appropriately determine the boundary scan chain helps in modular testing of each board of a system.

- For multiple logic chains separated with different headers, these can be tested by connecting different TAPs to each chain.
With high speed differential signals growing on boards, it is important to obtain maximum coverage on these nodes. The below DFT points help achieve this objective while performing DFT at board level.

Check if 1149.6 capabilities are present in devices with differential signals. It is good for board designers to review this aspect during design conception.

Find out the design parameters of $\Delta V_{tx}$ and $T_{Tran}$ to identify the voltage swing generated by the transmitter and $\Delta V_{rx}$ to assess receiver sensitivity to reliably detect transitions parameters. It is important to validate these parameters to ensure interoperability between the transmitter and the receiver devices.

Check if there is a need for external AC coupling capacitor if an on-chip capacitor is not present.

Verify that the AC cells can be operated in EXTEST mode to detect shorted caps.
Verification of BSDL contents for 1149.6 Test

For proper 1149.6 interconnect test coverage, the following details are to be ensured in the BSDL file.

- The "AIO_Pin_Behavior" attribute is provided for devices that contain AC pins. When the AIO_Pin_Behavior attribute is provided for a component, there shall be both an EXTEST_TRAIN and EXTEST_PULSE instruction documented in the <instruction opcode stmt> element of the BSDL for that component.

- For devices with AC differential inputs and/or outputs, a "PORT_GROUPING" attribute is detailed to identify positive (P) and negative (N) legs

```
attribute PORT_GROUPING of ASIC_A : entity is
  "Differential_VOLTAGE ((TX0_S0_SD0_P, TX0_S0_SD0_N), " &
   (TX1_S0_SD1_P, TX1_S0_SD1_N), " &
   (RX0_S0_SD0_P, RX0_S0_SD0_N), " &
   (RX1_S0_SD1_P, RX1_S0_SD1_N));
```

- The BSCAN cell attributes are defined in the “BOUNDARY_REGISTER”. It is important to ensure that input cells are of type BC_4. The output cells typically have a single driver on the P leg. But there are new devices which have a driver for N leg as well (as highlighted in green below).

```
attribute BOUNDARY_REGISTER of ASIC_A : entity is
  "0 ( AC_1, TX0_S0_SD0_P, output2, X ), " & -- AC
  "1 ( AC_1, TX0_S0_SD0_N, output2, X ), " & -- AC
  "2 ( BC_4, RX0_S0_SD0_P, OBSERVE_ONLY, X ), " & -- AC Input
  "3 ( BC_4, RX0_S0_SD0_N, OBSERVE_ONLY, X ), " & -- AC Input
  "4 ( AC_1, TX1_S0_SD1_P, output2, X ), " & -- AC
  "5 ( BC_0, * , INTERNAL, 1 ), " &
  "6 ( BC_4, RX1_S0_SD1_P, OBSERVE_ONLY, X ), " & -- AC Input
  "7 ( BC_4, RX1_S0_SD1_N, OBSERVE_ONLY, X ), " & -- AC Input
```

- The following screen shot of the BSDL defines the attributes of the AIO.

```
-- AIO_Component_Conformance defines the 1149.6 standard used in the device.
attribute AIO_Component_Conformance of ASIC_A : entity is "STD_1149_6_2003";
attribute AIO_EXTTEST_Pulse_Execution of ASIC_A : entity is "Wait_Duration 5.0e-6";
```

- AIO_Component_Conformance defines the 1149.6 standard used in the device.
- AIO_EXTTEST_Pulse_Execution attribute is optional. This indicates the pulse width requirement for EXTEST_PULSE.

- AIO_Pin_Behavior is a mandatory attribute that provides 1149.6 parametric information for the AC pins. The text following "AIO_Pin_Behavior" attributes defines the AC signals.

```
attribute AIO_Pin_Behavior of ASIC_A : entity is
  "RX0_S0_SD0_H[3] : LP_time=5.0e-9 HP_time=15.0e-9; " &
  "RX0_S0_SD0_H[2] : LP_time=5.0e-9 HP_time=15.0e-9; " &
  "RX0_S0_SD0_H[1] : HP_time=6.5e-9 OnChip; " & -- Keyword OnChip has to be mentioned if there is an internal capacitor on the IO
  "RX1_S0_SD1_P[6] : HP_time=6.5e-9 OnChip; " &
  "TXD_S0_SD0_P; " & -- This N leg definition is commented since there is a driver on both P and N legs.
  "TXD_S0_SD0_N; " &
  "TXD_S0_SD1_N; " & -- N leg port is defined since there is a single driver on the P leg
  "TXD_S0_SD1_P; ";
```
The first two lines in the screen shot above document the test receiver associated with single-ended input buffers “RX0_S0_SD0_N[3]” and “RX0_S0_SD0_P[2]”. These test receivers have a low-pass filter inside with a time constant of 5 ns, and this is indicated by the “LP_time” phrase. The “HP_time” phrase indicates the test receiver is designed to work with a high-pass coupling time constant of 15 ns or more. This coupling, if in place, would be provided by board components. One last detail: the “[3]” field directly following the signal name “RX0_S0_SD0_N” indicates that cell 3 is the cell that monitors the test receiver for this input.

Lines 3 and 4 in the figure above refer to “RX1_S0_SD1_N[7]” and “RX1_S0_SD1_P[6]” document both test receivers with no low-pass filter time constant. This buffer is AC-coupled by capacitors integrated into the IC itself, guaranteeing it to be AC-coupled. Again, the time constant of the AC-coupling is documented by the phrase “HP_time”. Additionally, take note the modifier “On_Chip” appears to indicate that the coupling is integrated into the receiver itself.

Lines 5 through 8 in the screen shot above refer to the AC driver cells.

Lines 5 and 6 document the drivers for “TX0_S0_SD0_N” and “TX0_S0_SD0_P”, and show that only the P driver on line 6 is documented and line 5 for N leg is commented. If there are 2 differential drivers for both P and N legs, then only the P leg of the differential pair is documented as N leg would “inherit” the characteristics of the P leg (both pins defined as differential pair and both are drivers).

Lines 7 and 8 document the drivers for both N and P legs. N leg port is defined as there is only a single driver on the P leg. In addition, the N leg has an inverter to the P for generation of differential signatures.

After ensuring the above details in the BSDL file of the board, the test would check for interconnects for .6 to .8 BSCAN cells with capacitor between the two end points.
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