Contents

Introduction .......................................................................................................................... 3
Test Strategy ........................................................................................................................ 5
  Boundary Scan test ........................................................................................................... 5
  Silicon Nail test ................................................................................................................ 5
  Loopback test .................................................................................................................. 5
  Programming .................................................................................................................... 5
  Voltage Monitoring ........................................................................................................ 5
TAP/IO Module Configuration ............................................................................................ 6
SODIMM Test Card .............................................................................................................. 7
PCIE Loopback Card ......................................................................................................... 8
Test Coverage Report ....................................................................................................... 9
Test Coverage on SODIMM Connector ............................................................................. 10
Test Time .......................................................................................................................... 10
Test Sequence Flow ......................................................................................................... 11
Total Solution .................................................................................................................. 12
CPU-PCH Bscan .............................................................................................................. 13
CPU-DIMM Bscan .......................................................................................................... 15
PEX-PEX Bscan .............................................................................................................. 18
PEX-PCIE Loopback Bscan ............................................................................................ 19
PEX-SPI Flash .................................................................................................................. 20
PCH-SPI Flash .................................................................................................................. 20
Conclusion ....................................................................................................................... 21
Introduction

This application note describes a boundary scan solution for Blade Server board using the x1149 Boundary Scan Analyzer. External cards like Keysight DDR4 SODIMM test card and PCIE loopback card are used in this solution to improve test coverage. In this approach, we will show you how x1149 multi-chain feature is used in different configurations to achieve boundary scan interconnection which provides testing for both Open and Shorts coverage between the interconnected device pins.

The objective is to demonstrate a viable boundary scan solution for blade server board in manufacturing environments using the x1149 and Keysight customized DDR4 SODIMM test cards and PCIE loopback cards to achieve full (both open and shorts) coverage for as high as 20% of the board’s total node count.

The x1149 boundary scan analyzer is a good fit here as there are commonly multiple boundary scan chains and devices with different JTAG logic levels on board. The x1149 multi-chain feature links these chains and devices into longer chains by handling the different JTAG logic levels automatically. All interconnections between the boundary scan devices within these longer chains can now be tested, thus increasing the boundary scan test coverage of the board. All these can be accomplished without any wire change to the fixture.

Examples include the chaining of configurations like CPU-PCH and CPU-DIMM. Different configurations are easily achieved through the x1149 multi-chain feature in software, thus offering the user great efficiency and flexibility.

Typically, a Blade Server board will consist of:

- CPU (soldered down)
- PCH
- CPLD
- PEX devices
- DIMM Connector
- SPI Flash

In this board, there are:

- 3 sets of CPU and PCH chipsets
- 2 PEX devices connected up as a chain
- 1 CPLD
- DIMM Connectors connected to CPU
- SPI Flash devices connected to PCH
- SPI Flash devices connected to PEX
- PCIE golden fingers connected to PEX

Figure 1. Blade Server Block diagram
Test Strategy

Boundary scan test
- Perform Interconnect test between the 2 PEX devices.
- Perform Interconnect test between CPU-PCH using the x1149 multi-chain feature.
- Plug in Keysight DDR4 SODIMM test cards into all 6 DIMM connectors and perform Interconnect tests between the CPU and SODIMM test cards.

Silicon nail test
- Perform Silicon Nail tests from PCH to SPI Flash devices.
- Perform Silicon Nail tests from PEX to SPI Flash devices.

Loopback test
- Plug in Keysight PCIE loopback card into PCIE gold finger and perform Interconnect test (loopback, Tx to Rx) within the PEX devices.

Programming
- Perform x1149 programming to program Serial Number, GUID, MAC Address into SPI Flash.

Voltage monitoring
- Perform voltage measurements at critical voltage rails. Providing indirect coverage for all voltage regulator circuitries.

Server block diagram

Figure 2. Blade Server Test Strategy
TAP/IO Module Configuration

There are 4 TAP/IO modules on the x1149. A Keysight customized Mux-Buffer board is added to each of the 4 TAP/IO modules to accommodate up to 8 Bscan chains.

The Mux-Buffer board has a 1:2 multiplexer on board to multiplex the JTAG signals (and the DIO resources).

![Figure 3. TAP/IO Module with Keysight customized Mux-Buffer board](image)

<table>
<thead>
<tr>
<th>TAP#</th>
<th>Mux Buffer #A</th>
<th>Mux Buffer #B</th>
</tr>
</thead>
<tbody>
<tr>
<td>TAP1</td>
<td>CPU1</td>
<td>PCH3</td>
</tr>
<tr>
<td>TAP2</td>
<td>CPU2</td>
<td>PCH1</td>
</tr>
<tr>
<td>TAP3</td>
<td>CPU3</td>
<td>PCH2</td>
</tr>
<tr>
<td>TAP4</td>
<td>PEX</td>
<td>DIMM Test Cards</td>
</tr>
</tbody>
</table>

The TAP/IO modules are set-up as above to allow for Multi-Chain test generation by linking the CPU and related PCH into chains (e.g. CPU1 to PCH1) as well as the CPU and DIMM test cards.

For example:

- To perform multi-chain interconnect test between CPU1-to-PCH1, user will enable TAP1-Mux#A and TAP2-Mux#B.
- To perform multi-chain interconnect test between the CPU1-to-DIMM test cards, user will enable TAP1-Mux#A and TAP4-Mux#B.

Note: The CPLD device is used to distribute power to the board. Many of the signals on the CPLD are “sensitive” because they may trigger a power shut down of the board if activated wrongly. They should not be toggled during test. Therefore, the CPLD is left out of the TAP configuration. Instead, voltage measurement on all critical voltage output rails of the CPLD device provides functional test coverage indirectly.
SODIMM Test Card

The DDR4 SODIMM test card (260 pins) is specially designed to provide maximum coverage on the SODIMM connector. Each of the Address, Data and Control pins on the SODIMM connector are connected to boundary scan bidirectional cells within the test card. When installed on the SODIMM connector, the Address, Data and Control pins on the SODIMM connector are then connected to the Intel CPU chipset on-board which is also a boundary scan compliant device. This allows us to perform an Interconnect test between the CPU chip and the SODIMM test card, achieving full coverage (shorts and open) on all Address, Data and Control pins.

Over 100 VDD and VSS pins (power and ground pins) on the SODIMM connector are also tested for opens or shorts using similar boundary scan methods between the CPU and the test cards. Testing the VDD and VSS pins is critical to ensure good signal qualities during the high speed communication between the CPU and DDR4 memory. All VDD and VSS pins are tested this way except for a few which are used to power up the SODIMM test card. The SODIMM test card taps power from the DUT board itself without need for external power supplies.

Since this method of testing the SODIMM connector using the SODIMM test card provides coverage for the VDD and VSS pins, this method outweighs the Cover-Extend method in terms of test coverage. The test time of running Interconnect test is also shorter than that of a CET test.
The PCIE loopback card is designed to short the Tx pins to the Rx pins on the PCIE bus. This provides a loopback path so that any signal output from the Tx pin can be immediately detected at the Rx pin. No active devices are required to short the pins, so the PCIE loopback card design is simple.

When the PCIE loopback card is connected to the gold fingers of the Blade Server board, this shorts the Tx fingers to the Rx fingers which ultimately shorts the corresponding pins on the PEX devices. Since the PEX device is IEEE 1149.6 boundary scan compliant, we can control the boundary scan cell to transmit and receive signals through the Tx and Rx fingers. Thus, we would be able to detect both shorts or opens on these fingers or traces from the PEX devices to the fingers. Since many IEEE 1149.6 compliant devices include AC-coupled capacitors between the devices, we would be able to ensure that these capacitors are detected and soldered properly.
Test Coverage Report

The total number of nodes for this Blade Server board is approximately 4900 nodes. The boundary scan test using the x1149 is capable of achieving Full coverage (both Open and Shorts) for as high as 20% of the total nodes (998 nodes).

Do note that there is a considerable number of nodes with “Shorts Only” coverage, these are the self-monitoring pins.

Keep in mind that there is also indirect coverage on Voltage Regulator circuitry by measuring their output voltages with the voltage measurement capability (using Digital_In resources) on x1149 TAP/IO module.

(Please note that the DDR4 SODIMM connectors are surface mounted connectors. Due to the high speed nature of the signals, no testpoints are usually assigned to the nodes interconnecting between the CPU and the SODIMM. Without testpoints and without through-hole pins, the DDR4 SODIMM nodes are usually inaccessible.)
Test Coverage on SODIMM Connector

The SODIMM test card is designed to cover all pins on the DDR4 SODIMM connector including power and ground pins. Test coverage of more than 96% (252 out of 260 pins) of the SODIMM connector pins is achieved with the DDR4 SODIMM test card.

<table>
<thead>
<tr>
<th>Tested</th>
<th>Number of Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>P2V5_PVPP</td>
<td>2</td>
</tr>
<tr>
<td>P2V5_DIMM</td>
<td>1</td>
</tr>
<tr>
<td>P1V2_VDDQ</td>
<td>28</td>
</tr>
<tr>
<td>P0V6_PVT</td>
<td>1</td>
</tr>
<tr>
<td>VREFCA</td>
<td>1</td>
</tr>
<tr>
<td>DDR4 I/O Signals (Including Data, Address &amp; Control lines)</td>
<td>125</td>
</tr>
<tr>
<td>GND</td>
<td>94</td>
</tr>
<tr>
<td><strong>Total Tested</strong></td>
<td><strong>252</strong></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Not Tested</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>NC Pins [CS2 – pin 162, CS3 – pin 165, SA0 – pin 256, SA1 – pin 260, SA2 – pin 166]</td>
<td>5</td>
</tr>
<tr>
<td>RESET_N – pin 108 (Not connected to CPU)</td>
<td>1</td>
</tr>
<tr>
<td>SCL – pin 253 (Not connected to CPU)</td>
<td>1</td>
</tr>
<tr>
<td>SDA – pin 254 (Not connected to CPU)</td>
<td>1</td>
</tr>
<tr>
<td><strong>Total Not Tested</strong></td>
<td><strong>8</strong></td>
</tr>
</tbody>
</table>

Test Time

The total test time for x1149 station testing is approximately 214 seconds (3 mins 34 seconds). The test time for each test section is shown below.

<table>
<thead>
<tr>
<th>Test</th>
<th>Time Taken (seconds)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Monitoring</td>
<td>7</td>
</tr>
<tr>
<td>CPU Bscan</td>
<td>2</td>
</tr>
<tr>
<td>CPU-PCH Bscan</td>
<td>2</td>
</tr>
<tr>
<td>CPU-DIMM Bscan</td>
<td>3</td>
</tr>
<tr>
<td>PEX Bscan (including PEX-PEX &amp; PEX-Loopback card)</td>
<td>1.5</td>
</tr>
<tr>
<td>PCH Bscan (including Silicon Nail test to SPI)</td>
<td>2.5</td>
</tr>
<tr>
<td>MAC &amp; GUID Programming to SPI (via PCH)</td>
<td>150</td>
</tr>
</tbody>
</table>

(Please note that the remaining outstanding timing is for the powering up sequence. This blade server board requires a specific powering up sequence which involve pauses as long as 7 seconds. A power cycle to the board is performed after the PEX Bscan tests. Refer to next section for a detailed flow.)

The bulk of the test time is consumed by the MAC & GUID Programming to the 3 SPI Flash devices.
Test Sequence Flow

Power Up
→ Voltage Monitoring
→ CPU Bscan
→ CPU-PCH Bscan
→ CPU-DIMM Bscan
→ PEX Bscan
→ Cycle Power
→ Power Down

All test sections will Go to Finalize if Fail

Total Solution

For this project, there is a 3070 ICT station before the x1149 station. All the unpowered testing including Pins test, Shorts test, Analog Unpowered test are executed on the 3070 ICT station. Then, the board is powered up at the x1149 station for the boundary scan test.

This strategy is employed for maximum test coverage. Probes load the feedback paths of voltage regulators consequently prevent them from oscillating correctly. This will not allow the board to power up correctly unless these probes are removed. Without the need to power up the board at the 3070 ICT, we can retain the probes around the “sensitive” feedback paths of the voltage regulator circuitries to perform the Pins test, Shorts test, and Analog Unpowered tests. This ensures that there is no Shorts defect on board before powering up the board at the x1149 station.

In the x1149 station, the board is powered up. Here, the DDR4 SODIMM test, PCIE loopback tests, and other boundary scan tests including Interconnect between devices, Silicon Nail test to downstream digital devices, Programming to SPI Flash and Voltage Measurements are performed. This covers most of the IC devices on the board.

The rest of the IC devices are mostly voltage regulator devices. The passive components surrounding the voltage regulators are already tested by the 3070 ICT. The functionality of the regulators and related power circuits are tested by measuring the correct output voltages using the x1149's voltage measurement capability (using Digital_In resources). Together, a very comprehensive coverage is achieved for the voltage regulator circuitries.

The x1149 is designed to accept the library files from the 3070 and vice versa and the board files from the 3070. This synergy allows the x1149 development time to be kept to a minimum.

The strategy of using the 3070 ICT and x1149 test stations, enables maximum test coverage with optimal stability in both Unpowered and Powered spaces.
CPU-PCH Bscan

Multi-chain test between the CPU and PCH is generated to test the DMI Interconnect between them.

Figure 8. CPU to PCH interfaces

Figure 9. CPU-PCH Multi-chain
A total of 8 pairs of 1149.1 Differential signals (DMI) is tested in each CPU-to-PCH Multi-chain.

**CPU-DIMM Bscan**

Each CPU chipset is connected to 2x SODIMM connectors. Hence, a total of 6x Keysight SODIMM DDR4 test cards are used for this project.
Figure 11. CPU to SODIMM interfaces
A long chain comprising of 6x SODIMM DDR4 test cards is configured as shown above. A multi-chain test is configured between the CPUs and the SODIMM DDR4 test cards (as seen below) will provide coverage for all the DDR4 interfaces from the CPU to the SODIMM connectors.
To optimize the test time when running the CPU-to-SODIMM test cards Interconnect test, only the relevant SODIMM test cards are turned on (with the rest declared as TAP Only). This shortens the boundary scan chain (boundary scan register length), thus the number of clocks required for each test step is less.

For example:

For CPU1-DIMM-CHAIN, only DIMM1 & DIMM2 which are connected to CPU1 are turned on with the rest (DIMM3 ~ DIMM6) declared as TAP Only.

For CPU2-DIMM-CHAIN, only DIMM3 & DIMM4 will be turned on.
For CPU3-DIMM-CHAIN, only DIMM5 & DIMM6 will be turned on.
PEX-PEX Bscan

A total of 16 pairs of 1149.6 Differential signals on the 2 PEX devices are tested.

Figure 18. IEEE 1149.6 Interconnect nodes from PEX1 to PEX2

Figure 19. IEEE 1149.6 Interconnect nodes from PEX2 to PEX1
A Keysight PCIe loopback card is loaded onto the gold fingers of the DUT to create a loopback from Transmit (Tx) pins to Receive (Rx) pins within the PEX1 device.

A total of 16 pairs of 1149.6 Differential loopback signals within the PEX1 device are tested via the PCIe loopback card. (See “PCIe Gen3 x16” in Figure above)
Figure 22. IEEE 1149.6 loopback interconnect nodes (positive leg) within PEX1

**PEX-SPI Flash**

Silicon Nail test (read IDCode) is performed on the SPI Flash devices connected to the PEX devices.

**PCH-SPI Flash**

Silicon Nail test (read IDCode) is performed on the SPI Flash devices connected to the PCH devices. The Serial Number, GUID, and MAC Address are programmed by the x1149 into the SPI Flash devices too.
Conclusion

Together with Keysight DDR4 SODIMM test card and PCIE Loopback test card, the x1149 station can test the powered portion and cover most of the Boundary Scan, Digital, Connector and Voltage Regulator devices on a Blade Server board.

With the 3070 ICT unpowered test coverage, which includes Pins, Shorts, Analog Unpowered tests, both the 3070 ICT and x1149 complement each other to achieve maximum test coverage with best stability.

The x1149 Multi-Chain feature is software configurable. It allows flexible configuration of boundary scan devices or chains into longer chains. The x1149 manages the different JTAG logic level automatically so that no additional external circuitry or level shifters are required. Plus, full coverage is added for those interconnect nodes between the connected devices or chains.

This strategy of the 3070 ICT and x1149 boundary scan solution is currently deployed in manufacturing production lines and is proven to be viable.

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