Case Study

GaN Power Devices Start to be Designed into Power Sources: Transphorm Details Know-how around Circuit Design and Associated Layouts

Commercial use of GaN (gallium nitride) power transistors has finally started. GaN power transistors can increase the conversion efficiency of power supply circuitry and reduce the external dimensions and weight of equipment, which is extremely beneficial. However, the difficulty in designing such power supply circuits is significantly higher compared to conventional Si (silicon) power MOSFETs. A poor design would cause a high level of electromagnetic interference (EMI),

increase power loss, and in the worst case, break the GaN power transistor itself.

But, there's no need to worry too much. You will be fine if you understand the characteristics of GaN power transistors and design them using an appropriate method and process. We will discuss such methods and processes below.

Normally-off GaN power transistors are realized in addition to high-performance

Let's list up the advantages of GaN power transistors first. The biggest advantages are their low on-resistance, high breakdown voltage, and fast switching speed. In addition, such devices offer three more benefits that are attractive when they are used for power supplies: 1) lower total gate charge (Qg), 2) lower output capacitance (Coss), and 3) extremely low reverse recovery charge (Qrr) (Table 1).

GaN power transistors used to suffer from the "normally-on problem," but the problem has already been solved. Generally, a GaN power transistor employs a high voltage HEMT (high-electron-mobility transistor) structure. Therefore, the devices are "normally-

on," which means a current goes through the devices when the gate-source voltage is zero, unless some creative measures are taken. This causes the current to continue to flow when the power supply circuit fails. Such a situation is very dangerous as power supplies handle large amounts of power. Transphorm Inc. has realized "normally-off" GaN power transistors by cascode-connecting a GaN power transistor and a low-withstand voltage Si power MOSFET to solve the problem. Transphorm currently has six GaN power transistor products with a 650 V withstand voltage (600 V for some products).

	Parameters	Parameter	IPW65R041CED (Infineon)	TPH3205WS (Transphorm)
Static	V_{DS_min}	Drain-to-source voltage	650V@25℃	600V (spike rating 750V)
	R_{DS}(25℃)	Drain-source on-resistance	37/41 mOhm	52/63 mOhm
	Qg	Total gate charge	300 nC	19 nC
	Qgd	Gate-drain charge	165 nC	6 nC
Dynamic	$C_{o(er)}$	Output capacitance, energy related	288 pF [1]	156 pF [2]
	$Co_{(tr)}$	Output capacitance, time related	1485 pF [1]	247 pF [2]
Reverse Operation	Qrr	Reverse recovery charge	1900 nC [3]	136 nC [3]
	trr	Reverse recovery time	250 ns [3]	30 ns [3]

Table 1: Comparison between Si power MOSFET and GaN power transistor

Comparison between conventional Si power MOSFET (SJ-MOSFET) and GaN HEMT from Transphorm

Improvement of the gate charge, output capacitance, and recovery characteristics reduces [1] driving loss, [2] switching loss, and [3] reverse recovery loss, which allows higher-efficiency, smaller power supplies.

[1] V_{GS} = 0V, V_{DS} = 0 — 400V
[2] V_{GS} = 0V, V_{DS} = 0 — 480V
[3] V_{DS} = 480V, I_{DS} = 49.6A, di/dt = 100A/μs
[4] V_{DS} = 400V, I_{DS} = 24A, di/dt = 450A/μs

Parasitic component has a strong influence

The difficulty in power supply design using GaN power transistors is caused by the transistors' extremely fast switching speed. The dv/dt and di/dt are more than 4 and 10 times higher than those of Si power MOSFETs respectively. Transphorm Japan (hereinafter all quotes are from Transphorm Japan) says, "The rise time of a voltage waveform at switching is as short as 7 ns." The shorter the rise time is, the higher the emitted frequency content is. The higher the frequency content, the greater the impact of the parasitic component. In conventional cases where Si power MOSFETs are used, little attention is paid to this issue, and parasitic inductance exceeds 10 nH in many cases.

When using a GaN power transistor, however, "the parasitic inductance must be down to 2 or 3 nH." Otherwise, the gate-source voltage (Vgs) will be modulated by the change in the drain-source current (Ids) flowing through the source inductance, causing a large amount of ringing (Figures 1 and 2). And it may result in high levels of EMI emissions or the breakage of the GaN power transistor.

However, it's not easy to suppress the parasitic inductance down to 2 or 3 nH, because a pattern just 1 mm long and 1 mm wide will generate 1 nH of parasitic inductance.
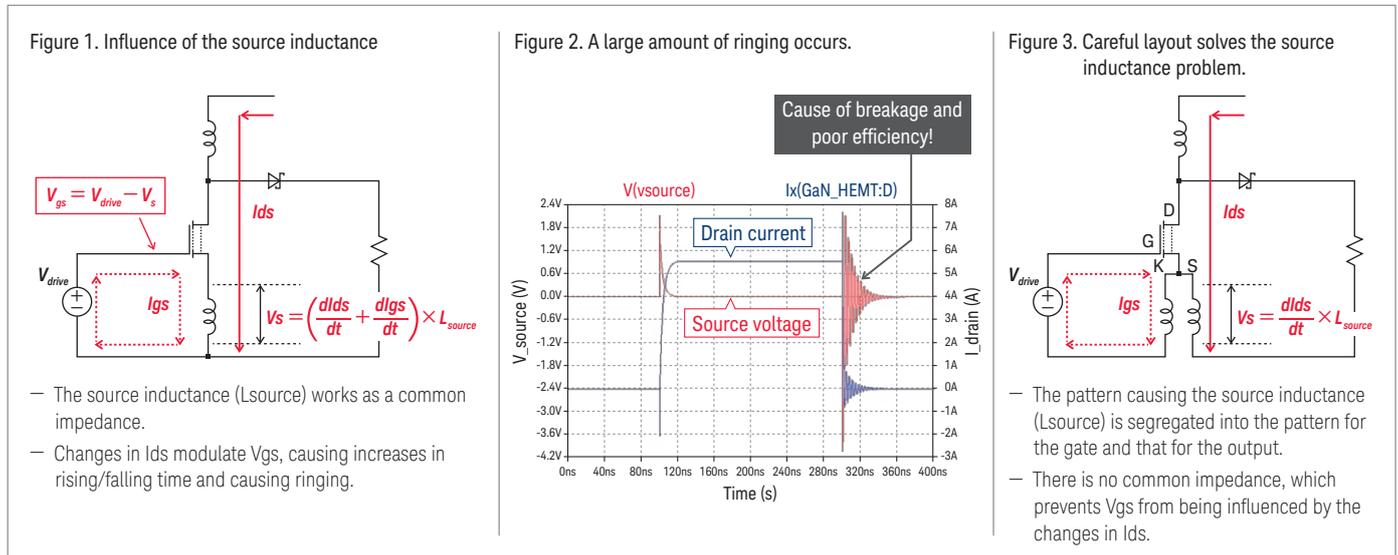
To solve these parasitic inductance problems, Transphorm presents two countermeasures.

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One is to address the source inductance using careful layouts. In general, the source pin of a GaN power transistor and the ground pin are connected with one signal pattern, and both the gate-source current (Igs) and the drain-source current (Ids) flow through this pattern. Therefore, the source inductance works as a common impedance, and consequently the gate-source voltage (Vgs) is modulated in accordance with the change in the drain-source current (Ids).

Transphorm recommends a layout that segregates the gate drive loop for the gate-source current (Igs) and the power loop for the drain-source current (Ids) (Figure 3). Since there is no common impedance for the path on which a large current flows, changes in the drain-source current (Ids) will not influence the gate-source voltage, preventing large amounts of ringing.

The other is to make gate resistance (Rg) unnecessary for the gate signal by selecting a gate driver IC whose output current is appropriate and to insert ferrite beads in series to cut off only the frequency component of the ringing. However, one must be careful when selecting ferrite beads; if the impedance is too high, the signal waveform shape becomes too blunt, increasing the delay.

Figure 1. Influence of the source inductance

$$V_{gs} = V_{drive} - V_s$$

$$V_s = \left(\frac{dIds}{dt} + \frac{dIgs}{dt}\right) \times L_{source}$$

— The source inductance (Lsource) works as a common impedance.
— Changes in Ids modulate Vgs, causing increases in rising/falling time and causing ringing.

Figure 2. A large amount of ringing occurs.

Cause of breakage and poor efficiency!

V(vsource)   Ix(GaN_HEMT:D)

Drain current

Source voltage

Figure 3. Careful layout solves the source inductance problem.

$$V_s = \frac{dIds}{dt} \times L_{source}$$

— The pattern causing the source inductance (Lsource) is segregated into the pattern for the gate and that for the output.
— There is no common impedance, which prevents Vgs from being influenced by the changes in Ids.

Simulation is effective

Properly designing circuit configurations and board layouts can solve the problems that reside in GaN power transistors, and you can enjoy the benefits only if you can confirm that your design actually solves the problems. You have to wait until you build an actual power supply to take measurements for verification/confirmation.

Circuit simulators, however, make considerably more detailed verification possible during the design phase. Transphorm provides a circuit model for GaN power transistors free of charge to support verification work using circuit simulators. It can be used in circuit analysis tools such as LTSpice and PSpice.

Remember that the switching speed of GaN power transistors is high. Verification using a circuit simulator needs to include distributed models that support frequencies as high as 1 GHz besides a circuit model for the devices. There are two ways of doing this. One is a "simple method," which is to combine simple models such as straight lines and L-shaped lines for the simulation of more complex models. The other is a "precision method," which is to conduct electromagnetic analysis of the entire printed circuit board to derive layout models for simulation and execute co-simulation of circuits and layouts.

Even the simple method makes the simulation much better than a simulation that doesn't use pattern models. And the precision method allows extremely reliable verification. Thus, Transphorm and Keysight collaborate on the development of co-simulation methods for circuits/layouts in power suppliesoutcome is the confirmation that the simulation analysis results agree with the actual measurement results fairly well. However, the precision method requires that the operators have deep knowledge and abundant know-how. Therefore, "as a first step, our recommendation is to implement a kind of circuit analysis that takes into consideration the effects of high frequencies by adopting the simple method." Note that general SPICE tools don't support precision methods. You need to adopt a circuit/electromagnetic field simulator, for example, ADS, provided by Keysight (Figure 4).
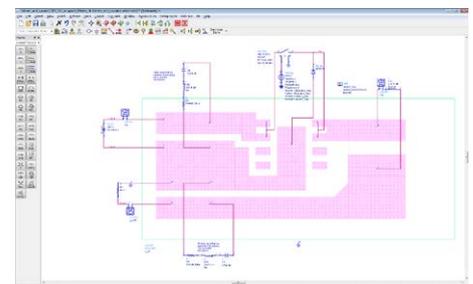
(Table 1 and Figures 1, 2, and 3 courtesy of Transphorm Japan)

Figure 4. An example of circuit/layout co-simulation that allows designs that take into consideration the effects of high frequencies

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