Case study

Panasonic Corporation

GaN Power Devices are Becoming Broadly Available, with Steady Progress in Design Environment in Addition to Secure Reliability

To exceed the limits of the performance of Si (silicon) power devices and contribute to industries — this is the ultimate goal of GaN (gallium nitride) power devices.

The benefits of GaN power devices are clear: fast switching speeds at high frequencies and low power loss. Such benefits enable power supply circuits to be dramatically smaller in size and more efficient in power conversion. Another piece of good news is that their availability has significantly improved over the past year. A few manufacturers have already commercialized GaN power devices so that users can purchase and examine the devices.

The conditions for the GaN power device market to expand seem to have been fulfilled in various respects. Despite the clear advantages mentioned above, there are still some critical issues left unsolved. It is still a challenging job to replace Si power devices with GaN power devices, as their reliability, robustness, and ease of design need to be the same as those of Si power devices. This article introduces the efforts made by Panasonic to solve such issues.

Beyond JEDEC

Panasonic launched two 600 V blocking voltage GaN power transistors: PGA26E19BA with 140 mΩ of on-resistance at 13 A of drain current, and PGA26E07BA with 56 mΩ of on-resistance at 26 A of drain current (Table 1).

A six-inch Si wafer has been adopted as the substrate. AlN and AlGaN layers are layered on the substrate, and over all this, a GaN epitaxial layer is formed. The issue here is the difference between the thermal expansion coefficients of Si and GaN. In the process of forming the epitaxial layer, the entire substrate is heated, and then cooled down instantaneously, which causes stress in the epitaxial layer, introducing cracks. Such cracks make the device useless.

To solve this issue, Panasonic inserts a buffer layer, which is an artificial lattice in which GaN layers and AlN layers are alternately stacked, beneath the GaN epitaxial layer. This reduces the stress, and consequently prevents cracks in the GaN epitaxial layer.

The developed GaN power transistors perfectly pass the reliability tests for power devices defined by JEDEC (Joint Electron Device Engineering Council). But, that does not necessarily prove that their reliability and robustness exceed those of Si power devices. Panasonic argues that the tests defined by JEDEC are not adequate to demonstrate the reliability and robustness of GaN power transistors, and that it is essential to make efforts for Beyond JEDEC, which aims for tests whose limits are stricter than those defined by JEDEC.

Panasonic X-GaN™ Family				
Product	PGA26E34BA	PGA26E19BA	PGA26E07BA	PGA26E07XX
Package	Power SMD(DFN)			Power DSO
	DFN 6x4 【Small footprint】	DFN 8x8 【High Speed】		DSO 20 【High Power】
Blocking Voltage	600V	600V	600V	600V
Drain Current	5A	13A	26A	31A
Rdson(typ)	280mΩ	140mΩ	56mΩ	56mΩ
Qg	1nC	2nC	5nC	5nC
Qr	0nC	0nC	0nC	0nC
Status	Sampling (18/CQ1)	In volume production	In volume production	Planning

Table 1 GaN Power Transistors from Panasonic Two products are on sale now. Two more products are planned to be launched in 2018.

Normally-off GaN devices realized by applying innovative structures

Panasonic's two products have already leveraged the outcomes of Beyond JEDEC. Panasonic has made multiple efforts, two of which are introduced below.

The first one was to realize normally-off GaN power transistors. Simply attaching a gate electrode makes a transistor normally-on. Normally-on is not acceptable for applications in power supplies because current in the device keeps flowing even if the power supply fails, which will likely cause fires or other disasters. Panasonic improved the electrode structure (Figure 2), using a creative way of sandwiching p-type GaN layer between the gate electrode and GaN epitaxial layer. When the device is turned off, the depletion layer expands in the channel and shuts off the drain current, which makes the device normally-off. This structure is called a gate injection transistor (GIT).

The second one was to take measures to prevent current collapse. Current collapse generally increases the dynamic on-resistance of GaN power transistors, accelerating heat generation, which shuts the power supply down.

Today, the mechanism of current collapse is understood as follows. There are still some stresses caused by the difference in the thermal expansion coefficients in the GaN epitaxial layer, causing dislocation. When voltage is applied in such a situation, highly-charged electrons are trapped by the dislocations, preventing the flow of drain current. Thus, the dynamic on-resistance increases.

Two measures were taken to solve the problem. The first one was to optimize the process of forming epitaxial layers and to optimize the artificial lattice buffer layers. This measure alone, however, cannot prevent an increase in on-resistance when the blocking voltage exceeds 600 V. Thus, a second measure was taken, which was to inject holes to recombine the holes with the trapped electrons, and thus eliminate the trapped electrons (Figure 3). In practice, a second drain electrode, whose structure is same as the gate electrode, is set next to the drain electrode, and holes are injected through the second drain electrode. This structure is called a hybrid drain embedded GIT (HD-GIT). By combining these two measures, Panasonic says, "the current collapse problem is completely solved for up to 850 V of blocking voltage."

Consequently, the GaN power transistors commercialized by implementing these measures fulfill even test requirements for reliability and robustness that are not defined by JEDEC. For instance, the transistors demonstrate no increase in on-resistance due to aging, and have achieved over 3,600 hours in the dynamic high temperature operating life (D-HTOL) test, which means that they are ready to replace Si power devices also in terms of reliability and robustness.

Also proceeding with development of design environment

The remaining challenge is to raise the ease of design. GaN power transistors have extremely high performance, and their switching speed is as high as tens of megahertz, which is almost impossible for Si power devices to achieve. Not all engineers, however, can benefit from such high performance. It requires high skills and varied experience in power supply design and PCB (printed circuit board) design. For example, patterns that are too long on a PCB may increase parasitic inductance, which prevents the circuitry from driving the devices at high frequencies.

Design engineers who don't pay attention to such factors in PCB design might achieve nothing more than performance similar to what they would get with Si power devices even if they use high-performance GaN power transistors. Unless such cases are eliminated, it will be difficult to make GaN power transistors much more common. In response to this, Keysight Technologies is making efforts in collaboration with Panasonic to develop a design environment for power supplies using GaN power transistors.

Two kinds of efforts are being made. One is about device models. The set of models is called ASM, and they are SPICE models for GaN power transistors developed by UC Berkeley. And, the other is the 3D electromagnetic field analysis of evaluation boards that Panasonic provides. Keysight's 3D electromagnetic analysis tool named ADS Momentum is used to extract S-parameter models. Figure 4 shows the outcome of such efforts. The plot is an analysis of results obtained through the combination of these two with Keysight's RF/microwave circuit simulator ADS. The simulated results for output capacitance (Coss) closely match the actually measured results. The results demonstrate that the commercialization of the design environment will allow a lot more power supply designers to design their circuits so that GaN power devices can perform adequately.

Figure 2 Realizing normally-off GaN power devices

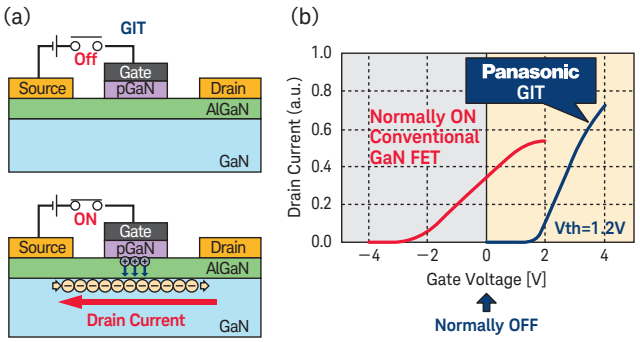


Figure 2 (a) shows the device structure. P-type GaN layer is used for the gate electrode to form a p-n junction. Figure 2 (b) shows the plot of the drain current vs the gate voltage. The GIT structure makes the device such that when its gate turns on, holes are injected into the channel.

Figure 3 Solving current collapse problem

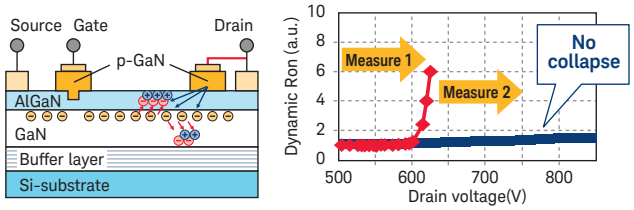
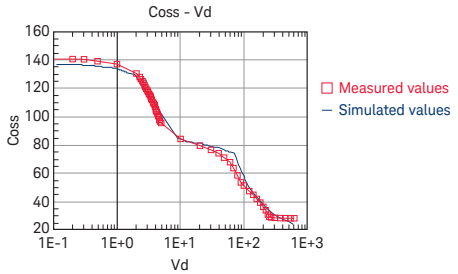


Figure 3 (a) illustrates the theory behind solving the current collapse problem using a HD-GIT structure (Measure 2).
Inject holes through the second drain to eliminate the trapped electrons. Figure 3 (b) shows the changes in dynamic on-resistance. The on-resistance doesn't significantly increase even if the drain voltage reaches 850 V. Note that the devices for which only improvements in manufacturing process and device structure (Measure 1) were made show a rapid increase in on-resistance around 600 V.

Figure 4 Enabling more accurate analysis



The graph shows the results from analysis using models named ASM for GaN power transistors, and S-parameter models for evaluation boards using an RF/microwave circuit simulator named ADS. Note that the measured values and simulated values match very well. Ciss (input capacitance) and Crss (reverse transfer capacitance) also show a similar correlation.

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Published in Japan, February 15, 2018
5992-2752ENN
0000-08cS
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