

PCIe 5.0

The Next Generation of Peripheral Component Interconnect

Defining the Next Standard in Interconnect Technology

PCI Express 5.0 represents the latest in PCI standards using non-return to zero (NRZ) signaling; doubling the PCIe 4.0 speed from 16 GT/s to 32 GT/s. The PCIe 5.0 standard is on a fast track for development as the PCISIG (PCI Special Interest Group) — the standard body which controls the PCI Express standard — has tasked the team to complete the PCIe 5.0 rules by the end of 2019.

Originally, the parallel PCI bus's purpose was to extend the functionality of standard personal computers and allow for the addition of networking cards, graphic cards, and other peripheral interfaces. PCI Express represents a high-speed, differential, serial version of I/O technology that shares significant roots with the old PCI bus. In all cases, the PCI and PCI Express standard's intent is for high-volume manufacturing with low material costs for PC Boards and connectors. The PCI Express standard successfully meets this goal with speeds of 2.5 GT/s, 5 GT/s, and 8 GT/s. But PCI Express 4.0 at 16 GT/s, the latest speed enhancement to the standard, has proved to be more difficult for adoption by the PC industry. Additionally, the motherboard and PC channels typical of most computers will be significantly challenged to transfer the 32 GT/s of PCI Express 5.0.

However, the demand for more speed has driven the standard body to define the next generation of PCI Express. The goal of PCIe 5.0 is to increase the standard's speed in as short a time as possible. As such, PCIe 5.0 is intended as a straightforward speed bump to the PCIe 4.0 standard without any other significant new features.

For example, PCIe 5.0 does not support PAM4 signaling and only includes new capabilities required to enable the PCIe standard to support 32 GT/s in as short a time as feasible.

Next Generation Challenges

The significant challenges to prepare a product to support PCI Express 5.0 relates to channel length. The faster the signaling rate, the higher the carrier frequency of the signal transmitted over the PC board.

Two types of physical impairments limit how far an engineer can expect to propagate their PCIe signals:

1. The attenuation of the channel
2. Reflections that occur within the channel due to impedance discontinuities found in pins, connectors, vias and other structures.

The PCIe 5.0 specification uses a channel with -36 dB attenuation at 16 GHz. The frequency 16 GHz represents the Nyquist frequency of a 32 GT/s digital signal. For example, when a PCIe 5.0 signal starts out, it may have a typical peak-to-peak voltage of 800 mV. However, after passing through the proposed -36 dB channel, any resemblance to an open eye is missing. It is only through the application of transmitter based equalization (de-emphasis) and receiver equalization (a combination of CTLE and DFE) that a PCIe 5.0 signal can pass through the system channel and be interpreted accurately by the receiver.

The minimum expectation for eye height for a PCIe 5.0 signal is 10 mV (post-equalization). Even with a near perfect, low jitter transmitter, the significant attenuation of the channel lowers the signal amplitude to the point where any other type of signal impairment caused by reflections and crosstalk works to close the recoverable eye.

How to Prepare for the Challenges

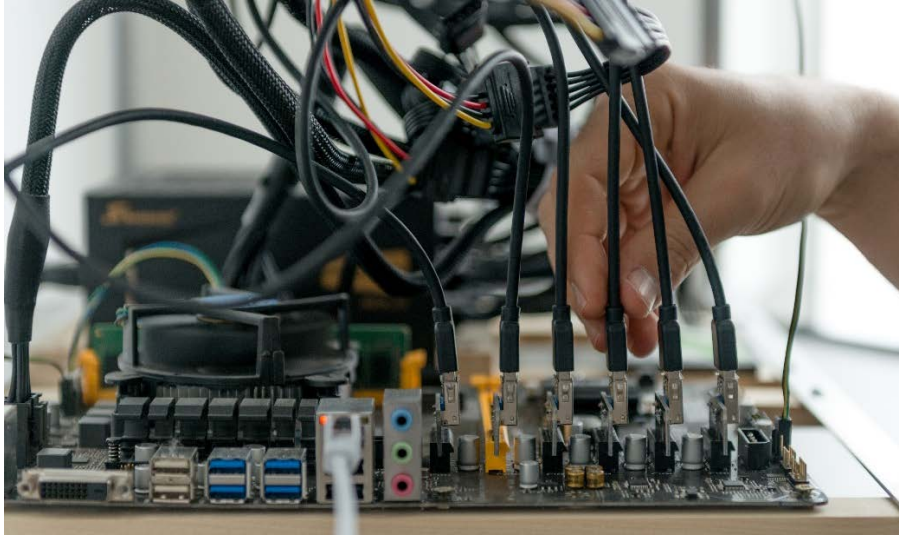
To help ensure success with products that support PCI Express 5.0, Keysight is actively engaged to provide test solutions for validation of the physical layer properties of PCIe 5.0 transmitters and receivers. Tools to help test PCIe 5.0 devices are available now, and used for the development of the PCIe 5.0 standard.

For example, to test a PCIe 5.0 transmitter, you should consider a real-time oscilloscope with a minimum bandwidth of 32 GHz. If validating new silicon, you want to measure the transmitter output of the integrated circuit as close to the output pins of the device as possible. De-embedding the loss attributable to any breakout channel between the balls of the package to the connectors used to attach the test fixture to your oscilloscope is required.

The transmit test parameters at 32 GT/s for PCIe 5.0 are the same parameters tested at the lower speeds of 16 GT/s and 8 GT/s. A high-bandwidth oscilloscope (63 GHz or more) with high-signal integrity is an ideal tool for these tests and PCIe development.

One of the most challenging aspects of PCIe 5.0 receiver testing is the stressed jitter measurement. A Bit Error Rate Tester (BERT) can be used to test your receiver. In this test, a worst case PCIe 5.0 eye is carefully constructed using calibrated impairments and physical ISI traces to achieve a target eye height of 10 mV (post-equalization). With the target DUT in loopback, the goal is to present the stressed eye to the receiver input and then to count errors as the signal loops back to the BERT's error detector.

It is the calibration of the test signal which is the most challenging aspect of receiver testing. The standard itself is not yet complete, so prototype software and test methods specific to PCIe 5.0 are evolving too.



The Keysight Z-Series oscilloscopes and M8040A JBERTs represent the preferred choices for many of today's pioneering technology companies looking to achieve PCIe 5.0 performance while also delivering high-quality, robust, and interoperable design.

Conclusion

Scheduled for completion by the end of 2019, PCI Express 5.0 represents the latest in PCIe standards doubling the data rate from the PCIe 4.0 speed of 16 GT/s to 32 GT/s using non-return to zero (NRZ) signaling. The challenges inherent in PCIe 4.0, include testing and implementation broadly across the PC industry, increases with PCIe 5.0 as the speed doubles. However, test companies like Keysight are already developing the test solutions to provide aid in overcoming these new design and test challenges.

Learn More

You can learn more about the recommended BERTs and oscilloscopes:

[Keysight Z-Series oscilloscopes](#)

[Keysight UXR Series oscilloscopes](#)

[Keysight M8040A Bit Error Rate Tester](#)

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