4 KEY CONSIDERATIONS FOR 5TH GENERATION HIGH-SPEED DIGITAL DESIGNS

Meeting the Data Center Need for Speed
Introduction

Paving the Way for 400GE in the Data Center

Next-generation technologies including Internet of Things (IoT), artificial intelligence (AI), and autonomous cars drive the need for more speed in data centers worldwide. Data center equipment manufacturers need to advance from 100 gigabit Ethernet (GE) to 400GE to meet the needs of these new applications. Faster data center speeds are only effective if the entire system can deliver. Faster networking requires faster memory and faster serial bus communications. Data center operators need to move to 5th generation high-speed computing interfaces, such as Peripheral Component Interconnect Express (PCI Express® or PCIe®) and Double Data Rate (DDR) memory, and consider new specialized interconnect technologies that offer alternatives to PCIe.

Each generational change of high-speed computing standards provides new features and faster data transfer rates, creating new test challenges for digital designers. Faster speeds require high-speed precision testing and validation of compliance to the latest standards.
CHAPTER 1
The Fast Track to PCIe 5.0 – If You Build It, They Will Come
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PCI Express Evolves to PCIe 5.0

PCIe is a high-speed, differential serial standard for point-to-point communications at the rack-level in a data center. Data center operators prefer to assign computing tasks to servers located in the same rack to avoid inundating the data center network with unnecessary traffic. The PCI Special Interest Group (PCI-SIG®) — the standard body that defines the PCIe specifications — plans to complete the PCIe 5.0 standard in 2019. Chipset and module manufacturers are racing to design PCIe 5.0 devices, seeking a first-to-market advantage, even as the standard evolves and settles.

PCle 5.0 Doubles the Throughput of PCIe 4.0

Each new generation of the PCIe standard provides additional features and faster data transfer rates than the previous generation. PCIe 5.0 doubles the throughput of PCIe 4.0. The transfer rate of PCIe 5.0 is 32 gigatransfers per second (GT/s) vs. the 16 GT/s supported by PCIe 4.0. With 64 gigabytes per second (GB/s) of unidirectional transfer bandwidth, PCIe 5.0 provides 128 GB/s of bidirectional data throughput. PCIe interconnect technology provides crucial connectivity for many other rack-based data center technologies, such as storage and graphics processing units (GPUs).

Figure 1: Evolution of the PCIe standard
5 Design and Test Challenges of PCIe 5.0

With server standards, it is crucial for designers to deliver interoperability and backward compatibility. Designers need tools to validate the parametric and protocol aspects of their designs, to ensure performance and standards compliance. Higher data rates increase signal integrity symptoms such as reflections and crosstalk, causing signal degradation and timing issues. A shorter clock cycle means a smaller jitter budget, so reducing jitter in PCIe 5.0 designs is far more complex than in previous generations of the standard. A successful design requires PCIe testing at the physical layer, data link layer, and transaction layer.
5 Design and Test Challenges of PCIe 5.0

PCIe Design and Simulation
High-speed serial data link design grows significantly more complex as data rates increase. Channel topologies become more diverse, and more parameters need to be tuned for active components. PCIe design simulation tools optimize signal and power integrity, and enable the analysis of the electromagnetic (EM) effects of components such as high-speed integrated circuit (IC) packages and printed circuit board (PCB) interconnects. Using design and simulation tools, designers can quickly and effectively evaluate end-to-end performance of all PCIe links before the first prototype, which prevents costly redesign cycles.

2. PCIe Transmitter Test
Specific types of uncorrelated jitter can undermine the reliability and performance of a PCIe transmitter. For PCIe speeds above 8 GT/s, PCIe receivers utilize strong equalization. While the equalizer can compensate for data-dependent jitter, the reference receiver equalization specified by the PCIe standard does not adequately compensate for uncorrelated transmitter jitter. Using test tools that account for uncorrelated jitter ensures the performance of PCIe transmitter designs.

3. PCIe Receiver Test
Extracting digital content from the 32 GT/s PCIe 5.0 signal presents new challenges. At these high data transfer rates, PCIe receivers often receive a heavily degraded signal due to the channel’s high-frequency loss characteristics, resulting in unacceptable bit error ratios (BERs). Designing and validating a robust receiver that can tolerate these distorted signals requires equalization techniques that restore the quality of the transmitted signal. Support for up to 16 lanes makes designing and debugging a PCIe 5.0 receiver even more challenging. A robust PCIe receiver test solution with support for test automation can reduce test time from days to hours.

4. PCIe Interconnect Test
The channel is one of the most critical elements of the PCIe system. Many sources of distortion in the channel can degrade signal quality from a PCIe transmitter to the PCIe receiver, including crosstalk, jitter, and intersymbol interference (ISI). Loss characteristics must be measured across the channel to ensure they are within limits defined by the PCIe specification for a given data rate. Scattering parameters (S-parameters) characterize high-frequency circuits such as the channel in a PCIe system. Design teams must test and validate the parametric aspects of PCIe designs to ensure they are within the performance requirements defined by the PCIe specification.
5. PCIe Protocol Test
Design teams must validate protocols at the physical layer, data link layer, and transaction layer. In addition to the mandatory protocol compliance tests, the PCI-SIG recommends more than a hundred additional tests to characterize PCIe designs accurately. Testing Link Training and Status State Machine (LTSSM) is particularly important. Link training ensures that data packets transfer reliably between link partners. Protocol analysis and exerciser tools determine whether a PCIe device can successfully communicate with its link partner. Engineers can use PCIe protocol test tools to quickly test a device for PCIe protocol compliance and to debug any detected errors.

PCIe 5.0 Test Solutions
Deploying the right test solutions at each stage of development will give you early insight and help you deliver PCIe devices that meet design quality expectations, achieve compliance to the PCIe standard, and interoperate with devices from other vendors. Validating PCIe performance involves characterizing the reference clock and data signals.

For Card Electromechanical (CEM) specifications, the PCI-SIG provides the Compliance Base Board (CBB), the Compliance Load Board (CLB), and SigTest software to facilitate electrical compliance testing. PCIe devices must successfully pass “Gold Suite” testing, a superset of what the PCI-SIG SigTest software tests, at a PCI-SIG workshop using the official PCI-SIG approved test fixtures. Designers using test tools that provide complete PCIe standard support can be confident that their PCIe devices will pass all compliance tests before attending a workshop.
CHAPTER 2

Faster Networking Speeds Require Faster Memory
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Full Speed Ahead to DDR5

IoT has proliferated billions of internet-connected devices. Data center operators must find ways to meet ever-increasing data transfer and storage demands, while preserving quality of service and minimizing cost. Each new generation of the DDR synchronous dynamic random access memory (SDRAM) standard increases speed, reduces footprint, and improves power efficiency. DDR5, defined by the Joint Electronic Devices Engineering Council (JEDEC) organization, will offer improved performance with greater power efficiency compared to previous generation DRAM technologies.

To support longer battery life in mobile devices, JEDEC also introduced a low-power DDR (LPDDR) standard. The LPDDR standard uses lower signal amplitude to reduce power consumption.

DDR5 Doubles the Data Rate of DDR4

DDR5 will provide double the bandwidth and memory capacity of DDR4. DDR5 supports 6.0 GT/s and one terabit (Tb) of memory, as well as improved power efficiency. DDR5 will provide the performance enhancements and power management capabilities needed to support 400GE networking speeds in the data center.
### DDR5 Introduces New Design and Test Challenges

DDR memory is everywhere — not just in servers, workstations, and desktops, but also embedded in consumer electronics, automobiles, and other system designs. The DDR standard provides fast access to data stored in memory in a multitude of consumer devices, as well as in the data center.

As the speed of DDR technology increases, engineers face new design and validation challenges. Design error margins decrease, and signal integrity becomes more challenging to maintain. Test and measurement solutions enable DDR5 designers to optimize their transmitter, receiver, and channel designs for best performance and reliability at the increased data transfer rate of 6 GT/s.

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**Figure 3: Evolution of the DDR standard**
3 Design and Test Challenges of DDR5

1. DDR Design and Simulation
Each new version of the DDR standard supports faster access to data stored in memory. Design and simulation of next-generation DDR5 memory designs enable chip designers and device manufacturers to discover issues before silicon tapeout and to maximize the signal integrity of their designs. Using design and simulation tools, DDR5 designers can quickly resolve signal integrity issues, ensure power efficiency, and stay within tight error margins before first prototypes.

2. DDR Physical Layer Test
DDR5 transmitter (Tx) and receiver (Rx) designs need to comply with the DDR specifications defined by the JEDEC to ensure interoperability with components and devices from other vendors in the system. Each new generation of the standard introduces new DDR physical layer test requirements. DDR5 introduces new receiver compliance tests, not required in previous generations of the standard.

3. PCIe Protocol Validation
Data corruption is a common symptom encountered during DDR design validation, and its root cause can be difficult to determine. Usually, there are either signal integrity or functional issues with the designs. When DDR memory systems do not behave as expected, designers need functional debug, analysis, and protocol compliance validation solutions. Test solutions that provide trace capture and analysis capabilities provide designers the insight required to understand their system’s behavior and quickly find the root cause of any issues.
DDR5 Test Solutions

Each new version of the LPDDR / DDR standards supports faster access to data stored in memory. As the speed of double data rate technology increases, designers face new design and validation challenges.

Measurement methods and tools developed to test to precise industry specifications allow designers to focus on designing instead of trying to understand the details and requirements of each new generation of the standard. The right test solutions ensure the quality and performance of next-generation DDR designs and help companies get them to market faster.
CHAPTER 3
Emerging Standards for Optimized Designs
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OpenCAPI, Gen-Z, and CCIX

New interconnect standards, such as Open Coherent Accelerator Processor Interface (OpenCAPI), Gen-Z, and Cache Coherent Interconnect for Accelerators (CCIX), offer alternatives to the PCIe standard. These bus standards are optimized for application-specific use cases, such as low-latency interconnect, unsupervised direct memory access, and cache coherency.

3 New Interconnect Standards Emerge

1. **OpenCAPI Accelerates Computing**
   OpenCAPI is an open, coherent, high-performance bus standard that accelerates computing through tighter integration of different types of technologies within servers, such as advanced memory, accelerators, networking, and storage. The OpenCAPI standard, defined by the OpenCAPI Consortium, provides 25 Gbps data rate and aims to improve server performance by moving computing power closer to the data. OpenCAPI creates a very low latency interface between the CPU and an attached device, removing bottlenecks caused by I/O inefficiencies.

2. **Gen-Z Targets Memory-to-CPU Connections**
   Gen-Z, defined by the Gen-Z Consortium, is an open interconnect standard optimized for storage technology to increase the speed of memory-to-CPU connections. Gen-Z version 1.0, based on IEEE-802.3 physical layer specifications, provides 25 GT/s and 28 GT/s interconnect speeds and is scalable to 112 GT/s and higher. Gen-Z components use low-latency read and write operations for direct data access with minimal application or processor involvement.

3. **CCIX Increases Data Throughput**
   The principle behind CCIX, defined by the CCIX Consortium, is to use the PCIe physical (PHY) layer but to change the function of the bus for increased efficiency and faster speeds. The CCIX standard currently supports data rates up to 25 Gbps and is expected to extend that to 40 Gbps soon. In addition to faster interconnect speeds, CCIX enables cache coherency. Cache coherency quickly propagates any changes to data in one area of memory to all other instances of the data stored in different memory locations throughout the entire system. For example, there can be a copy of data in main memory as well as one in the local cache of every processor that has previously requested the data. With cache coherency, CPUs can communicate faster with the rest of the system.
400GE Introduces New Test Challenges

Four considerations for high-speed computing interfaces to support 400GE in the data center
Higher Data Rates Increase Complexity

High-speed serial data link design becomes significantly more complex as data rates increase. Channel topologies become more diverse, and the number of parameters tuned for active components multiply. High-speed computing interface designers must solve signal integrity challenges to achieve 400GE speeds. With the right tools, you can optimize transmitter, receiver, and channel designs to achieve the best performance and reliability at the desired data rate. These tools allow you to resolve signal integrity issues up front, ensure power efficiency, and stay within tight error margins before the first prototypes.
Testing Compliance to Industry Standards

Test engineers must develop comprehensive test plans to ensure compliance with industry standards and interoperability with devices from other vendors. Test requirements differ drastically from one generation to the next, creating new challenges that must be overcome. For example, the DDR5 standard specifies that test engineers need to test both the transmitter and the receiver. Previous DDR technologies required only transmitter testing. Testing new interconnect technologies, such as OpenCAPI, Gen-Z, or CCIX, present new challenges because test engineers have never tested them before. The right tools help engineers ramp up quickly on test requirements and procedures.

Compliance test software developed in accordance to industry standards can reduce test time from days or weeks to hours. Industry compliant test solutions ensure that next-generation devices comply with industry standards and are interoperable with devices from other vendors. Using fully compliant test solutions, engineers can focus on designing next-generation devices, instead of learning the details of each new standard.
Summary

Evolution of High-Speed Computing Interfaces

As data center operators begin the migration of their data center networks from 100GE to 400GE, they need a migration plan that delivers the next-generation of high-speed computing interfaces such as PCIe 5.0 and DDR5.

New interconnect standards, such as OpenCAPI, Gen-Z, and CCIX, designed to optimize specific data transfer functions, provide alternatives to PCIe yet introduce another level of complexity for high-speed digital designers. Test solutions designed to test specific industry standards reduce test time and ensure compliance and interoperability of devices. Data center operators can ensure a smooth transition to the next speed class by choosing network equipment that has been thoroughly tested to conform to industry standards.

FOR MORE INFORMATION

To find out how Keysight solutions can help you address your high-speed computing interface design and test challenges, check the following links:

- To accelerate the time-to-market of your gigabit digital designs, check out High-Speed Digital System Design
- To learn more about test solutions to simulate, characterize, and validate your PCIe designs, check out PCI Express (PCIe) Design and Test
- To learn how to quickly and accurately test all required parameters in your DDR designs and get them to market faster, check out Double Data Rate (DDR) Memory Design and Test