IBIS Models

Agilent Technologies
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CAUTION
A CAUTION notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.

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A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.
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This chapter introduces the IBIS Models in terms of their use model and interface.
Overview

IBIS Models provides easy and reliable access to IBIS technology that is compliant with the current standard and accurate in its simulation results.

This feature provides the following:
• an interface between ADS and the standard IBIS parser (currently supporting version 4.2)
• ADS components for each high-level IBIS model type
• a generic IBIS component
• a schematic palette of these built-in IBIS components
• an IBIS model in the ADS simulator

Use Model

The primary use for IBIS models is designing memory modules and boards. You can also use these models to design equalized backplane and cable assemblies.

These models are not designed for use in creating very high speed driver and receiver circuits above 5 GB/sec.
Implementation Limitations

Presently, IBIS Models are not compliant with the following specification parameters:

- [Pin Mapping]
- Series models: [Series Pin Mapping], [Series Switch Groups], [On], [Off], [R/L/R1/C/Lc/Rc Series], [Series Current], [Series MOSFET]
- [Model Spec]
- [Receiver Thresholds]
- [Add Submodel] and [Submodel]
- Internal power supply: [Pullup/Pulldown/POWER Clamp/GND Clamp/External Reference or Voltage Reference]
- Board description files (*.ebd)
- Package files (*.pkg): [Package Model], [Alternate Package Models], [Define Package Model]
- External models and circuits: [External Model], [External Circuit], [Node Declarations], [Circuit Call]
- [Test Data]
- [External Reference]

Presently, Interconnect Modeling (ICM) is not supported. Neither keyword form or file form packages are supported.
1 Introducing IBIS Models

IBIS Models Main Dialog

This feature provides IBIS file choice and high-level parameter configuration through its main dialog and detailed parameter configuration through six tabs.

**IBIS File** Click **Select IBIS File** to browse to the .ibs file containing your model. This field is initially blank and not directly editable. With the exception of the Display tab, all other tabs and fields are inactive and blank until content is available.

**Component** The component name to use from the IBIS file. Default component is the first choice.

**Set all data** Select this checkbox to set all the model’s fields as typical, minimum, or maximum (Typ, Min, Max or one of two predefined combinations: Fast or Slow). Selecting this checkbox disables other Typ/Min/Max fields and allows
Typ/Min/Max/Fast/Slow values. Selecting Fast and Slow sets some fields to Min and others to Max in the model. This parameter is selected (On) by default.

To configure a particular set of parameters:

1. Click on the associated tab.
2. Configure the parameters.
3. Click Apply > OK.

**Package Tab**

**R/L/C_pkg** Data type to be extracted from the IBIS file for R/L/C_pkg under the [Package] keyword if **Set all data** is Off.
## Pin Tab

**Name**  
Pin number of an IC, or the non-inverting pin number for a differential buffer. Default value is the first choice.

**Model Selector**  
Current model selected. Disabled and empty if irrelevant for selected pin. Default is first choice.

**Package Overrides**  
Values are informational. If not present in the IBIS file, values are blank. If Use package is deselected (Off), these fields are blank and disabled. If present and Use package is selected, these values will override those shown on the Package tab.

**Pin Mapping**  
Lists pin references in the IBIS file. Disabled and empty if not included in IBIS file.
Introducing IBIS Models

**Differential Pin**  Lists values for the differential pin, if present in the IBIS file. Disabled and empty if not included in IBIS file.

**Model Tab**

![](image)

**Model Information**  General information read from the IBIS file.

**Die Capacitances**  These fields are enabled/disabled and populated as appropriate. Typ/Min/Max can be specified if Set all data is deselected (Off). Values are informational.

**Ttngnd, Ttpower, Rgnd, Rpower, Rac, Cac**  These fields are enabled/disabled and populated as appropriate. Typ/Min/Max can be specified if Set all data is deselected (Off). Values are informational.
I-V Data Tab

**Voltage Range**  Values are informational. Always disabled and empty if not included in IBIS file.

**Pullup, Pulldown, POWER Clamp, GND Clamp**  Typ/Min/Max can be specified if Set all data is deselected (Off).

**Pullup Ref, Pulldown Ref, POWER Clamp Ref, GND Clamp Ref**  Values are informational.

**Rising/Falling Waveform, Ramp**  Typ/Min/Max can be specified if Set all data is deselected (Off). This parameter determines which values will be used during simulation. Rising/Falling waveform data is more accurate than Ramp data.
**Driver Schedule Tab**

Entire tab is disabled if irrelevant for the selected component/pin/model. Table content is informational.
1 Introducing IBIS Models

Display Tab

To display parameter values on the schematic page, select the associated checkbox.

**NOTE**

The following parameters are not editable from the schematic page: File, Component, Pin, Inverting Pin, and ModelName.
This appendix covers IBIS model symbols, parameters, equivalent circuits, and notes.
A IBIS Model Reference

Overview

IBIS Models provides built-in components representing each high-level type of IBIS model.

Most IBIS models have a specific pin configuration for wiring within a circuit schematic. Each model has a component dialog that displays only those pin/model/[Diff Pin] combinations that match the component's model type.

In addition, this feature provides a generic IBIS component that furnishes a mechanism for selecting any type of supported IBIS model. The generic component has no pins and will not run in the simulator. The generic IBIS model uses the same dialog as the other IBIS components, but it displays all supported pin/model combinations available in the IBIS file. Once you specify enough information to determine the type of IBIS model and apply the settings, the generic component transforms into the appropriate IBIS component.

Definitions

- **buffer state** refers to the die (pad) voltage, either low or high. High-Z refers to the high impedance state.

- **digital output** refers to the voltage at the node DgO (Digital Output) which can be either 0 or 1 depending on the buffer state and polarity.
**disable event** refers to the voltage at the node E (or Enable) and represents a change of the buffer state from enabled to disabled.

Enable/disable events take place when the voltage at node E crosses the same trigger thresholds as specified by the TriggerLevel parameter value M. If the parameter Enable is set to Active-High, the enable event occurs when the buffer state is disabled and the voltage at node E becomes greater than the value of M. If the parameter Enable is set to Active-High, the disable event happens when the buffer is enabled and the voltage at node E becomes smaller than the value of (1−M). The opposite applies when the parameter Enable is set to Active-Low. If the enable state is undefined (for example, at the beginning of the simulation) the initial enable state is determined as disabled or enabled depending on whether $V_E \leq 0.5$ or $V_E > 0.5$, respectively.

**enable event** refers to the voltage at the node E and describes a change of the buffer state from disabled to enabled.

**enable state** refers to the voltage at the node E. The buffer can be enabled or disabled depending whether the IBIS model parameter Enable is set to Active-High or Active-Low, to interpret the actual voltage for each state.

**falling transition** refers to the die voltage going from high to low.

**rising transition** refers to the die voltage going from low to high.

**trigger event** refers to the voltage at the node T (Trigger or Digital Input) and represents a change of trigger state. The trigger events happen when the voltage at node T crosses the trigger threshold specified by the value of TriggerLevel parameter M. There are two types of trigger events: (1) when the trigger state is low and the voltage at node T becomes greater than the value of M ($0.5 \leq M < 1$), and (2) when the trigger state is high and the voltage at node T becomes smaller than the value of $(1-M)$. The following descriptions typically refer to non-inverting buffers. It applies to the inverting buffers by interchanging the trigger states.
A  IBIS Model Reference
Model Parameters

Depending on the model type, IBIS models will have some or all of the following parameters:

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Values</th>
<th>Default</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>IbisFile</td>
<td>IBIS file name</td>
<td>User selectable</td>
<td>Required</td>
<td></td>
</tr>
<tr>
<td>ComponentName</td>
<td>IC identifier</td>
<td>User selectable</td>
<td>Not required</td>
<td></td>
</tr>
<tr>
<td>PinName</td>
<td>Pin number of an IC, or the non-inverting pin number for a differential buffer</td>
<td>User selectable</td>
<td>Not required</td>
<td>In case when the selected pin is one of the pins in the keyword [Diff Pin] this is set to the first (non-inverting) pin.</td>
</tr>
<tr>
<td>InvPinName</td>
<td>Inverting pin number for a differential buffer</td>
<td>Required for all differential buffers. Automatically set if the selected [Pin] is one of the pins in [Diff Pin].</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ModelName</td>
<td>IBIS file model name</td>
<td>Required</td>
<td>Follows ComponentName and PinName selections. Redundant if both are specified and [Model Selector] is not used.</td>
<td></td>
</tr>
<tr>
<td>SetAllData</td>
<td>Flag to use Data type set by the DataTypeSelector for all data and ignore individual parameter settings</td>
<td>yes, no</td>
<td>yes</td>
<td>User selectable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Not required</td>
<td></td>
</tr>
<tr>
<td>DataTypeSelector</td>
<td>A global setting of data type to be extracted from the IBIS file.</td>
<td>1 - typ 2 - min 3 - max 4 - fast 5 - slow</td>
<td>1</td>
<td>User selectable</td>
</tr>
</tbody>
</table>
UsePkg | Flag to ignore the package description in the IBIS file (as set by R/L/C_pkg or R/L/C_pin) and exclude the package components from the equivalent circuit. | yes, no | yes | User selectable | Not required |
RpkgType | Data type to be extracted from the IBIS file for R_pkg under the [Package] keyword. | 1 - typ, 2 - min, 3 - max | 1 | User selectable | Not required |

LpkgType | Data type to be extracted from the IBIS file for L_pkg under the [Package] keyword. | 1 - typ, 2 - min, 3 - max | 1 | User selectable | Not required |
<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Values</th>
<th>Default</th>
<th>Notes</th>
</tr>
</thead>
</table>
| CpkgType           | Data type to be extracted from the IBIS file for C_pkg under the [Package] keyword. | 1 - typ  
2 - min  
3 - max   | User selectable  
Not required  
Ignored if SetAllData=yes or if UsePkg=uno  
Ignored if C_PIN is specified in the IBIS file under the [Pin] keyword for the selected PinName (the value of C_PIN overrides the value of C_PKG)  
To avoid simulation errors, all values listed in the IBIS file for typ, min, and max must be real numbers. | |
| DiffTimeDelayType  | Data type to be extracted from the IBIS file as the time delay between the inverting and non-inverting pins for differential buffers, specifically the launch delays of the non-inverting pins relative to the inverting pins. | 1 - tdelay Typ  
2 - tdelay Min  
3 - tdelay Max   | User selectable  
Not required  
Ignored if SetAllData=yes | |
| CcompType          | Data type to be extracted from the IBIS file for the die capacitance C_comp, or C_comp_* if they are specified and used. | 1 - typ  
2 - min  
3 - max   | User selectable  
Not required  
Ignored if SetAllData=yes | |
| TgndType           | Data type to be extracted from the IBIS file for the transit time for the ground clamp diffusion capacitance. | 1 - typ  
2 - min  
3 - max   | User selectable  
Not required  
Ignored if SetAllData=yes | |
| TpowerType         | Data type to be extracted from the IBIS file for the transit time for the power clamp diffusion capacitance. | 1 - typ  
2 - min  
3 - max   | User selectable  
Not required  
Ignored if SetAllData=yes | |
| RgndType           | Data type to be extracted from the IBIS file for the parasitic resistance Rgnd in a terminator buffer. | 1 - typ  
2 - min  
3 - max   | User selectable  
Not required  
Ignored if SetAllData=yes | |
| RpowerType         | Data type to be extracted from the IBIS file for the parasitic resistance Rpower in a terminator buffer. | 1 - typ  
2 - min  
3 - max   | User selectable  
Not required  
Ignored if SetAllData=yes | |
<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Values</th>
<th>Default</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>RacType</td>
<td>Data type to be extracted from the IBIS file for the AC terminator resistance Rac.</td>
<td>1 - typ 2 - min 3 - max</td>
<td>1</td>
<td>User selectable  Not required  Ignored if SetAllData=yes</td>
</tr>
<tr>
<td>CacType</td>
<td>Data type to be extracted from the IBIS file for the AC terminator capacitance Cac.</td>
<td>1 - typ 2 - min 3 - max</td>
<td>1</td>
<td>User selectable  Not required  Ignored if SetAllData=yes</td>
</tr>
<tr>
<td>PuDataTpe</td>
<td>Data type to be extracted from the IBIS file as I-V data for the pullup device.</td>
<td>1 - typ 2 - min 3 - max</td>
<td>1</td>
<td>User selectable  Not required  Ignored if SetAllData=yes</td>
</tr>
<tr>
<td>PoDataTpe</td>
<td>Data type to be extracted from the IBIS file as I-V data for the pulldown device.</td>
<td>1 - typ 2 - min 3 - max</td>
<td>1</td>
<td>User selectable  Not required  Ignored if SetAllData=yes</td>
</tr>
<tr>
<td>PcDataTpe</td>
<td>Data type to be extracted from the IBIS file as I-V data for the power clamp.</td>
<td>1 - typ 2 - min 3 - max</td>
<td>1</td>
<td>User selectable  Not required  Ignored if SetAllData=yes</td>
</tr>
<tr>
<td>GcDataType</td>
<td>Data type to be extracted from the IBIS file as I-V data for the ground clamp.</td>
<td>1 - typ 2 - min 3 - max</td>
<td>1</td>
<td>User selectable  Not required  Ignored if SetAllData=yes</td>
</tr>
<tr>
<td>WaveformType</td>
<td>Data type to be extracted from the IBIS file for the rising and falling waveforms.</td>
<td>1 - typ 2 - min 3 - max</td>
<td>1</td>
<td>User selectable  Not required  Ignored if SetAllData=yes</td>
</tr>
<tr>
<td>RampType</td>
<td>Ramp data type to be extracted from the IBIS file for the rising and falling transitions.</td>
<td>1 - typ 2 - min 3 - max</td>
<td>1</td>
<td>User selectable  Not required  Ignored if SetAllData=yes</td>
</tr>
<tr>
<td>IgnoreWaveforms</td>
<td>Flag to use the [Ramp] data even if the waveform tables are provided in the IBIS file.</td>
<td>yes, no</td>
<td>no</td>
<td>User selectable  Not required  Ignored if SetAllData=yes</td>
</tr>
</tbody>
</table>
### IBIS Models

#### Polarity

Flag to override the IBIS file setting for the [Polarity] keyword.

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Values</th>
<th>Default</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polarity</td>
<td>Flag to override the IBIS file setting for the [Polarity] keyword.</td>
<td>0 = non-inverting</td>
<td>0</td>
<td>User selectable</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = inverting</td>
<td></td>
<td>Not required</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Must not be netlisted if the IBIS file setting is to be used.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The default of “non-inverting” is used if the model polarity is</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>not specific in the IBIS file.</td>
</tr>
</tbody>
</table>

- **TriggerLevel**: The voltage level at the input node T (Digital In) of a non-inverting output buffer triggering the rising transition from a “low” state to “high” state. The one-complement is used for the opposite event. The range is **[0.5, 1.0)**.

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Values</th>
<th>Default</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TriggerLevel</td>
<td>The voltage level at the input node T (Digital In) of a non-inverting output buffer triggering the rising transition from a “low” state to “high” state. The one-complement is used for the opposite event.</td>
<td>range: [0.5, 1.0)</td>
<td>0.5</td>
<td>Not required</td>
</tr>
</tbody>
</table>
IBIS (Generic Model)

Symbol

Available in ADS

Parameters  See "Model Parameters" on page 19.

Notes/Equations
1 Provides a mechanism for selecting any type of IBIS model.
2 Because the generic component can be used to specify any one of the IBIS model types, it has no pins and cannot be simulated.
3 This component shows all supported pin/model combinations available for the selected component in the IBIS file.
4 When you specify enough information to determine the type of IBIS model and apply the settings, the generic model transforms into the appropriate specialized component.
**IBIS_3S (3-State)**

**Symbol**

![IBIS_3S Symbol](image)

**Available in ADS**

**Parameters**  See "Model Parameters" on page 19.

**Equivalent Circuit**

![IBIS_3S Equivalent Circuit](image)

**Notes/ Equations**

1. This buffer behaves like "IBIS_O (Output)" if the buffer is enabled.
2. If the buffer is disabled the buffer state becomes high-Z.
3. The transitions between the enabled and disabled states follow the enable/disable events.
4. Enable = ActiveHigh
   - Time = 0
     - Disable State if VE < 0.5
     - Enable State if VE ≥ 0.5
Time > 0
- Disabling trigger if VE < 1 – TriggerLevel
- Enabling trigger if VE ≥ TriggerLevel

Enable = ActiveLow

Time = 0
- Enable State if VE ≤ 0.5
- Disable State if VE > 0.5

Time > 0
- Enabling trigger if VE ≤ 1 – TriggerLevel
- Disabling trigger if VE > TriggerLevel
IBIS Model Reference A

IBIS_D3S (Differential 3-State)

Symbol

Available in ADS

Parameters See "Model Parameters" on page 19.

Equivalent Circuit
Notes/Equations
1 This buffer consists of two 'IBIS_3S (3-State)' buffers, one non-inverting and one inverting.
2 The trigger event can be delayed for one of the buffers.
3 This delay is controlled by the value of the subparameter $t_{\text{delay\_typ}}, t_{\text{delay\_min}}, t_{\text{delay\_max}}$ (whichever is selected) under the keyword [Diff Pin] in the IBIS file.
4 Which buffer gets a delayed trigger event depends on the sign of $t_{\text{delay}}$:
   If $t_{\text{delay}} \geq 0$
   \[
   \text{DelayNI} = t_{\text{delay}} \quad \text{DelayI} = 0
   \]
   If $t_{\text{delay}} < 0$
   \[
   \text{DelayNI} = 0 \quad \text{DelayI} = -t_{\text{delay}}
   \]
IBIS DI (Differential Input)

Symbol

Available in ADS

Parameters See “Model Parameters” on page 19.
This buffer consists of two ‘IBIS_I (Input)’ buffers.

It can function as a driver: it supports digital output which can assume the values of 0 or 1 depending on the voltage difference between the nodes InNI and InI as compared to the IBIS model parameter vdif specified under the [Diff Pin] keyword.

There are no separate thresholds and the absolute value of vdif is used, as follows:

\[ \text{digital output} = 0 \text{ if } V_{\text{InNI}} - V_{\text{InI}} < \text{vdif} \]
\[ \text{digital output} = 1 \text{ if } V_{\text{InNI}} - V_{\text{InI}} > \text{vdif} \]
IBIS_DIO (Differential Input/Output)

Symbol

Available in ADS

Parameters See "Model Parameters" on page 19.
Equivalent Circuit

Notes/Equations

1. This buffer consists of two “IBIS_IO (Input/Output)” buffers, one non-inverting and one inverting.

2. Depending on the enable state, this model acts as a “IBIS_DO (Differential Output)” buffer or a “IBIS_DI (Differential Input)” buffer.
IBIS_DIO_OPENSINK (Differential I/O Open Sink)

Symbol

Available in ADS

Parameters  See ‘Model Parameters’ on page 19.

Equivalent Circuit
Notes/Equations

1 This buffer consists of two “IBIS_IO_OPEN (I/O Open Sink)” buffers, one non-inverting and one inverting.

2 The functionality follows that of the “IBIS_DOPENSINK (Differential Open Sink)” buffer or the “IBIS_DI (Differential Input)” buffer depending on the enable state.
IBIS_DIO_OPENSOURCE (Differential I/ O Open Source)

Symbol

Available in ADS

Parameters See ‘Model Parameters’ on page 19.

Equivalent Circuit
Notes/ Equations
1. This buffer consists of two "IBIS_IO_OPENSOURCE (I/O Open Source)" buffers, one non-inverting and one inverting.
2. The functionality follows that of the "IBIS_DOPENSOURCE (Differential Open Source)" buffer or the "IBIS_DI (Differential Input)" buffer depending on the enable state.
IBIS Model Reference

IBIS Models

IBIS DO (Differential Output)

Symbol

Available in ADS

Parameters

See “Model Parameters” on page 19.

Equivalent Circuit
Notes/Equations

1. This buffer consists of two “IBIS_O (Output)” buffers, one non-inverting and one inverting.
2. The trigger event can be delayed for one of the buffers.
3. This delay is controlled by the value of the subparameter tdelayTyp, tdelay_min, tdelay_max (whichever is selected) under the keyword [Diff Pin] in the IBIS file.
4. Which buffer gets a delayed trigger event depends on the sign of tdelay:
   - If tdelay ≥ 0
     DelayNI = tdelay  DelayI = 0
   - If tdelay < 0
     DelayNI = 0  DelayI = −tdelay
IBIS_DOPENSINK (Differential Open Sink)

Symbol

Available in ADS

Parameters  See ‘Model Parameters’ on page 19.

Equivalent Circuit
Notes/ Equations

1. This buffer consists of two “IBIS_OPENSINK (Open Sink)” buffers, one non-inverting and one inverting.

2. The trigger event can be delayed for one of the buffers.

3. This delay is controlled by the value of the subparameter tdelay_typ, tdelay_min, tdelay_max (whichever is selected) under the keyword [Diff Pin] in the IBIS file.

4. Which buffer gets a delayed trigger event depends on the sign of tdelay:
   - If tdelay $\geq 0$
     - DelayNI = tdelay
     - DelayI = 0
   - If tdelay < 0
     - DelayNI = 0
     - DelayI = $-tdelay$
IBIS_DOPESOURCE (Differential Open Source)

Symbol

Available in ADS

Parameters  See "Model Parameters" on page 19.

Equivalent Circuit
Notes / Equations

1. This buffer consists of two ‘IBIS_OPENSOURCE (Open Source)’ buffers, one non-inverting and one inverting.
2. The trigger event can be delayed for one of the buffers.
3. This delay is controlled by the value of the subparameter `tdelay_typ`, `tdelay_min`, `tdelay_max` (whichever is selected) under the keyword [Diff Pin] in the IBIS file.
4. Which buffer gets a delayed trigger event depends on the sign of `tdelay`:
   - If `tdelay` ≥ 0
     \[ \text{DelayNI} = \text{tdelay} \quad \text{DelayI} = 0 \]
   - If `tdelay` < 0
     \[ \text{DelayNI} = 0 \quad \text{DelayI} = -\text{tdelay} \]
IBIS_DT (Differential Terminator)

Symbol

Available in ADS

Parameters  See "Model Parameters" on page 19.
1 This buffer consists of two “IBIS_T (Terminator)” buffers.
2 This buffer is similar to the “IBIS_DI (Differential Input)” buffer without the digital output and with additional parasitic components.
**IBIS Model Reference**

**IBIS_I (Input)**

**Symbol**

![Symbol Diagram]

**Available in ADS**

**Parameters**  See “Model Parameters” on page 19.

**Equivalent Circuit**

![Equivalent Circuit Diagram]

**Notes/ Equations**

1. This buffer can function as a driver.
2. It supports digital output which can assume the values of 0 or 1 depending on the voltage at the node In as compared to the IBIS model parameters Vinl and Vinh, and polarity.
**IBIS IO (Input/Output)**

**Symbol**

![Symbol Image]

**Available in ADS**

**Parameters** See “Model Parameters” on page 19.

**Equivalent Circuit**

![Equivalent Circuit Image]

**Notes/Equations**

1. This is the most commonly used buffer and it functions as either the “IBIS_O (Output)” buffer or the “IBIS_I (Input)” buffer depending on the enable state.

2. If the buffer is disabled, it behaves as an “IBIS_I (Input)” buffer with input node IO (it is In for the Input buffer).

3. In the Input mode, the buffer supports digital output which can assume the values of 0 or 1 depending on the voltage at the node IO as compared to the IBIS model parameters Vinl and Vinh, and polarity.
4 When the buffer is enabled it functions as an “IBIS_O (Output)” buffer. However the voltage source Dig0 is still active.

5 This buffer is a combination of the “IBIS_3S (3-State)” and “IBIS_I (Input)” buffers.
IBIS_IO_OPENSINK (I/O Open Sink)

Symbol

Available in ADS

Parameters  See “Model Parameters” on page 19.

Equivalent Circuit

Notes/Equations

1. This buffer does not have the pullup device. Otherwise, all rules of the “IBIS_IO (Input/Output)” buffer apply.
**IBIS_IO_OPENSOURCE (I/O Open Source)**

**Symbol**

Available in ADS

**Parameters**  See "Model Parameters" on page 19.

**Equivalent Circuit**

**Notes/ Equations**

1. This buffer does not have the pulldown device. Otherwise, all rules of the "IBIS_IO (Input/Output)" buffer apply.
IBIS_O (Output)

Symbol

Available in ADS

Parameters
See “Model Parameters” on page 19.

Equivalent Circuit

Notes/Equations

2 The trigger event results in a rising or falling trigger depending on the voltage at the node T as compared to the parameter TriggerLevel and polarity.

3 Polarity = Non-Inverting
Time = 0
Low State if VT < 0.5
High State if VT ≥ 0.5
Time > 0
   Falling trigger if VT < 1 – TriggerLevel
   Rising trigger if VT ≥ TriggerLevel
4 Polarity= Inverting
   Time = 0
      High State if VT ≤ 0.5
      Low State if VT > 0.5
   Time > 0
      Rising trigger if VT ≤ 1 – TriggerLevel
      Falling trigger if VT > TriggerLevel
IBIS OPENSINK (Open Sink)

Symbol

Available in ADS

Parameters  See "Model Parameters" on page 19.

Equivalent Circuit

Notes/Equations

1 This buffer does not have the pullup device. Otherwise, all rules of the "IBIS_O (Output)" buffer apply.
**IBIS_OPENSOURCE (Open Source)**

**Symbol**

![Symbol Diagram](image)

**Available in ADS**

**Parameters** See ‘Model Parameters’ on page 19.

**Equivalent Circuit**

![Equivalent Circuit Diagram](image)

**Notes/Equations**

1. This buffer does not have the pulldown device. Otherwise, all rules of the ‘IBIS_O (Output)’ buffer apply.
IBIS T ( Terminator )

Symbol

Available in ADS

Parameters  See “Model Parameters” on page 19.

Equivalent Circuit

Notes/Equations
1 This buffer is similar to the “IBIS_I (Input)” buffer without the digital output and with additional parasitic components.
This appendix covers obsolete signal integrity model symbols, parameters, and notes.
Overview

IBIS Version 3.2 models are commonly used for analysis and design of high-speed printed circuit boards.

The IBIS driver (output) models provide the waveform as it appears at the output pin on an IC for a given loading condition. The receiver (input) model provides the nonlinear terminating impedance as presented by the IC pin.

The IBIS equivalent circuit of a typical chip I/O structure includes five basic elements: pull-down driver, pull-up driver, power supply and ground clamping diodes, slew rate of the waveform, and parasitic elements associated with each pin.

![Output Driver Diagram](image)

**Figure 1** Output Driver

NOTE

These obsolete signal integrity components have been included for backwards compatibility. Use the latest IBIS models (see "IBIS Model Reference" on page 15) to create new designs.
The pull-down driver models I/O buffer characteristics when driven low or towards ground voltage. The pull-up driver models the characteristic when driven high or towards the power supply voltage.

A power supply clamping diode is connected between output and power supply ports. It is used to prevent the output waveform from swinging above the power supply voltage, referred to as beyond-the-rail circuit protection. The ground clamping diode (between the output and ground ports) prevents any voltage transition going below ground voltage.

The parasitic elements consist of $C_{\text{comp}}$, resistive, inductive, and capacitive pin package parasitics.

$C_{\text{comp}}$ is an inherent capacitance between silicon die and mounted substrate; its value is estimated for every pin.

There are two kinds of pin package parasitics: individual pin parasitics and global defaults. Individual pin parasitics $R_{\text{pin}}$, $L_{\text{pin}}$ and $C_{\text{pin}}$ can be estimated or measured accurately and are specified in the pin section if the .ibs file. Global defaults (or average values) $R_{\text{pkg}}$, $L_{\text{pkg}}$, and $C_{\text{pkg}}$ can be found on the component section of the file and are used when no individual pin parasitics are specified. Individual $R_{\text{pin}}$, $L_{\text{pin}}$, and $C_{\text{pin}}$ values, if specified, are more accurate than the global defaults. $R_{\text{pin}}$, $L_{\text{pin}}$, and $C_{\text{pin}}$ replace corresponding values of $R_{\text{pkg}}$, $L_{\text{pkg}}$ and $C_{\text{pkg}}$ respectively.

Statistically, device characteristics deviate due to variations in device operation temperature and variations and fluctuations in the underlying fabrication processes. Three different characteristic values (typical, minimum and maximum values) are available to reflect these deviations in device performance. Minimum specifies an IC manufactured using slow process characteristics, such as 75 MHz CPU; maximum specifies an IC manufactured using fast process characteristics, such as 135 MHz CPU.

The IBIS models can be edited on screen to change the pin number. Once the pin number is selected, all the model parameters are automatically selected. Select only the pin number and the type of model parameters (Minimum,
Typical, or Maximum). Other parameter numeric values (for example, mode file, pin parasitics and the voltage range equivalent circuit) will be automatically selected.

A sample IBIS data file is supplied with ADS and can be accessed from DesignGuides > IBIS Library > Examples > Sample IBIS Data File. This will copy lab_1.ibs file to your current project directory.

The DesignGuides > IBIS Library > Component Palette provides access to Buffer Library components. The components in Buffer Library provide easy-to-use sub-circuits for high-speed simulation.
Obsolete IBIS Models Import

NOTE

These obsolete signal integrity components have been included for backwards compatibility. Use the latest IBIS models (see “IBIS Model Reference” on page 15) to create new designs.

The Agilent EESof IBIS Data Import provides the capability to import IBIS Version 3.2 models (.ibs) in ADS.

To import IBIS models in ADS:

1. In the ADS schematic window, select DesignGuides > IBIS Library > IBIS Model Import to open the IBIS translator.

![Figure 2 Importing IBIS Version 3.2 Models](image)

2. Click Select IBIS Data File to select the .ibs file that corresponds to the IC component of interest. Browse and select the IBIS data file.

3. Enter the desired IBIS design kit name.
4 Select the **Customize Bitmap** checkbox and enter text in the Bitmap Caption entry field to add captions to the bitmap palettes.

**NOTE**
The IBIS translator allows you to add multiple components in the same design kit. To identify the different IC component, you can select different bitmap captions for different .ibs files. If you are adding components to an existing IBIS designkit, restart ADS to access the newly added components.

5 Click **Create IBIS Design Kit** button to create the design kit.
6 In the ADS Main window, select **DesignKit > Install DesignKits** to install the IBIS design kit.
7 Using **Browse** button located next to the Path edit field, select the designkit directory, located in your home directory.

Once the IBIS design kit is installed, all the IBIS components will be available as the first item in your component palette. Select the IBIS component and use it in your design. In an IBIS component, the power supply port (labeled Vd) receives power supply voltage. The ground port (labeled Vg) provides the ground connection.

The following steps are performed during IBIS model translation:
1. The IBIS file is parsed through an IBIS parser.
2. All pins are grouped based on IBIS Model Type.
3. ADS component Form Sets and component definition are created as `/circuit/ael/*.ael` files.
4. IBIS data is stored as `.mdf` files under `/circuit/data` directory.
5. The ADS design kit is created.
## Obsolete IBIS Model Types and Bitmap Representations

IBIS simulation in ADS2005A supports basic IBIS models and Vt tables. Not all the keywords defined in the IBIS specifications are supported. The following table shows the supported IBIS model types and their bitmap representation.

<table>
<thead>
<tr>
<th>Model Type</th>
<th>Bitmap Label</th>
<th>Bitmap</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output</td>
<td>O</td>
<td><img src="image" alt="Output Bitmap" /></td>
</tr>
<tr>
<td>3-state</td>
<td>3S</td>
<td><img src="image" alt="3-state Bitmap" /></td>
</tr>
<tr>
<td>V/O</td>
<td>IO</td>
<td><img src="image" alt="V/O Bitmap" /></td>
</tr>
<tr>
<td>Open_source</td>
<td>OS</td>
<td><img src="image" alt="Open_source Bitmap" /></td>
</tr>
<tr>
<td>Open_sink</td>
<td>OD</td>
<td><img src="image" alt="Open_sink Bitmap" /></td>
</tr>
<tr>
<td>V/O_open_source</td>
<td>OS</td>
<td><img src="image" alt="V/O_open_source Bitmap" /></td>
</tr>
<tr>
<td>V/O_open_sink</td>
<td>OD</td>
<td><img src="image" alt="V/O_open_sink Bitmap" /></td>
</tr>
<tr>
<td>Input</td>
<td>I</td>
<td><img src="image" alt="Input Bitmap" /></td>
</tr>
<tr>
<td>Terminator</td>
<td>T</td>
<td><img src="image" alt="Terminator Bitmap" /></td>
</tr>
</tbody>
</table>
## B Obsolete IBIS Model Reference

<table>
<thead>
<tr>
<th>Model Type</th>
<th>Bitmap Label</th>
<th>Bitmap</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differential Input</td>
<td>DI</td>
<td><img src="image" alt="DI" /></td>
</tr>
<tr>
<td>Differential Output</td>
<td>DO</td>
<td><img src="image" alt="DO" /></td>
</tr>
<tr>
<td>Differential I/O</td>
<td>DIO</td>
<td><img src="image" alt="DIO" /></td>
</tr>
<tr>
<td>Differential Open_source</td>
<td>DOS</td>
<td><img src="image" alt="DOS" /></td>
</tr>
<tr>
<td>Differential Open_sink</td>
<td>DOD</td>
<td><img src="image" alt="DOD" /></td>
</tr>
<tr>
<td>Differential I/O_open_sink</td>
<td>DIOD</td>
<td><img src="image" alt="DIOD" /></td>
</tr>
<tr>
<td>Differential I/O_open_source</td>
<td>DIOS</td>
<td><img src="image" alt="DIOS" /></td>
</tr>
<tr>
<td>Differential 3-state</td>
<td>D3S</td>
<td><img src="image" alt="D3S" /></td>
</tr>
</tbody>
</table>
## Obsolete IBIS Model Parameters

Depending on the Model Type, IBIS Version 3.2 component will have some or all of the following parameters:

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Default</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ibis_file</td>
<td>IBIS file name</td>
<td>Auto select</td>
<td></td>
</tr>
<tr>
<td>Pin_name</td>
<td>Pin number of an IC</td>
<td>User selectable</td>
<td></td>
</tr>
<tr>
<td>IO_flag</td>
<td>Input/Output flag</td>
<td>0</td>
<td>User definable (1 or 0)</td>
</tr>
<tr>
<td>Polarity</td>
<td>Inverting/Non-inverting</td>
<td>Inverting</td>
<td>User selectable</td>
</tr>
<tr>
<td>Volt_range</td>
<td>Voltage Range</td>
<td>Typical</td>
<td>User selectable</td>
</tr>
<tr>
<td>Pullup</td>
<td>Pull-up driver</td>
<td>Typical</td>
<td>User selectable</td>
</tr>
<tr>
<td>Pulldown</td>
<td>Pull-down driver</td>
<td>Typical</td>
<td>User selectable</td>
</tr>
<tr>
<td>Groundclamp</td>
<td>Ground Clamp diode</td>
<td>Typical</td>
<td>User selectable</td>
</tr>
<tr>
<td>Vrise</td>
<td>Slew rate of Rising Edge Waveform</td>
<td>Typical</td>
<td>User selectable</td>
</tr>
<tr>
<td>Vfall</td>
<td>Slew rate of Falling Edge Waveform</td>
<td>Typical</td>
<td>User selectable</td>
</tr>
<tr>
<td>R_pkg</td>
<td>Pin Package Resistance</td>
<td>Typical</td>
<td>User selectable</td>
</tr>
<tr>
<td>L_pkg</td>
<td>Pin Package Inductance</td>
<td>Typical</td>
<td>User selectable</td>
</tr>
<tr>
<td>C_pkg</td>
<td>Pin Package Capacitance</td>
<td>Typical</td>
<td>User selectable</td>
</tr>
<tr>
<td>C_comp</td>
<td>Chip-to-Mounting substrate pin capacitance</td>
<td>Typical</td>
<td>User selectable</td>
</tr>
<tr>
<td>R_pin</td>
<td>Pin Parasitic Resistance</td>
<td>Auto Select</td>
<td></td>
</tr>
<tr>
<td>L_pin</td>
<td>Pin Parasitic Inductance</td>
<td>Auto Select</td>
<td></td>
</tr>
<tr>
<td>C_pin</td>
<td>Pin Parasitic Capacitance</td>
<td>Auto Select</td>
<td></td>
</tr>
</tbody>
</table>
The parameters listed below have three different characteristic values (typical, minimum and maximum) and can be selected by the user to represent a typical, fast, or slow device.

- **Pull-up** specifies the selection of I-V curve for pull-up driver.
- **Pull-down** specifies the selection of I-V curve for the pull-down driver.
- **Power_clamp** specifies the selection of I-V curve for the power supply clamping diodes.

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Default</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_comp</td>
<td>Chip-to-Mounting Substrate capacitance</td>
<td>Auto Select</td>
<td></td>
</tr>
<tr>
<td>Model_file</td>
<td>.mdif file associated with the pin</td>
<td>Auto Select</td>
<td></td>
</tr>
<tr>
<td>Voltage_range</td>
<td>Voltage range associated with the pin</td>
<td>Auto Select</td>
<td></td>
</tr>
<tr>
<td>V_fixture1</td>
<td>Fixture voltage 1</td>
<td>Auto Select</td>
<td></td>
</tr>
<tr>
<td>R_fixture1</td>
<td>Fixture resistance</td>
<td>Auto Select</td>
<td></td>
</tr>
<tr>
<td>V_fixture2</td>
<td>Fixture voltage 2</td>
<td>Auto Select</td>
<td></td>
</tr>
<tr>
<td>R_fixture2</td>
<td>Fixture resistance 2</td>
<td>Auto Select</td>
<td></td>
</tr>
<tr>
<td>VTtype</td>
<td>No of VT tables associated with the pin model</td>
<td>Auto Select</td>
<td></td>
</tr>
<tr>
<td>Scaling_coeff</td>
<td>Scaling coefficient used to model current through pull-up and pull-down device when only one VT table is present</td>
<td>User definable</td>
<td></td>
</tr>
<tr>
<td>Ioflag</td>
<td>Input/Output switch flag (Input=1, Output=0)</td>
<td>User selectable</td>
<td></td>
</tr>
<tr>
<td>Enable</td>
<td>Output Enable Switch Flag (Enable=1, Disabled=0)</td>
<td>User selectable</td>
<td></td>
</tr>
</tbody>
</table>

The parameters have different selection criteria.

- **P.1**: Pull-up
- **P.0**: Pull-down
- **P.2**: Power_clamp
- **Auto Select**
• Gnd_clamp specifies the selection of I-V curve for the ground clamping diode.
• Vrise specifies the selection of Vt curves for the rising edge.
• Vfall specifies the selection of Vt curves for the falling edge.
• Volt_range specifies the selection of bias voltage or power supply voltage.

The parameters listed below specify average pin package parasitic. They have three characteristic values—typical, minimum and maximum. The default is typical. In general, these parameters should all be set to the same value. The actual numeric values to which the characteristic values correspond are defined in the .ibs file. If individual pin parasitic values of R_pin, L_pin and C_pin are available, the values R_pkg, L_pkg and C_pkg are ignored and R_pin, L_pin, and C_pin are automatically chosen.
• R_pkg specifies pin parasitic resistance
• L_pkg specifies pin parasitic inductance
• C_pkg specifies pin parasitic capacitance
• Ccomp specifies the die capacitance

Parameter Settings for a Typical Device

To select a typical device, select the following combination of parameters:

Volt_range = Typical
Pullup = Typical
Pulldown = Typical
Powerclamp = Typical
Groundclamp = Typical
Vrise = Typical
Parameter Settings for a Fast Device
To select a fast device, select the following combination of parameters:
Volt_range = Maximum
Pullup = Maximum
Pulldown = Maximum
Powerclamp = Maximum
Groundclamp = Maximum
Vrise = Maximum
Vfall = Maximum
R_pkg = Minimum
L_pkg = Minimum
C_pkg = Minimum
Ccomp = Minimum

Parameter Settings for a Slow Device
To select a slow device, select the following combination of parameters:
Volt_range = Minimum
Pullup – Minimum
Pulldown – Minimum
Powerclamp – Minimum
Groundclamp – Minimum
Vtrise – Minimum
Vfall – Minimum
R_pkg – Maximum
L_pkg – Maximum
C_pkg – Maximum
Ccomp – Maximum
Buffer Components

Ideal Buffer, 1 to 2

Symbol

Available in ADS

Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Units</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>Impedance</td>
<td>Buffer impedance</td>
<td>Ohm</td>
<td>50</td>
</tr>
<tr>
<td>Signal_1_delay</td>
<td>Delay of Signal 1</td>
<td>sec</td>
<td>0</td>
</tr>
<tr>
<td>Signal_2_delay</td>
<td>Delay of Signal 2</td>
<td>sec</td>
<td>0</td>
</tr>
</tbody>
</table>

Notes/Equations

1. The buffer splits the input to two output ports and may be used to increase the number of inputs available from the pulse and step meter simulation component, or to split other sources.
2. Delay may be added to each output signal.
3. The port impedance is used to match the port impedance to the signal source.
Ideal Buffer, 1 to 4

Symbol

Available in ADS

### Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Units</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>Impedance</td>
<td>Buffer impedance;</td>
<td>Ohm</td>
<td>50</td>
</tr>
<tr>
<td>Signal_1_delay</td>
<td>Delay of Signal 1</td>
<td>sec</td>
<td>0</td>
</tr>
<tr>
<td>Signal_2_delay</td>
<td>Delay of Signal 2</td>
<td>sec</td>
<td>0</td>
</tr>
<tr>
<td>Signal_3_delay</td>
<td>Delay of Signal 3</td>
<td>sec</td>
<td>0</td>
</tr>
<tr>
<td>Signal_4_delay</td>
<td>Delay of Signal 4</td>
<td>sec</td>
<td>0</td>
</tr>
</tbody>
</table>

Notes/Equations

1. The buffer splits the input to four output ports and may be used to increase the number of inputs available from time domain sources.
2. Delay may be added to each output signal.
3. The port impedance is used to match the port impedance of the signal source.
Ideal Buffer, 1 to 8

Symbol

Available in ADS

Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Units</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>Impedance</td>
<td>Buffer Impedance</td>
<td>Ohm</td>
<td>50</td>
</tr>
<tr>
<td>Signal_1_delay</td>
<td>Delay of Signal 1</td>
<td>sec</td>
<td>0</td>
</tr>
<tr>
<td>Signal_2_delay</td>
<td>Delay of Signal 2</td>
<td>sec</td>
<td>0</td>
</tr>
<tr>
<td>Signal_3_delay</td>
<td>Delay of Signal 3</td>
<td>sec</td>
<td>0</td>
</tr>
<tr>
<td>Signal_4_delay</td>
<td>Delay of Signal 4</td>
<td>sec</td>
<td>0</td>
</tr>
<tr>
<td>Signal_5_delay</td>
<td>Delay of Signal 5</td>
<td>sec</td>
<td>0</td>
</tr>
<tr>
<td>Signal_6_delay</td>
<td>Delay of Signal 6</td>
<td>sec</td>
<td>0</td>
</tr>
<tr>
<td>Signal_7_delay</td>
<td>Delay of Signal 7</td>
<td>sec</td>
<td>0</td>
</tr>
<tr>
<td>Signal_8_delay</td>
<td>Delay of Signal 8</td>
<td>sec</td>
<td>0</td>
</tr>
</tbody>
</table>
Notes/ Equations
1. The buffer splits the input to eight output ports and may be used to increase the number of inputs available from time domain sources.
2. Delay may be added to each output signal.
3. The port impedance is used to match the port impedance to the signal source.
Impedance Meter

Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Units</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>clock_period</td>
<td>Clock Period</td>
<td>sec</td>
<td>1e-9</td>
</tr>
<tr>
<td>rise_time</td>
<td>Pulse Rise Time</td>
<td>sec</td>
<td>1e-9</td>
</tr>
</tbody>
</table>

Notes/Equations

1. Use the impedance meter to calculate transmission line impedance.

2. See the example DesignGuides > IBIS Library > Examples > Impedance Simulation for an example using the impedance meter component.
Impedance Optimizer

Symbol

Available in ADS

Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Units</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>desired_impedance</td>
<td>Desired Impedance of Transmission Line</td>
<td>Ohm</td>
<td>50</td>
</tr>
<tr>
<td>clock_period</td>
<td>Clock Period</td>
<td>sec</td>
<td>1e-9</td>
</tr>
<tr>
<td>rise_time</td>
<td>Pulse Rise Time</td>
<td>sec</td>
<td>1.1e-9</td>
</tr>
</tbody>
</table>

Notes/ Equations

1. Use the impedance optimizer to determine transmission line characteristic, given the desired line impedance.

2. See the example DesignGuides > IBIS Library > Examples > Impedance Optimization for an example using the impedance optimizer component.
Octal Load

Available in ADS

Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Units</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rload</td>
<td>Load impedance</td>
<td>Ohm</td>
<td>1e6</td>
</tr>
<tr>
<td>Cload</td>
<td>Load capacitance</td>
<td>F</td>
<td>20e-12</td>
</tr>
</tbody>
</table>

Notes/Equations

1. The octal load provides a convenient method of inserting a load to multilayer lines and components.
2. In addition to load impedance, you can specify capacitance to ground.
3. All eight loads have the same value.
Octal Load without Ground

Symbol

Available in ADS

Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Units</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rload</td>
<td>Load impedance</td>
<td>Ohm</td>
<td>1e6</td>
</tr>
<tr>
<td>Cload</td>
<td>Load capacitance</td>
<td>F</td>
<td>20e-12</td>
</tr>
</tbody>
</table>

Notes/ Equations

1. The octal load provides a convenient method of inserting a load to multilayer lines and components.
2. The load can be terminated to points other than ground.
3. All eight loads have the same value.
4. Pin 9 is the termination pin for the resistive load.
5. Pin 10 terminates the capacitive load.
Octal Pulse Generator

Symbol

Available in ADS

Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Units</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vlow</td>
<td>Minimum Source Amplitude</td>
<td>V</td>
<td>0</td>
</tr>
<tr>
<td>Vhigh</td>
<td>Maximum Source Amplitude</td>
<td>V</td>
<td>5</td>
</tr>
<tr>
<td>Rsource</td>
<td>Source Impedance</td>
<td>Ohm</td>
<td>50</td>
</tr>
<tr>
<td>Tdelay</td>
<td>Time Delay</td>
<td>sec</td>
<td>0</td>
</tr>
<tr>
<td>Trise</td>
<td>Pulse Rise Time</td>
<td>sec</td>
<td>0</td>
</tr>
<tr>
<td>Tfall</td>
<td>Pulse Fall Time</td>
<td>sec</td>
<td>0</td>
</tr>
<tr>
<td>Width</td>
<td>Pulse Width</td>
<td>sec</td>
<td>3e-9</td>
</tr>
<tr>
<td>Period</td>
<td>Pulse Period</td>
<td>sec</td>
<td>10e-9</td>
</tr>
</tbody>
</table>
The octal pulse generator provides a convenient method of connecting multiple sources to multilayer lines and components. It is based on the time domain pulses voltage source, VTPulse. All the eight sources share the same parameter settings.
Oscilloscope Probe

Symbol

Available in ADS

Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Units</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>Probe Resistance</td>
<td>MΩ</td>
<td>1</td>
</tr>
<tr>
<td>C</td>
<td>Probe Capacitance</td>
<td>pF</td>
<td>10</td>
</tr>
</tbody>
</table>

Notes/Equations

1. Use the probe to collect voltage data at the inserted point.
2. The data will be stored in the oscilloscope_probe component name.
3. The probe may be used in conjunction with time domain simulation.
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