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PLL Design Guide

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Chapter 1: PLL QuickStart Guide

This PLL QuickStart Guide is intended to help you get started using the Phase-Locked Loop Design Guide effectively. For detailed reference information, refer to Chapter 2, PLL DesignGuide Reference.

The PLL DesignGuide has many simulation setups and data displays that are very useful for designing a phase-locked loop. The simulation set-ups are categorized by the PLL configuration, simulation technique, and type of phase detector and low-pass filter. The simulation set-ups are for analysis.

**Note** This DesignGuide is not a complete solution for all phase-locked loop techniques, but covers the most common approaches. Subsequent releases of this DesignGuide will include an expanded range of features.
Using the Phase-Locked Loop DesignGuide

The features and content of the PLL DesignGuide are accessible from the DesignGuide menu found in the ADS Schematic window.
Using a dialog box of Phase-Locked Loop schematics, you select your desired PLL configuration, as shown here.

You select one of the available PLL configurations shown.
Having identified the type of PLL structure, you then select one of the three simulations available from the Simulation tab, as shown here. The simulations include:

- Closed and Open Loop frequency response
- Phase Noise response
- Transient response
You then need to identify the phase detector and low-pass filter used in your design. Some combinations are unavailable at this time but are expected to be available in future upgrades.

The selection box for phase detectors is shown here.
Shown here is the selection box for loop filters. The grayed-out selections are not available at this time. Right-click one of the available selections. For a detailed description of the loop filter selections, refer to the Chapter 2, PLL Design Guide Reference.
Selecting Appropriate Configurations

The Phase-Locked Loop DesignGuide is broken up into different sub-categories, as shown in the previous section. The specifications that you select depend on your desired simulation and the type of PLL structure that your system can utilize.

If, for example, you are designing a synthesizer, you can start with the loop frequency response configurations shown in the section “Phase Margin and Unity Gain Bandwidth” on page 1-8. The output parameters will be used for evaluating the phase noise and transient responses.

Most of the information on the data display for this design simulation and others is in a format that engineers can easily understand. The visibility of equation syntaxes is minimized. Information about items on a data display that you will want to modify is enclosed in red boxes.
Phase Margin and Unity Gain Bandwidth

The optimization procedure based on achieving a desired Phase margin and Unity Gain Bandwidth is shown here. Enter your desired values, as well as your VCO tuning parameter, the divide ratio, and the Phase Detector characteristics. (Enter this data in the area of the schematic encircled in this illustration.)
In the data display results shown here, the resultant Phase Margin and Unity Gain Frequency are displayed, along with the optimized loop filter parameters. If the objectives have not been met, you should adjust the loop filter parameters to alter the initial conditions of the optimization and re-run the simulation.

<table>
<thead>
<tr>
<th>UnityGainFreq</th>
<th>12.59k</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase_Margin_at_UgainFreq</td>
<td>45.336</td>
</tr>
</tbody>
</table>
Phase Noise Response

The parameters derived from the Loop Frequency Response schematic should be entered into the Phase Noise Response schematic.

The phase noise characteristics of each component should be set on each subcircuit block. The F and L parameters that describe the noise versus frequency characteristics are depicted in the schematic.
The data display corresponding to the Phase Noise schematic is shown here.

The graph on the left displays the individual noise source's contributions and the graph on the right shows the overall noise performance of the PLL.
Transient Time Response

Shown here is the schematic for evaluating the transient time response of a synthesizer. The loop filter parameters derived from the Loop Frequency response need to be entered into this schematic, along with the VCO and Phase Detector constants. The transient response requires additional parameters such as the Reference Frequency and the stop and delay time, as well as the Divider Ratio step change.
The Transient response data display has a number of figures that will describe the PLL performance as a function of time. From this display, you can evaluate the settling time and use the results to debug the phase-locked loop.
Chapter 2: PLL DesignGuide Reference

Using the PLL DesignGuide

The Phase-Locked Loop (PLL) DesignGuide is integrated into Agilent EEsof’s Advanced Design System environment, working as an interactive handbook for the creation of useful designs. The Guide contains many templates to be used in the ADS software environment. These templates can assist the PLL developer in designing a phase-locked loop to meet performance specifications. You can use the optimization templates to define the loop performance, then proceed to evaluate the phase noise response and transient response. The DesignGuide provides a complete tool kit to interactively explore dynamic PLL systems at the top level as part of an integrated design process.

In addition to the requirements of the ADS HP EEsof software, the PLL DesignGuide requires approximately 5 MB of additional storage space.

**Note** This manual assumes that you are familiar with all of the basic ADS program operations. For additional information, refer to the ADS User’s Guide.

The primary features of the PLL DesignGuide are:

- Complete PLL synthesis capability
- Frequency synthesizer design
- Phase modulator design
- Frequency modulator design
- Phase demodulator design
- Frequency demodulator design
- Open and closed loop frequency response
- Phase noise simulation
- Time domain transient simulation
- Four distinct phase detectors
- Seven loop filter configurations
PLL Configurations

Following are diagrams and basic descriptions of the PLL configurations included in this DesignGuide. To access these tools, select DesignGuide > PLL DesignGuide > Select PLL Configuration from the ADS Schematic window, and make appropriate selections in the tabs of the dialog box.

Frequency Synthesizer (SYN)

A block diagram of the basic phase-locked synthesizer is shown in Figure 2-1.

The voltage controlled oscillator frequency is divided by $N$ and then compared in a phase detector with the reference oscillator. The accuracy and long-term stability of the output frequency are controlled by the reference oscillator. The short-term stability is $N$ times the reference inside the loop bandwidth and that of the VCO outside of the loop bandwidth. This allows a means of generating several highly accurate output frequencies. Frequency selection is performed by changing the divider ratio $N$. 
**Frequency Modulator (FMD)**

Frequency modulation of the phase-locked loop is produced by adding a baseband voltage into the VCO tuning terminal along with the output of the loop filter, as shown in Figure 2-2.

The loop bandwidth must be smaller than the smallest modulation frequency to avoid linear distortion. The VCO characteristics must be linear to avoid nonlinear distortion of the modulation.
**Frequency Demodulator (FDM)**

The frequency modulated reference signal is applied to the PLL. For the loop to remain in lock, the VCO frequency must track the incoming frequency, as shown in Figure 2-3.

![Frequency Demodulator Diagram](image)

**Figure 2-3. Frequency Demodulator**

The frequency of the VCO is proportional to the tuning voltage. Therefore, the tuning voltage must be a close replica of the modulation of the signal. The recovered signal is equivalent to the original signal filtered by the closed loop transfer function of the PLL. To avoid distortion, the VCO control characteristics must be linear and the loop bandwidth must be large compared to the input modulation.
Phase Modulator (PMD)

Phase modulation of the phase-locked loop is produced by adding a baseband voltage into the VCO tuning terminal along with the output of the loop filter, as shown in Figure 2-4.

Another alternative is to add the phase modulator input before the loop filter, thereby, eliminating the need for the differentiator. The loop bandwidth must be smaller than the smallest modulation frequency to avoid linear distortion. The VCO and phase detector characteristics must be linear to avoid nonlinear distortion of the modulation. Phase modulation of the phase-locked loop is produced by adding a baseband voltage into the VCO tuning terminal along with the output of the loop filter. Another alternative is to add the phase modulator input before the loop filter, thereby eliminating the need for the differentiator. The loop bandwidth must be smaller than the smallest modulation frequency to avoid linear distortion. The VCO and phase detector characteristics must be linear to avoid nonlinear distortion of the modulation.
Phase Demodulator (PDM)

The frequency modulated reference signal is applied to the PLL. For the loop to remain in lock, the VCO frequency must track the incoming frequency, as shown in Figure 2-5.

The frequency of the VCO is proportional to the tuning voltage. Therefore, the integral of the tuning voltage must be a close replica of the phase modulation of the signal. The recovered signal is equivalent to the derivative of the original frequency modulated signal after it has been filtered by the closed loop transfer function of the PLL. To avoid distortion, the VCO control characteristics must be linear and the loop bandwidth must be large compared to the input modulation.
Phase Detectors
This section provides detailed information on the phase detectors used in the PLL DesignGuide.

Detector Types
- Phase/Frequency Detector
- Charge Pumped Detector
- Mixer
- Exclusive OR

Phase/Frequency Detector
The digital behaviour is modelled as a common D flip-flop. Phase correction is provided by pulse width modulation of the output.

\[ |K_d| = \frac{\log_2(1) - \log_2(0)}{2\pi} \cdots \left(\frac{V}{\text{radian}}\right) \]  \hspace{1cm} (2-1)

Charge Pumped Detector
The charge pumped detector is identical to the Phase/Frequency detector except that the output is a single-ended current source.

\[ K_d = \frac{I_d}{2\pi} \cdots \left(\frac{\text{Amps}}{\text{radian}}\right) \]  \hspace{1cm} (2-2)

Mixer
Mixers having wide bandwidths of operation but also have a limited locking range and therefore tend to require help during start-up.

\[ K_d = \text{MixerGain} \cdots \left(\frac{V}{V}\right) \]  \hspace{1cm} (2-3)
Exclusive OR

An exclusive OR consists of basic logic components. When combined, they obey the Truth Table shown here. They provide only phase-error information.

\[
K_d = \frac{\text{Logic}_1 - \text{Logic}_0}{\pi/2} \text{ radian}
\]  

(2-4)

<table>
<thead>
<tr>
<th>Input #1</th>
<th>Input #2</th>
<th>Output #1</th>
<th>Output #2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 2-1.
Reference

This section provides some useful reference information on the use of the PLL DesignGuide.

Template Reference Guide

To access the templates listed here, select DesignGuide > PLL DesignGuide > Select PLL Configuration from the ADS Schematic window, and make appropriate selections in the tabs of the dialog box.

Circuit Types
SYN (Synthesizer)
FMD (Frequency Modulator)
PMD (Phase Modulator)
PDM (Phase Demodulator)
FDM (Frequency Demodulator)

Simulations
FQ (Loop Frequency Response)
PN (Phase Noise Response)
TN (Transient Time Domain Response)

Phase Detectors
PF (Phase/Frequency)
CP (Charge Pump)
MX (Mixer)
XR (Exclusive OR)

Loop Filters
P3P (Passive 3-pole PLL integrator)
P4P (Passive 4-pole PLL integrator)
PLL DesignGuide Reference

A2P (Active 2-pole PLL integrator)
A2PLG (Active 2-pole PLL integrator for Low Gain Opamps)
A3P (Active 3-pole PLL integrator)
A3PPF (Active 3-pole PLL integrator with passive pre-filtering)
A4PPF (Active 4-pole PLL integrator with passive pre-filtering)

Possible Template Configurations
Following are two possible template configurations. The sections that follow provide more detailed template examples.

SYN_CP_FQ_P4P
Closed and Open Loop Response of Frequency Synthesizer with charge pump detector and using a 4-pole passive PLL integrator.

PMD_PF_TN_A3PPF
Transient Response of a Phase Modulator with a Phase/Frequency Detector using an active 3-pole PLL integrator with a pre-filter.
Template Example: SYN_CP_FQ_A3P

This example is of a phase-locked loop frequency synthesizer that uses a charge-pumped phase detector and has an active 3-pole PLL integrator. The template SYN_CP_FQ_A3P identifies the fact that we are interested in the closed- and open-loop frequency response. This template also contains an optimization for determining the best resistor and capacitor values in the integrator based on the desired loop bandwidth and phase margin. There are three distinct circuits in this template:

- Closed Loop Response
- Open Loop Response
- Loop Filter Response

Active 3-Pole Integrator

The active 3-pole PLL integrator is a second-order filter. This combines with the VCO's pole to create a 3-pole PLL. The loop bandwidth must be significantly lower than the reference frequency to ensure proper sideband suppression. The loop filter consists of two capacitors (Clpf1 and Clpf2) as well as a resistor (Rlpf1). The operational amplifier used has ideal characteristics.

PLL Input Parameters

You need to identify various parameters before simulating. The VCO gain constant or tuning sensitivity parameter is identified as Kv (MHz/volt). The-charge pumped phase detector uses current Id (amps). The divider ratio N0 is the ratio between the VCO center frequency and the reference frequency. The other parameters are the Loop filter component values. The filter parameters are optimized from an initial guess value.

Optimization Parameters

The optimization criteria are the desired PLL loop filter bandwidth and the corresponding phase margin. The goals of the optimization process are to vary the loop filter component values until the loop filter bandwidth and the phase margin are within the error bounds specified in the Goal item. The frequency range and number of data points for the simulation are set in AC. The type of optimization and considerations are identified in the Nominal Optimization item. The measurement equations assist in the collection and plotting of the data results.
Closed Loop Response

The closed loop frequency response is simulated based on the optimized loop filter component values.

Simulation Results

The initial guess values of the loop filter components can be altered if the optimization results do not meet the desired design constraints. Once the Simulate button is chosen, the optimizer begins to adjust the loop filter components to obtain the desired loop filter bandwidth and phase margin. The New Data Display Window button corresponding to the design schematic is then chosen. Open the data set corresponding to the template name. In this example, open SYN_CP_FQ_A3P.dds. The Optimized filter bandwidth and Phase Margin are identified, as well as the corresponding loop filter component values. The plots of the open and closed loop frequency responses are displayed.
Template Example: SYN_CP_PN_A3P

This example is of a phase-locked loop frequency synthesizer that uses a charge pumped phase detector and has an active 3-pole PLL integrator. The template SYN_CP_PN_A3P identifies the fact that we are interested in the phase noise response. The optimized loop filter parameters generated from the frequency response template SYN_CP_FQ_A3P can be used in this template. The PLL parameters and the desired AC frequency sweep range need to be specified. The opamp noise characteristics can be altered to reflect your opamp.

PLL Parameters

The PLL parameters consist of the VCO tuning sensitivity Kv (MHz/volt), phase detector current Id (amps), inner loop frequency divider N0, reference frequency divider N0ref (if applicable), and the loop filter components.

Simulation Frequency Sweep

The sweep range of the AC simulator is set by the start and stop frequency, as well as the grid on the logarithmic plot.

Phase Noise Characteristics

In modeling the phase noise of the various phase-locked loop components, three distinct frequencies (F3,F2,F1) are defined at which the phase noise characteristics exhibit single sideband slopes of (-30,-20,-10 dBc/Hz), respectively. These frequencies (F3,F2,F1) correspond to the phase noise values of (L3,L2,L1), respectively. L0 defines the broadband noise floor.

Simulation Results

The Simulate button is then chosen and once the simulation is complete, the New Data Display Window button corresponding to the design schematic is chosen. The data set corresponds to the template name. In this example, open SYN_CP_PN_A3P.dds. The plot on the left depicts the phase noise contribution versus frequency of the various components of the PLL in the locked state. The plot on the right shows the overall PLL phase noise performance, where we expect to see system phase noise characteristics to track the reference oscillator inside the loop bandwidth, then track the phase noise of the VCO outside the loop bandwidth. The table demonstrates the PLL phase noise at different frequencies.
Template Example: SYN_CP_TN_A3P

This example is of a phase-locked loop frequency synthesizer that uses a charge-pumped phase detector and has an active 3-pole PLL integrator. The template SYN_CP_TN_A3P identifies the fact that we are interested in the transient time domain response. The optimized loop filter parameters generated from the frequency response template SYN_CP_FQ_A3P can be used in this template. The PLL parameters need to be set up. An Envelope Simulation is performed, where the fundamental frequency is that of the reference oscillator.

PLL Parameters

The PLL parameters consist of the individual loop filter component resistor and capacitor values. These values are typically derived from the optimized frequency response simulation template. In addition, the parasitic capacitance \( C_{vco} \) and resistance \( R_{vco} \) can be included in the transient simulation. The PLL parameters are specified VCO tuning sensitivity \( K_v \), initial divider ratio \( N_0 \), reference frequency \( F_{ref} \), and charge pump maximum current \( I_d \). The transient parameters are then specified: the loop divider step change \( N_{\text{Step}} \), the delay time before the step occurs \( \text{Delay Time} \), the step time of the simulation \( \text{Step Time} \), and the stop time of the simulation \( \text{Stop Time} \). The delay time is used to allow the simulation conditions to stabilize before the divider step change occurs. The step time refers to the resolution accuracy of the simulation. The stop time identifies the length of time the simulation results progress, this time should be long enough to observe the step change stabilizing. The initial divider ratio \( N_0 \) needs to be entered in two places: the variable equation and the measurement equation.

Simulation Schematic

The individual components of the PLL transient simulation are identified. Note that the reference oscillator is a sawtooth waveform, allowing for better accuracy in the phase detector.

Simulation Results

The Simulate button is then chosen. Upon completion of the simulation, the New Data Display Window button corresponding to the design schematic is chosen. The data set corresponding to the template name. In this example, open SYN_CP_TN_A3P.dds. The upper left plot depicts the tuning voltage that controls the VCO. The corresponding VCO frequency tracks the tuning voltage in the lower
left plot. The upper right plot shows the charge pump current as a function of time. The lower right plot is the step function for the divider ratio.

**Parameter Definitions**

[UnityGainFreq] Loop Bandwidth: Loop bandwidth in Hertz. The loop bandwidth is the frequency at which the PLL's open loop gain equals unity (0 dB).

[Min_Phase_Margin] Phase Margin: Loop phase margin in degrees. The phase margin is equal to 180 degrees minus the open loop phase at the loop bandwidth frequency.

[Clpf1] Capacitor #1: First loop filter capacitor.

[Clpf2] Capacitor #2: Second loop filter capacitor.

[Clpf3] Capacitor #3: Third loop filter capacitor.

[Rlpf1] Resistor #1: First loop filter resistor.

[Rlpf2] Resistor #2: Second loop filter resistor.

[Rlpf3] Resistor #3: Third loop filter resistor.

[C_vco] Parasitic VCO Capacitor: VCO tuning line can be modelled as having a shunt capacitor.

[R_vco] Parasitic VCO Resistor: VCO tuning line can be modelled as having a series resistance.

[BStopN] Bandstop Filter Order: The bandstop filter is used to reduce the reference sideband level. This filter can significantly alter the loop performance. The phase margin can be degraded, which will introduce instability to the loop.

(Id) Charge Pumped Phase Detector: Maximum output current for the charge pump detector.


[Logic0] Phase Frequency Detector Lower Voltage: Lower logic level in the digital circuit.

[Mixer_Gain] Mixer voltage gain: Forward gain of the mixer. Typically it is set to 1 for a passive ring diode mixer.

[N0] PLL loop divider: Divider value in the loop.

[N0ref] Reference oscillator divider: Divider value for the reference oscillator.
PLL Design Guide Reference

[N_Step] PLL loop divider step change: Sstep change in the divider value of the loop.

[Kv] VCO tuning sensitivity in MHz/volt: The VCO tuning sensitivity is assumed to be linear across the tuning bandwidth.

[freq] frequency: Generic name for the simulation frequency.

[timestep] time step: Generic name for the simulation time steps.

[Freq_0] initial VCO frequency: Defines the initial VCO frequency before the divider step function is applied.

[Fref] reference oscillator frequency: Defines the reference oscillator frequency.

[K0] VCO tuning sensitivity (MHz/volt): The VCO tuning sensitivity is assumed to be linear across the tuning bandwidth. This value is used in the transient simulation.

[Step_Time] transient sampling period: The transient simulation time step controls the accuracy of the simulation.

[Stop_Time] transient stop time: The transient simulation stop time sets the duration of the simulation.

[Delay_Time] transient delay time: The transient simulation delay time determines the start of the change in the divider ratio value.

[Switch_Time] transient switch time: The transient simulation switch time determines the rate of change of the modulation.

[Vp_dev] modulation voltage (volts): The PLL is modulated by this peak-to-peak voltage in the transient simulation.

[Rout_mod] modulator output resistance (kohms): The PLL is modulated by a source with this output resistance.

[N_Step] divider step change: The transient simulation divider ratio is changed by this value.

[L0] broadband phase noise parameter: The component broadband phase noise is set by this value.

[F1] frequency #1 phase noise parameter: The component frequency corresponding to the phase noise L1 is set by this value.

[L1] phase noise #1: The component phase noise corresponding to the frequency F1 is set by this value.
[F2] frequency #2 phase noise parameter: The component frequency corresponding to the phase noise L2 is set by this value.

[L2] phase noise #2: The component phase noise corresponding to the frequency F2 is set by this value.

[F3] frequency #3 phase noise parameter: The component frequency corresponding to the phase noise L3 is set by this value.

[L3] phase noise #3: The component phase noise corresponding to the frequency F3 is set by this value.

[F4] frequency #4 phase noise parameter: The component frequency corresponding to the phase noise L4 is set by this value.

[L4] phase noise #4: The component phase noise corresponding to the frequency F4 is set by this value.

[in0] spectral noise current parameter #0 of opamp (amps/sqrt(Hz)): Defines one of the noise current parameters that model the opamp characteristics.

[vn0] spectral noise voltage parameter #0 of opamp (Volts/sqrt(Hz)): Defines one of the noise voltage parameters that model the opamp characteristics.

[in1] spectral noise current parameter #1 of opamp (amps/sqrt(Hz)): Defines one of the noise current parameters that model the opamp characteristics.

[vn1] spectral noise voltage parameter #1 of opamp (Volts/sqrt(Hz)): Defines one of the noise voltage parameters that model the opamp characteristics.

[fvn1] spectral noise frequency corresponding to vn1: Defines one of the noise voltage parameters that model the opamp characteristics.

[fin1] spectral noise frequency corresponding to in1: Defines one of the noise current parameters that model the opamp characteristics.

[Filt_out] loop filter frequency response: Loop filter frequency response output value.

[Vout_OL] open loop frequency response: Open loop frequency response output value.

[Vout] closed loop frequency response: Closed loop frequency response output value.


PLL DesignGuide Reference

**[VCOout]** overall phase noise of PLL: The overall noise voltage generated by the PLL.

**[phi_rms]** vco phase noise: The phase noise contributed by the VCO.

**[refv]** reference oscillator: The reference oscillator is modelled as a sawtooth waveform.

**[VCO_FR]** output at vco frequency: Output of the PLL at the VCO frequency.

**[N0output]** divider ratio function: Step function that describes the divider ratio defines this value.

**[vtune]** tuning voltage: Control voltage that drives the VCO defines this value.

**[VCO_freq_MHz]** VCO frequency (MHz): VCO output frequency.

**[ChargePumpI]** charge pump current (amps): The charge pump current defines this value.

**[DivideRatioN]** frequency divider ratio: Frequency divider ratio.

**[Vcon]** VCO divided output: VCO output after it has passes through the frequency divider.

**[Vref]** reference voltage: The reference oscillator voltage defines this value.

**[V_U]** upper phase/ frequency detector: The upper phase/frequency detector output.

**[V_D]** lower phase/ frequency detector: The lower phase/frequency detector output.
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