TD-SCDMA DesignGuide

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Contents

1 TD-SCDMA Standard
   Introduction ............................................................................................................... 1-1
   Physical Layer .................................................................................................... 1-1
   DesignGuide Examples Overview ............................................................................ 1-3

2 TD-SCDMA BER Performance Designs
   Introduction ............................................................................................................... 2-1
   12.2k Uplink Channel with AWGN ................................................................. 2-2
   12.2k Uplink Fading Channel with Joint Detection Receiver ......................... 2-4
   12.2k Downlink Fading Channel ................................................................. 2-7

3 TD-SCDMA Instrument Link Designs
   Introduction ............................................................................................................... 3-1
   Base Station Signal Generated Using ADS-ESGc Link Measured by VSA89600.... 3-2
   User Equipment Signal Generated Using ADS-ESGc Link Measured by VSA89600 3-5

4 TD-SCDMA Power Amplifier Designs
   Introduction ............................................................................................................... 4-1
   Complementary Cumulative Distribution Function Measurements ................ 4-2
   Power vs. Time Measurement ............................................................................ 4-4
   CCDF and Spectrum Measurements of Multi-carrier Signal ......................... 4-6

5 TD-SCDMA Receiver Designs
   Introduction ............................................................................................................... 5-1
   Base Station Reference Sensitivity Level ............................................................. 5-2
   User Equipment Adjacent Channel Selectivity .................................................. 5-4

6 TD-SCDMA Signal Source Designs
   Introduction ............................................................................................................... 6-1
   Uplink Signal Characteristics ............................................................................ 6-2
   Adjacent Channel Power Leakage Ratio ........................................................... 6-6
   Rate Match Calculator ....................................................................................... 6-8

7 TD-SCDMA Transmitter Designs
   Introduction ............................................................................................................... 7-1
   Base Station Error Vector Magnitude ................................................................. 7-2
   User Equipment Code Domain Power ............................................................... 7-5

Index
Chapter 1: TD-SCDMA Standard

Introduction

TD-SCDMA is a Chinese contribution to the international family of Mobile Radio Systems for 3G services of UMTS and IMT 2000. It is now one option of UTRA-TDD, called 1.28Mcps TDD or low chip rate (LCR) TDD. It is an advanced CDMA/TDMA/TDD system with an adaptive synchronous operation.

TD-SCDMA system simulation models based on the 3GPP TDD LCR standard demonstrate signal generation capabilities; basic measurements are considered. TD-SCDMA aligns with the same version of the specification used by the Agilent ESG-C, PSA II and VSA.

Physical Layer

The frame structure, illustrated in Figure 1-1, recognizes new smart antenna and uplink synchronization technologies.

Figure 1-1. Physical Channel Signal Format

Uplink and downlink time slots in each frame are separated by a switching point. There are two switching points in each sub-frame: TS0 is always allocated as downlink; TS1 is always allocated as uplink. There are three special time slots:
TD-SCDMA Standard

- DwPTS: downlink pilot time slot, 96 chip duration
- UpPTS: uplink pilot time slot, 160 chip duration
- GP: main guard period for TDD operation, 96 chip duration

The system can operate on symmetric and asymmetric modes by properly configuring the number of downlink and uplink time slots.

The burst structure is illustrated in Figure 1-2.

![Figure 1-2. Burst Structure](image)

The transmitter structure of a physical channel is illustrated in Figure 1-3.

![Figure 1-3. Transmitter Structure](image)
There are two kinds of receiver algorithm for TD-SCDMA: Rake and Joint Detection.

Physical channels have a 3-layer structure.

- **Time slot**: 675 usec slot consisting of a number of Symbols. Time slots are used in a TDMA component to separate different user signals in time and code domain.
- **Radio frame**: 5 msec frame consisting of 7 time slots
- **System frame numbering**

**DesignGuide Examples Overview**

Example designs are provided in the `/examples/tdscdma` directory. Projects and their corresponding design examples are:

The TDSCDMA_BER project demonstrates BER and BLER performance.

- BER and BLER performance of a 12.2k uplink channel with AWGN: TDSCDMA_12_2_UL_AWGN.dsn
- BER and BLER performance of a 12.2k uplink reference fading channel with joint detection receiver: TDSCDMA_12_2_UL_Fading_J_D.dsn
TD-SCDMA Standard

• BER and BLER performance of a 12.2k downlink fading channel with joint detection receiver: TDSCDMA_12_2_DL_Fading_J_D.dsn

The TD-SCDMA_LinkTest project demonstrates the characteristics of ADS and instrument links.
• Base station signal generated using ADS-ESGc link measured by VSA89600: TDSCDMA_DL_Link.dsn.
• User equipment signal generated using ADS-ESGc link measured by VSA89600: TDSCDMA_UL_Link.dsn.

The TDSCDMA_PA_Test project includes these design examples.
• Characterization of peak average power ratio versus probability: TDSCDMA_DL_CCDF.dsn.
• Instant and average power versus time measurements: TDSCDMA_UL_Power_vs_Time.dsn.
• CCDF and spectrum of multi-carrier signal measurements: TDSCDMA_MC_Test.dsn.

The TDSCDMA_Rx project demonstrates user equipment and base station characteristics.
• BTS reference sensitivity level: TDSCDMA_UL_Sensitivity.dsn.
• UE adjacent channel selectivity: TDSCDMA_DL_AdjacentChannel.dsn.

The TDSCDMA_SignalSource project demonstrates the special transient characteristics of TD-SCDMA signals from time and frequency domains.
• Uplink signal characteristics: TDSCDMA_UL_Spectrum.dsn.
• Downlink signal characteristics: TDSCDMA_DL_ACLR.dsn.

The TDSCDMA_Tx project demonstrates user equipment and base station characteristics.
• Base station error vector magnitude: TDSCDMA_DL_EVM.dsn.
• User equipment code domain power: TDSCDMA_UL_CDP.dsn.
Chapter 2: TD-SCDMA BER Performance Designs

Introduction

The TDSCDMA_BER project demonstrates BER and BLER performance. Three example designs are included in this project:

• BER and BLER performance of a 12.2k uplink channel with AWGN: TDSCDMA_12_2_UL_AWGN.dsn

• BER and BLER performance of a 12.2k uplink reference fading channel with joint detection receiver: TDSCDMA_12_2_UL_Fading_JD.dsn

• BER and BLER performance of a 12.2k downlink fading channel with joint detection receiver: TDSCDMA_12_2_DL_Fading_JD.dsn
12.2k Uplink Channel with AWGN

TDSCDMA_12_2_UL_AWGN.dsn

Description

BER and BLER performance of a 12.2k uplink channel with AWGN is demonstrated in this design.

The top-level schematic for this design is shown in Figure 2-1.

- **TDSCDMA_RefCh_RF** is used to generate an uplink RF reference measurement channel. One physical channel is used to carry one DCH and one DCCH. The spreading factor is 8.

- A convolution encoder is used. The code rate is 1/3 and the constraint length is 7. A rate match component is placed after the encoder with a 1/3 puncture rate.

- A Rake receiver is applied.

Figure 2-1. TDSCDMA_12_2_UL_AWGN.dsn Schematic
Simulation Results

Simulation results are displayed in Figure 2-2.

![Graph](image)

**Figure 2-2. Simulation Results**

**Benchmark**
- Hardware Platform: Pentium 4 1.8GHz, 512 MB memory
- Software Platform: Windows XP, ADS 2003A
- Simulation Time: 20 hours

**References**

12.2k Uplink Fading Channel with Joint Detection Receiver

TDSCDMA_12_2_UL_Fading_JD.dsn

Description

BER and BLER performance of a 12.2k uplink reference fading channel with joint detection receiver is demonstrated in this design.

The top-level schematic for this design is shown in Figure 2-3.

- TDSCDMA_RefCh_RF is used to generate an uplink reference measurement channel. One DPCH is used to carry one DCH and one DCCH. The spreading factor is 8.
- A convolution encoder is used. The code rate is 1/3 and the constraint length is 7. A rate match component is placed after the encoder with a 1/3 puncture rate.
- Table 2-1 lists propagation conditions (defined in [1]) for multi-path fading environment performance measurements (Case 3 is applied in this design). All taps have classical Doppler spectrum.
Simulation Results

Simulation results are displayed in Figure 2-4.

Table 2-1. Propagation Conditions for Multi-Path Fading Environments

<table>
<thead>
<tr>
<th>Relative Delay (nsec)</th>
<th>Average Power (dB)</th>
<th>Relative Delay (nsec)</th>
<th>Average Power (dB)</th>
<th>Relative Delay (nsec)</th>
<th>Average Power (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2928</td>
<td>-10</td>
<td>2928</td>
<td>0</td>
<td>781</td>
<td>-3</td>
</tr>
<tr>
<td>1200</td>
<td>0</td>
<td>1563</td>
<td>-6</td>
<td>2344</td>
<td>-9</td>
</tr>
</tbody>
</table>

Benchmark

- Hardware Platform: Pentium 4 2.3GHz, 512 MB memory
- Software Platform: Windows 2000, ADS 2003C
TD-SCDMA BER Performance Designs

- Simulation Time: 60 hours

References

12.2k Downlink Fading Channel

TDSCDMA_12_2_DL_Fading_JD.dsn

Description

BER and BLER performance of a 12.2k downlink fading channel with joint detection receiver is demonstrated in this design.

The top-level schematic for this design is shown in Figure 2-5.

Figure 2-5. TDSCDMA_12_2_DL_Fading_JD.dsn Schematic

- **TDSCDMA_RefCh_RF** is used to generate a downlink reference measurement channel. Two DPCHs carry one DCH and one DCCH. The spreading factor is 16.

- A convolution encoder is used. The code rate is 1/3 and the constrain length is 7. A rate matching component is placed after the encoder with a 1/3 puncture rate.

- A joint detection receiver is applied.

- **Table 2-2** lists propagation conditions (defined in [1]) for multi-path fading environment performance measurements (Case 3 is applied in this design).
TD-SCDMA BER Performance Designs

Table 2-2. Propagation Conditions for Multi-Path Fading Environments

<table>
<thead>
<tr>
<th>Case 1, 3 km/hr</th>
<th>Case 2, 3 km/hr</th>
<th>Case 3, 120 km/hr</th>
</tr>
</thead>
<tbody>
<tr>
<td>Relative Delay (nsec)</td>
<td>Average Power (dB)</td>
<td>Relative Delay (nsec)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2928</td>
<td>-10</td>
<td>2928</td>
</tr>
<tr>
<td>1200</td>
<td>0</td>
<td>1563</td>
</tr>
<tr>
<td>2344</td>
<td>-9</td>
<td></td>
</tr>
</tbody>
</table>

Simulation Results
Simulation results are displayed in Figure 2-6.

![Figure 2-6. Simulation Results](image)

Benchmark
- Hardware Platform: Pentium 4 2.3GHz, 512 MB memory
- Software Platform: Windows 2000, ADS 2003C
• Simulation Time: 35 hours

References

Chapter 3: TD-SCDMA Instrument Link Designs

Introduction

The TD-SCDMA_LinkTest project demonstrates the characteristics of ADS and instrument links. Design examples in this project are described in the following sections:

- Base station signal generated using ADS-ESGc link measured by VSA89600: TDSCDMA_DL_Link.dsn.
- User equipment signal generated using ADS-ESGc link measured by VSA89600: TDSCDMA_UL_Link.dsn.
TD-SCDMA Instrument Link Designs

Base Station Signal Generated Using ADS-ESGc Link Measured by VSA89600

TDSCDMA_DL_Link.dsn

Description

This design demonstrates ADS and instrument links. The BTS signal is generated using ADS-ESGc link, then measured by VSA89600.

The top-level schematic for this design is shown in Figure 3-1.

- TDSCDMA_DL_RF is used to generate downlink RF signal.
- VSA_89600_1_Sink is used to start VSA89600 software to measure the RF signal.
- ESG_E4438C_Sink is used to send I, Q data to ESG.

Figure 3-1. TDSCDMA_DL_Link.dsn Schematic
Simulation Results

Simulation results are displayed in VSA89600 window and shown in Figure 3-2.

Figure 3-2. TDSCDMA_DL_Link.dsn Simulation Results
Benchmark

- Hardware Platform: Pentium III 800 MHz, 512 MB memory
- Software Platform: Windows 2000, ADS 2002C, VSA89600 4.00x2_BETA
- Simulation Time: N/A

References

User Equipment Signal Generated Using ADS-ESGc Link Measured by VSA89600

TDSCDMA_UL_Link.dsn

Description

This design demonstrates ADS and instrument links. The user equipment signal is generated using ADS-ESGc link, then measured by VSA89600.

The top-level schematic for this design is shown in Figure 3-3.

- TDSCDMA_DL_RF is used to generate uplink RF signal.
- VSA_89600_1_Sink is used to start VSA89600 software to measure the RF signal.
- ESG_E4438C_Sink is used to send I, Q data to ESG.

Figure 3-3. TDSCDMA_UL_Link.dsn Schematic
**Simulation Results**

Simulation results are displayed in VSA89600 window and shown in Figure 3-4.

**Benchmark**

- Hardware Platform: Pentium III 800 MHz, 512 MB memory
- Software Platform: Windows 2000, ADS 2002C, VSA89600 4.00x2_BETA
- Simulation Time: N/A

**References**

Chapter 4: TD-SCDMA Power Amplifier Designs

Introduction

The TDSCDMA_PA_Test project includes these design examples.

- Characterization of peak average power ratio versus probability: TDSCDMA_DL_CCDF.dsn.
- Instant and average power versus time measurements: TDSCDMA_UL_Power_vs_Time.dsn.
- CCDF and spectrum of multi-carrier signal measurements: TDSCDMA_MC_Test.dsn.
Complementary Cumulative Distribution Function Measurements

TDSCDMA_PA_Test_prj Design Name

- TDSCDMA_DL_CCDF.dsn

Features

- Configurable signal source subnetwork model.
- DUT_Gain, FCarrier, Power, SamplesPerSymbol and SlotIndex parameter values can be set by the user.

Description

Complementary cumulative distribution function (CCDF) fully characterizes the power statistics of a signal. It provides peak-average ratio versus probability.

The top-level schematic for this design is shown in Figure 4-1.

Simulation Results

Simulation results are displayed in TDSCDMA_DL_CCDF.dds.

Page main, Figure 4-2, contains the most important final results and indicates if the measurement results met the requirement of technical specification. In this
measurement, the test results would always be passed since there is no requirement of CCDF in TD-SCDMA technical specification.

Page figures, Figure 4-3, shows the CCDF curve.

Page equations contains all variable definitions and calculations.

<table>
<thead>
<tr>
<th>MeanPower(dBm)</th>
<th>PeakPower(dBm)</th>
<th>Peak_to_Mean(dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>40.1142</td>
<td>45.552</td>
<td>6.457</td>
</tr>
</tbody>
</table>

Figure 4-2. Page Main of Simulation Results

Complementary Cumulative Distribution Function (CCDF)

Figure 4-3. Page Figures of Simulation Results

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT 4.0 Workstation, ADS 2002
- Simulation Time: approximately 3 minutes

References

TD-SCDMA Power Amplifier Designs

Power vs. Time Measurement

TDSCDMA_UL_Power_vs_Time.dsn

Features

- Power vs. time measurement
- 12.2kbps uplink reference measurement channel
- Roll-off $\alpha = 0.22$ root raised-cosine filter

Description

This example measures power vs. time for TD-SCDMA uplink. Power vs. time is calculated by averaging the power of chips at the same position in all measured subframes.

The schematic for this design is shown in Figure 4-4. TDSCDMA_UL_RF generates the 12.2k measurement channel. TDSCDMA_PwrMeasure implements the power measurement.

Figure 4-4. TDSCDMA_Power_vs_Time Schematic
Simulation Results

Simulation results are displayed in Figure 4-5.

The Equations page shows the equations that are used for calculating the mask.

![TDSCDMA RF Power vs. Time](image)

The test result curves should be within the masks.

Test Results

Passed

Figure 4-5. Power vs. time for TD-SCDMA Uplink

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 2001
- Simulation Time: approximately 2 minutes

References

CCDF and Spectrum Measurements of Multi-carrier Signal

TDSCDMA_PA_Test_prj Design Name
- TDSCDMA_MC_Test.dsn

Features
- Multi-carrier signal source with 16 code channels on each carrier.
- FCarrier, FiletrLength, SamplesPerSymbol, DUT_Gain, NumSlotsMeasured and SystemDelay parameter values can be set by the user.

Description
The top-level schematic for this design is shown in Figure 4-6.

The sub_TDSCDMA_Channel16_MC provides multi-carrier signal on (1900-1.6)MHz, 1900MHz and (1900+1.6)MHz. The CCDF MeasurementMC and SpectrumAnalyzer is used to measure the CCDF and spectrum of the multi-carrier signal and the CCDF MeasurementSC is used to measure the CCDF of the single-carrier signal on 1900MHz.
The sub_TDSCDMA_Channel16_MC schematic is shown in Figure 4-7.

![Figure 4-7. sub_TDSCDMA_Channel16_MC Schematic](image)

X1, X2 and X3 are sub_TDSCDMA_Channel16 subnetworks which provide baseband signal of a subframe including 16 code channels in time slot 6 and null in other time slots. X1 is modulated to 1900 MHz, X2 to (1900-1.6) MHz and X3 to (1900+1.6) MHz.

**Simulation Results**

Simulation results displayed in TDSCDMA_MC_Test.dds are shown in Figure 4-8.
TD-SCDMA Power Amplifier Designs

Benchmark

- Hardware Platform: Pentium III 1 GHz, 512 MB memory
- Simulation Time: approximately 5 minutes

References

Chapter 5: TD-SCDMA Receiver Designs

Introduction

The TD-SCDMA receiver project demonstrates user equipment and base station characteristics. Design examples in this project are described in the following sections:

- BTS reference sensitivity level: TDSCDMA_UL_Sensitivity.dsn.
- UE adjacent channel selectivity: TDSCDMA_DL_AdjacentChannel.dsn.
Base Station Reference Sensitivity Level

TDSCDMA_UL_Sensitivity.dsn

Description
This design measures the base station reference sensitivity level. The reference sensitivity level is the minimum mean power received at the antenna connector at which BER cannot exceed the value given in Table 5-1.

<table>
<thead>
<tr>
<th>Reference Measurement Channel Data Rate</th>
<th>BS Reference Sensitivity Level</th>
<th>BER</th>
</tr>
</thead>
<tbody>
<tr>
<td>12.2 kbps</td>
<td>-110 dBm</td>
<td>BER cannot exceed 0.001</td>
</tr>
</tbody>
</table>

The top-level schematic for this design is shown in Figure 5-1.

- TDSCDMA_RefCh_RF is used to generate 12.2 kbps uplink RF signal.
- TDSCDMA_12_2_UL_RakeReceiver is used to receive the uplink RF signal with data rate 12.2 kbps.
- TDSCDMA_BER is used to measure the BER.
- TDSCDMA_RF_PwrMeasure is used to measure the mean power at the input port of the receiver.

Figure 5-1. TDSCDMA_UL_Sensitivity.dsn Schematic
Simulation Results

Simulation results are displayed in the data display window and shown in Figure 5-2.

<table>
<thead>
<tr>
<th>Signal Power (dBm)</th>
<th>Reference (dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>-30</td>
</tr>
<tr>
<td>20</td>
<td>-20</td>
</tr>
<tr>
<td>30</td>
<td>-10</td>
</tr>
<tr>
<td>40</td>
<td>0</td>
</tr>
<tr>
<td>50</td>
<td>10</td>
</tr>
<tr>
<td>60</td>
<td>20</td>
</tr>
<tr>
<td>70</td>
<td>30</td>
</tr>
<tr>
<td>80</td>
<td>40</td>
</tr>
<tr>
<td>90</td>
<td>50</td>
</tr>
</tbody>
</table>

Expected: less than 0.1% within 95% confidence

Result: IMPER

Figure 5-2. TDSCDMA_UL_Sensitivity.dsn Simulation Results

Benchmark

• Hardware Platform: Pentium III 400 MHz, 512 MB memory
• Software Platform: Windows NT, ADS 2002
• Simulation Time: approximately 6 hours

References

User Equipment Adjacent Channel Selectivity

TDSCDMA_DL_AdjacentChannel.dsn

Description

This design measures the adjacent channel selectivity. Adjacent channel selectivity is a measure of the receiver’s ability to receive a wanted signal at its assigned channel frequency in the presence of an adjacent channel signal.

For the user equipment power class 2 and 3, the BER cannot exceed 0.001 for parameters specified in Table 5-2. This test condition is equivalent to an adjacent channel selectivity value of 33 dB.

Table 5-2. Test Parameters for Adjacent Channel Selectivity

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>ΣDPCH-Ec/I₀</td>
<td>dB</td>
<td>0</td>
</tr>
<tr>
<td>I₀</td>
<td>dBm/1.28 MHz</td>
<td>-91</td>
</tr>
<tr>
<td>Iosc</td>
<td>dBm/1.28 MHz</td>
<td>-54</td>
</tr>
<tr>
<td>F_UW offset</td>
<td>MHz</td>
<td>+1.6 or -1.6</td>
</tr>
</tbody>
</table>

The top-level schematic for this design is shown in Figure 5-3.

- The upper TDSCDMA_RefCh_RF is used to generate wanted 12.2 kbps downlink RF signal; the lower TDSCDMA_RefCh_RF is the adjacent channel signal.
- TDSCDMA_12_2_DL_RakeReceiver is used to receive the wanted downlink RF signal with a 12.2 kbps data rate in the presence of adjacent channel signal.
- TDSCDMA_BER is used to measure the BER.
- TDSCDMA_RF_PwrMeasure is used to measure the mean power at the input port of the receiver.
Simulation Results

Simulation results are shown in Figure 5-4.

<table>
<thead>
<tr>
<th>Signal Power (dBm)</th>
<th>(dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1001</td>
<td>1.500</td>
</tr>
<tr>
<td>1002</td>
<td>2.000</td>
</tr>
<tr>
<td>1003</td>
<td>2.500</td>
</tr>
<tr>
<td>1004</td>
<td>3.000</td>
</tr>
<tr>
<td>1005</td>
<td>3.500</td>
</tr>
<tr>
<td>1006</td>
<td>4.000</td>
</tr>
<tr>
<td>1007</td>
<td>4.500</td>
</tr>
<tr>
<td>1008</td>
<td>5.000</td>
</tr>
<tr>
<td>1009</td>
<td>5.500</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Interference Power (dBm)</th>
<th>(dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1001</td>
<td>-199.984</td>
</tr>
<tr>
<td>1002</td>
<td>-198.984</td>
</tr>
<tr>
<td>1003</td>
<td>-197.984</td>
</tr>
<tr>
<td>1004</td>
<td>-196.984</td>
</tr>
<tr>
<td>1005</td>
<td>-195.984</td>
</tr>
<tr>
<td>1006</td>
<td>-194.984</td>
</tr>
<tr>
<td>1007</td>
<td>-193.984</td>
</tr>
<tr>
<td>1008</td>
<td>-192.984</td>
</tr>
<tr>
<td>1009</td>
<td>-191.984</td>
</tr>
</tbody>
</table>

Expected: less than 0.1% within 95% confidence

Result: 0.004

Figure 5-4. Adjacent Channel Selectivity Measurement Results
TD-SCDMA Receiver Designs

Benchmark

- Hardware Platform: Pentium III 450MHz, 512MB memory
- Simulation Time: approximately 9 hours

References

Chapter 6: TD-SCDMA Signal Source Designs

Introduction

The TDSCDMA_SignalSource project demonstrates the special transient characteristics of TD-SCDMA signals from time and frequency domains, as well as rate matching calculation. Design examples in this project are described in the following sections:

- Uplink signal characteristics: TDSCDMA_UL_Spectrum.dsn.
- Downlink signal characteristics: TDSCDMA_DL_ACLR.dsn.
- Rate matching calculator demonstration: TDSCDMA_RM_Cal_Demo.dsn
Uplink Signal Characteristics

TDSCDMA_UL_Spectrum.dsn

Description

This design demonstrates user equipment out-of-band emissions; these are unwanted emissions immediately outside the nominal channel that result from the modulation process and non-linearity in the transmitter but excluding spurious emissions. This out-of-band emission limit is specified in terms of a spectrum emission mask and adjacent channel power.

The spectrum emission mask of the user equipment applies to carrier frequencies that are between 0.8 and 4.0 MHz. The out-of-channel emission is specified relative to the user equipment output power measured in a 1.28 MHz bandwidth. The power of any user equipment emission cannot exceed the levels specified in Table 6-1.

The top-level schematic for this design is shown in Figure 6-1.

- TDSCDMA_UL_RF generates a 12.2 kbps uplink RF signal source that includes one DPCH.
• The SpectrumMeasure subnetwork, Figure 6-2, measures the out-of-band emission spectrum and the average power measured in a 1.28 MHz bandwidth centered at the carrier frequency.
TD-SCDMA Signal Source Designs

Figure 6-2. SpectrumMeasure Subnetwork Schematic

Simulation Results

Simulation results displayed in the TDSCDMA_UL_Spectrum.dds data display window are shown in Figure 6-3.
Benchmark

- Hardware Platform: Pentium III 800 MHz, 512 MB memory
- Simulation Time: approximately 1 hour

References

Adjacent Channel Power Leakage Ratio

TDSCDMA_DL_ACLR.dsn

Features
- ACLR measurements for TD-SCDMA downlink
- 12.2 kbps downlink reference measurement channel
- Roll-off $\alpha = 0.22$ root raised-cosine filter

Description
This example measures ACLR for TD-SCDMA downlink.

The schematic for this design is shown in Figure 6-4. TDSCDMA_DL_RF generates the 12.2 kbps downlink reference channel for the measurement. The SpectrumMeasure subnetwork implements average power measurement through a root raised-cosine filter. By offsetting the center frequency of the root raised-cosine filter, power leakage on the adjacent channel is measured.
Simulation Results

Simulation results displayed in the TDSCDMA_DL_ACLR.dds data display window are shown in Figure 6-5.

<table>
<thead>
<tr>
<th>FreqOffset</th>
<th>CarrierPower[2..5]-CarrierPower[1..3]</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.200</td>
<td>67.497</td>
</tr>
<tr>
<td>1.600</td>
<td>49.925</td>
</tr>
<tr>
<td>0.000</td>
<td>0.000</td>
</tr>
<tr>
<td>1.600</td>
<td>49.913</td>
</tr>
<tr>
<td>3.200</td>
<td>60.300</td>
</tr>
</tbody>
</table>

Notes:
The ACLR is measured in dB.
The limits for +/-1.6MHz and +/-3.2MHz offset from the Center Frequency are 40dB and 50dB, respectively, for the minimum requirement.

Figure 6-5. ACLR Measurements for TD-SCDMA Downlink

Benchmark

- Hardware Platform: Pentium II 400MHz, 523MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 2002
- Simulation Time: approximately 20 minutes

References

Rate Match Calculator

TDSCDMA_RM_Cal_Demo.dsn

Description

This design demonstrates the use of TDSCDMA_RM_Cal rate matching calculator model. The puncture limit and rate match attributes are specified by users when they configure TDSCDMA Design Library models related to rate matching.

In TDSCDMA specifications, frame sizes before and after rate matching are supplied for reference measurement channels only. TDSCDMA_RM_Cal calculates the puncture limit and rate match attributes from the given frame sizes.

The schematic for this design is shown in Figure 6-6.

Simulation Results

Simulation results displayed in TDSCDMA_RM_Cal_Demo.dds are shown in Figure 6-7.
Figure 6-7. Puncture Limit and Rate Match for each Transport Channel

**Benchmark**

- Hardware Platform: Pentium IV 2.26 GHz, 512 MB memory
- Software Platform: Windows 2000, ADS 2003C
- Simulation Time: 4 seconds

**References**

TD-SCDMA Signal Source Designs
Chapter 7: TD-SCDMA Transmitter Designs

Introduction

The TDSCDMA Tx project demonstrates user equipment and base station characteristics. Design examples in this project are described in the following sections:

- Base station error vector magnitude: TDSCDMA_DL_EVM.dsn.
- User equipment code domain power: TDSCDMA_UL_CDP.dsn.
TD-SCDMA Transmitter Designs

**Base Station Error Vector Magnitude**

TDSCDMA_DL_EVM.dsn

**Description**

This design demonstrates the base station error vector magnitude measurement to determine the difference between the reference waveform and the measured waveform. This difference is called the error vector. Both waveforms pass through a matched root raised-cosine filter with a bandwidth corresponding to the considered chip rate and roll-off a = 0.22. Both waveforms are then further modified by selecting the frequency, absolute phase, absolute amplitude and chip clock timing so as to minimize the error vector. The EVM result is defined as the square root of the ratio of the mean error vector power to the mean reference power expressed as a percentage. The measurement interval is one time slot. The error vector magnitude (EVM) cannot exceed 12.5%. The requirement is valid over the total power dynamic range as specified in subclause 6.4.3 of TS 25.105.

The top-level schematic for this design is shown in Figure 7-1.

- TDSCDMA_DL_RF is used to generate a 12.2 kbps uplink RF signal.
- TDSCDMA_EVM is used to measure the EVM value of the RF signal. The algorithm is the same as that of VSA89600.

Simulation Results

Simulation results are shown in Figure 7-2.
Average Channel Results

<table>
<thead>
<tr>
<th>Subframe</th>
<th>CId/Id (avg)</th>
<th>PId/Id (avg)</th>
<th>CPh/Id (avg)</th>
<th>PPh/Id (avg)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.274</td>
<td>0.334</td>
<td>0.276</td>
<td>0.334</td>
</tr>
<tr>
<td>2</td>
<td>0.334</td>
<td>0.276</td>
<td>0.334</td>
<td>0.276</td>
</tr>
<tr>
<td>3</td>
<td>0.334</td>
<td>0.276</td>
<td>0.334</td>
<td>0.276</td>
</tr>
<tr>
<td>4</td>
<td>0.334</td>
<td>0.276</td>
<td>0.334</td>
<td>0.276</td>
</tr>
<tr>
<td>5</td>
<td>0.334</td>
<td>0.276</td>
<td>0.334</td>
<td>0.276</td>
</tr>
<tr>
<td>6</td>
<td>0.334</td>
<td>0.276</td>
<td>0.334</td>
<td>0.276</td>
</tr>
</tbody>
</table>

Channel Results vs Subframe

<table>
<thead>
<tr>
<th>Subframe</th>
<th>CId/Id (avg)</th>
<th>PId/Id (avg)</th>
<th>CPh/Id (avg)</th>
<th>PPh/Id (avg)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.274</td>
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<td>0.334</td>
</tr>
<tr>
<td>2</td>
<td>0.334</td>
<td>0.276</td>
<td>0.334</td>
<td>0.276</td>
</tr>
<tr>
<td>3</td>
<td>0.334</td>
<td>0.276</td>
<td>0.334</td>
<td>0.276</td>
</tr>
<tr>
<td>4</td>
<td>0.334</td>
<td>0.276</td>
<td>0.334</td>
<td>0.276</td>
</tr>
<tr>
<td>5</td>
<td>0.334</td>
<td>0.276</td>
<td>0.334</td>
<td>0.276</td>
</tr>
<tr>
<td>6</td>
<td>0.334</td>
<td>0.276</td>
<td>0.334</td>
<td>0.276</td>
</tr>
</tbody>
</table>

Average Composite Results

<table>
<thead>
<tr>
<th>Avg_CompId/Id</th>
<th>Avg_CompPId/Id</th>
<th>Avg_CompCPh/Id</th>
<th>Avg_CompPPh/Id</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.271</td>
<td>0.337</td>
<td>0.276</td>
<td>0.334</td>
</tr>
</tbody>
</table>

Composite Results vs Subframe

<table>
<thead>
<tr>
<th>Subframe</th>
<th>CId/Id (avg)</th>
<th>PId/Id (avg)</th>
<th>CPh/Id (avg)</th>
<th>PPh/Id (avg)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.274</td>
<td>0.334</td>
<td>0.276</td>
<td>0.334</td>
</tr>
<tr>
<td>2</td>
<td>0.334</td>
<td>0.276</td>
<td>0.334</td>
<td>0.276</td>
</tr>
<tr>
<td>3</td>
<td>0.334</td>
<td>0.276</td>
<td>0.334</td>
<td>0.276</td>
</tr>
<tr>
<td>4</td>
<td>0.334</td>
<td>0.276</td>
<td>0.334</td>
<td>0.276</td>
</tr>
<tr>
<td>5</td>
<td>0.334</td>
<td>0.276</td>
<td>0.334</td>
<td>0.276</td>
</tr>
<tr>
<td>6</td>
<td>0.334</td>
<td>0.276</td>
<td>0.334</td>
<td>0.276</td>
</tr>
</tbody>
</table>

Figure 7-2. TDSCDMA_DL_EVM.dsn Simulation Results
TD-SCDMA Transmitter Designs

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT 4.0, ADS 2003A
- Simulation Time: 1 minute

References

User Equipment Code Domain Power

TDSCDMA_UL_CDP.dsn

Description

This design demonstrates the code domain power measurement of user equipment. Code domain power is the part of the mean power which correlates with a particular (OVSF) code channel. The sum of all powers in the code domain equals the mean power in a bandwidth of \((1+a)\) times the chip rate of the radio access mode.

The top-level schematic for this design is shown in Figure 7-3.

- TDSCDMA_DL_RF is used to generate an uplink RF signal.
- VSA_89600_1_Sink is used to start the VSA89600 software to measure the RF signal.
- ESG_E4438C_Sink is used to send I, Q data to ESG.

Figure 7-3. TDSCDMA_UL_Link.dsn Schematic

Simulation Results

Simulation results are displayed in a VSA89600 window are shown in Figure 7-4.
Figure 7-4. TDSCDMA_UL_Link.dsn Simulation Results

**Benchmark**

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT4.0, ADS 2002C, VSA89600 4.00x2_BETA
- Simulation Time: 1 minute

**References**

# Index

**B**
- BER performance, 2-1
- BLER performance, 2-1
- burst structure, 1-2

**I**
- instrument links, 3-1

**J**
- joint detection receiver, 1-3

**P**
- physical layer, 1-1
- power amplifiers, 4-1

**R**
- Rake receiver, 1-3
- receivers, 5-1

**S**
- signal sources, 6-1
- smart antenna, 1-1

**T**
- TD-SCDMA standard, 1-1
- time slots, 1-1
- transmitter structure, 1-2
- transmitters, 7-1

**U**
- uplink synchronization, 1-1