Open solder joints are one of the most prominent faults in surface mount manufacturing.

Vectorless tests find them. But how do you determine if a given technique is effective?
Two years ago, you were probably asking, “What is vectorless test and why do I need it?” Today, the question is, “Which vectorless test technique is best for me?”

This guide will help you evaluate different vectorless test options, such as X-ray laminography, capacitive lead-frame testing, parasitic diode analysis, and inductive coupling, as well as complementary techniques like boundary-scan which easily produces vectors. It is designed to help you judge objectively which test technique will ultimately serve you most effectively.

The most important question is, how well does a given test technique really work?

Will it test your particular board topologies? Are its measurements dependable, providing unquestionable diagnostics? Does it stress your ICs? Does it depend upon a known good board? Will it function well in your production environment? Is it reliable, repeatable and transportable?

The following set of questions elaborates on these issues. And for further background, a tutorial briefly describes how a “false” test result can occur, and why that matters.

Know Your Typical Faults

It is important to know whether a vectorless test technique reliably addresses your top faults or whether it focuses on less significant ones. For instance, SMT solder opens occur so frequently that they are measured in percentages, but other faults occur so rarely that they are measured in PPM. So it is obviously more important to have an accurate test of solder opens than a collection of mediocre tests for the infrequently occurring faults.

It is also important to assess a test system’s entire suite of tools—how close does the entire set come to 100% coverage? How do you choose which mix of tools to use for your particular situation and how easily are incremental tests added to your manufacturing process?

Assess Industry Acceptance of the Technique

One indication of how well a given technique works is the number of other companies that have licensed it for use on their own systems.

Also find out which companies are successfully using the technique. The vendor’s willingness to give you names and phone numbers of specific references is an indication of the technique’s usefulness.

Ask Current Users These Questions

Asking the following questions of customers using the technique will help you determine its actual effectiveness.

1. How dependable is this technique?

Getting a board to “pass” does not necessarily mean the solder opens are being detected. (See Tutorial) How do you know open solder joints are really being detected, so that boards fail only when faults are present and pass only when they are truly good boards?

1.1 Have standard deviations and areas of discrimination been measured and characterized? Is the test threshold valid?

1.2 Does the test discriminate between a fault and a no-fault signal?

2. How effective is this technique?

False passes from vectorless test send faulty boards to the next stage—or even to the customer—where repair is more expensive.

2.1 How many solder opens do you detect in your next stage of test?

Vectorless Test Saves Time and Reduces Manufacturing Costs

In surface mount manufacturing, the solder open is one of the most frequently occurring faults. It was also one of the most expensive faults to detect, because powered in-circuit test requires a great deal of programming time to generate custom tests or translate vectors. And the necessary test libraries are often difficult and time-consuming to create.

Meanwhile, shorter product life cycles pressure manufacturers to reduce test development time. Today’s vectorless test solutions play a significant role in meeting this challenge.

The benefits of vectorless test are its speed in detecting opens—especially considering that no programming is required—and its ability to diagnose process faults to the pin level. Vectorless test can dramatically improve time-to-volume and reduce your manufacturing costs.

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3. Does this technique test every topology?
Any test technique is useful only to the extent that it can test the real boards that you build in the real world.

3.1 Is it limited by buses? By tied pins? By mixed technologies? By mixed logic families?
3.2 Can it test both sides of double-sided boards?
3.3 How do you know you are finding solder opens on the bottom-side components?

4. Are the measurements accurate?
Effective tests give you confidence in the ability to make decisions based solely on the diagnostic system.

4.1 Is the technique able to eliminate cross talk?
4.2 Are the measurements diminished in the inevitable noise of a manufacturing floor?
4.3 No-clean adds variable, unpredictable miliohms to ohms of fixture contact resistance. How accurately does this technique function within that range of variance?

5. Are the measurements stable?
Consistency over time and over change—two elements typical of every manufacturing environment—will affect your ability to trust the test technique.

5.1 Are tests stable from one test system to another?
5.2 Do measurements fluctuate during the test development process?
5.3 How sensitive is this technique to component vendor or batch changes?
5.4 How clearly are problems identified when the device-under-test is rotated or missing?
5.5 Can the technique test parallel or bussed devices?
5.6 Are the measurements affected by adhesive paper or metalized labels on the device-under-test?

6. What measurement approach is used?
A learned technique tells you the measurement values for a good board, but does not tell you the values for a bad board, or adjust well to variation between vendors. Setting a value threshold for a learned board becomes problematic, with the risk of increased false passes and false failures.

6.1 Does this technique use a calculated measurement approach, or a “learned good board” approach?
6.2 Are you dependent upon a known good board for test development? What happens if you have legitimate but unknown opens on your known good board?

7. Is the technique suited to a production environment?
Effective test lowers manufacturing costs—only if it dependable keeps pace with your production environment.

7.1 Is the throughput adequate for your production line?
7.2 How long does debug continue after release to production? Does this debug increase or decrease fault coverage?

If you answer all these questions to your satisfaction, you will end up with a reliable, repeatable, transportable vectorless test product that will work for you.

8. Does this technique stress your IC?
Some vectorless techniques may draw excessive levels of current, stressing the device outside of its specification ranges, and impacting the device’s ultimate useful life span.

8.1 Have you ever observed device damage caused by using this test technique?
8.2 Are the product’s current or voltage levels and test times sufficient to cause IC damage?

9. Does this technique reduce or increase your time to volume?
Some techniques can be up and running within 20 minutes. Others require extensive coordination between design and test. Time is a key variable in selecting a vectorless technique—don’t miss the hidden time consumers.

9.1 How much information is needed about the package?
9.2 What information is needed about the board topology? Is all of this information in your CAD data?
9.3 How long does it take to debug a new test in test development?
9.4 How much time and effort are required to maintain the test in manufacturing, after your application is in production?
9.5 How do you know you are finished debugging the test?

10. What impact does this technique have on your cost of manufacturing?
A test technique’s technical performance and impact on time-to-volume have everything to do with cost of manufacturing test.

If you answer all these questions to your satisfaction, you will end up with a reliable, repeatable, transportable vectorless test product that will work for you.
The Significance of False Failures and False Passes

Vectorless tests are useful only to the extent that they are accurate—passing good boards on to the next step, and failing boards that actually have faults—and provide accurate diagnostics. Vectorless test techniques have different levels of success in providing accurate results, with implications to cost of test and cost of manufacturing.

False failures and false passes are expensive. A missed fault (false pass) may be revealed later in the manufacturing process—when repair is significantly more costly. Or it may be passed on to a customer. False failures can result in perfectly good—and possibly very expensive—parts being removed and replaced unnecessarily.

How Does a Test System Produce a False Failure?

For a good component to fail test, its actual measured value must be within its tolerance limits yet outside its test limits. Error is inherently introduced by the measurement device, so judgements must be made about readings near the tolerance limits. Should a device near its limits pass or fail?

To answer this, measurement uncertainty error, describing measurement precision, must be characterized by the standard deviation of measurement values and combined with device limits to rationally remove the risk of tester-induced error.

Measurement uncertainty error is the effect of random errors, and can be influenced by contact resistance between the tester and the device-under-test, environmental effects on the measurement system (such as noise, power and temperature), or component aging of the test system.

How Does a Test System Produce a False Pass?

A false pass occurs when a device’s measured value is above its test limits. False passes can also occur when the area of discrimination is so narrow that the tester cannot accurately set the threshold between the measurement values of a good solder and an open solder connection.

Another cause of false passes is topological interaction—unexpected or unanalyzed feedback paths on the board or intrinsic characteristics of the device being tested.

Valid thresholds can be set for both the third and fourth pins’ set of measurements, because there is ample area of discrimination between the two six-sigma lines cross, as in the first pin, thus eliminating the area of discrimination.

Validation thresholds can be set for good solder connections—passing good boards and failing bad ones.

Measuring Test Effectiveness

A test is a collection of measurements whose returned values are compared to predetermined thresholds. Measurements which fall to one side of the threshold pass. Measurements which fall to the other side fail. The extent to which a test fails a working assembly and passes a faulty assembly determines the test’s effectiveness.

Setting valid thresholds for vectorless test is challenging for several reasons. The graph below shows a set of 25 measurements for each of four IC pins.

Green represents the measurement values for good solder connections; black represents those for open solder connections.

The green dotted lines represent six sigma below the mean of good solder measurement values—the closest threshold that can rationally be set. The solid black lines represent six sigma above the mean of open solder measurement values. The space between the dotted upper and solid lower lines for pins 3 and 4 is the area of discrimination. A threshold can be set anywhere within this area. There is no area of discrimination for pins 1 and 2.

The first pin’s 25 measurements show a valid measurement threshold cannot be set for two reasons: high standard deviation of measurements of both good and open solder joints, and no area of discrimination between the measured values of good solder and open solder measurements.

The second pin’s measurements cannot have a valid threshold set, due to the magnitude of standard deviation of the good solder measurement values. Although there appears to be a reasonable area of discrimination between measurement values, the six-sigma lines cross, as in the first pin, thus eliminating the area of discrimination.

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Finding Thresholds for Vectorless Test

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Valid thresholds can be set for good solder connections—passing good boards and failing bad ones.