Help Volume

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System: E5820A Demo Board
The Agilent E5820A Demo Board

The Agilent E5820A Demo Board can be used to gain familiarity with and verify setup of logic analyzers. It provides an 8-bit (count or toggle) data pattern at the rate of 200 Mb/s.

The Demo Board offers two types of logic analyzer connectors, which allow connection to standard Agilent logic analyzer probe cables. The Demo Board also has a pin header that allows connection using flying leads. The pin header can be used to show the signals on an oscilloscope while simultaneously making an Eye Scan measurement.

Some of the data bits on the Demo Board have intentional signal conditioning: delay, damping, peaking, and DC offset. These are useful in demonstrating Agilent Eye Scan and Timing Zoom. If desired, you can connect an external pattern generator to the Demo Board. The intentional signal conditioning is applied to the external pattern.

The Demo Board is powered from the logic analyzer, so an external power supply is not required.

**CAUTION**

You must not connect to J1 and J2 at the same time. Doing so will short the +5 V power supplies of the analyzers together, possibly resulting in serious equipment damage.

See:

- “Setting the Demo Board Configuration Switches” on page 19
- “Using the Demo Board with 16753/54/55/56/60 Analyzers” on page 6
- “Using the Demo Board with 16750/51/52 Logic Analyzers” on page 15

Reference Information:

- “Demo Board Connector Descriptions” on page 17
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Summary
This section will lead you through setting up the demo board and using state mode, timing mode, eye scan, and timing zoom with the 16753A, 16754A, 16755A, 16756A, and 16760A logic analyzer modules.

CAUTION
You must not connect to J1 and J2 at the same time. Doing so will short the +5 V power supplies of the analyzers together, possibly resulting in serious equipment damage.

Choose the cable that you will use to connect the logic analyzer to the demo board.

- “Connecting with the E5378A Single-Ended Probe” on page 6
- “Connecting with the E5379A Differential Probe” on page 7
- “Connecting with the E5382A Single-Ended Flying Lead Probe” on page 8

Connecting with the E5378A Single-Ended Probe

Connect the E5378A single-ended probe to the Samtec connector (J1) on the demo board. This 34-channel, high-density Samtec probe allows two pods worth of data to be probed using one Samtec connector on the target. When using this connector, the pods are referred to as ODD and EVEN (for example: Pod1 = ODD, Pod2 = EVEN).

The E5820A demo board will output 8 bits of data to each of the two pods in this cable. It will also provide a synchronous clock that can be used during STATE mode. All sampling should be done off of the ODD clock. If you are using pods 1 and 2 with this cable, the sampling clock will be J-clock.
For demo board compatibility with both the single-ended and differential probe cables, the 8 bits of data going to the ODD pod are the inverted version of the 8-bits of data going to the EVEN pod. So during a COUNT pattern, the EVEN pod will display an 8-bit UP counter while the ODD pod will display an 8-bit DOWN counter. Again, all data should be clocked off of the ODD clock (usually J- clock).

**Pod Assignments**

Use the "Format" tab in the "Setup and Trigger" window to set up two labels for the lower 8 bits of both pods that are connected to the E5378A probe cable. Also setup a label for the clock on the ODD pod.

**Thresholds**

Set the threshold voltage for all data bits to +2.0 V (LVPECL). Set the threshold for the clock to Differential.

Now you can choose to acquire data from the demo board in one of the following modes:

- “Using the Demo Board with 16753/54/55/56 in Timing Mode” on page 9
- “Using the Demo Board with 16753/54/55/56 in State Mode” on page 10
- “Using Demo Board with 16753/54/55/56, 4 GHz Timing Zoom” on page 11
- “Using the Demo Board with 16753/54/55/56 in Eye Scan Mode” on page 12

**Connecting with the E5379A Differential Probe**

Connect the E5379A Differential Probe to the Samtec connector (J1) on the demo board. This 17-channel differential probe will allow 16 bits of differential data and 1 differential clock to be probed using a Samtec connector on the target.

When using the differential probe, you will only see 8 bits of data (counting up) and one clock.
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Pod Assignments

Use the "Format" tab in the "Setup and Trigger" window to set up one label for the lower 8 bits of the pod that is connected to the E5379A probe cable. Also setup a label for the clock on this pod.

Thresholds

The logic analyzer will automatically recognize the probe cable and set the thresholds accordingly.

Now you can choose to acquire data from the demo board in one of the following modes:

- “Using the Demo Board with 16753/54/55/56 in Timing Mode” on page 9
- “Using the Demo Board with 16753/54/55/56 in State Mode” on page 10
- “Using Demo Board with 16753/54/55/56, 4 GHz Timing Zoom” on page 11
- “Using the Demo Board with 16753/54/55/56 in Eye Scan Mode” on page 12

Connecting with the E5382A Single-Ended Flying Lead Probe

Connect the E5382A Flying Lead Probe to the pin header (P10) on the demo board. The pin header brings out the 8 bits from the EVEN pod of the J1 connector. It also brings out the associated clock and 9 ground pins. When using the flying lead set, you will still need to have a connector plugged into the demo board in order to provide power. You will effectively be double-probing the EVEN pod when using the flying leads. Be sure to connect the J clock negative lead to ground.

NOTE: The clock on the demo board is single ended. Therefore, you MUST connect the "/CLK" lead from the Flying Lead Probe to a ground point (such as TP2) on the demo board. One of the supplied grabber clips (Agilent P/N 16517-82109) can be used for this purpose.

Pod Assignments

Use the "Format" tab in the "Setup and Trigger" window to set up one
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label for the lower 8 bits of the pod that is connected to the E5382A probe cable plugged into the demo board. Also setup a label for the clock on this pod.

Thresholds

Set the threshold voltage for all data and clock bits to +2.0 V (LVPECL).

Now you can choose to acquire data from the demo board in one of the following modes:

- “Using the Demo Board with 16753/54/55/56 in Timing Mode” on page 9
- “Using the Demo Board with 16753/54/55/56 in State Mode” on page 10
- “Using Demo Board with 16753/54/55/56, 4 GHz Timing Zoom” on page 11
- “Using the Demo Board with 16753/54/55/56 in Eye Scan Mode” on page 12

Using the Demo Board with 16753/54/55/56 in Timing Mode

Timing Mode allows you to Asynchronously sample the data using the analyzer clock. The 16753A, 16754A, 16755A, and 16756A provide 600 MHz Full Channel Timing Mode or 1.2 GHz Half Channel Mode.

At this point you are ready to take an acquisition. First setup the demo board to the correct mode using the RED toggle switches. Set the switches to CNT, INT, and up arrow.

- Under the "Sampling" tab on the "Setup and Trigger" menu, set the analyzer sampling mode to "Timing Mode" and the Timing Mode Controls to "xM Sample Full Channel 600 MHz Conventional". Set your Sample Period to 1.67 ns.

- Click the "RUN" button (the green arrow in the top left of your screen).

Examine the results in the WAVEFORM window. If you are using the E5378A probe, you will see an 8-bit UP counter on the EVEN pod and an 8-bit DOWN counter on the ODD pod. If you are using the E5379A
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probe, you will see an 8-bit UP counter. You will also see an associated clock. The clock is toggling at 200 MHz and the data is changing every 5 ns.

Since you are in TIMING mode, you can see when the individual bits switch within the 8-bit counter to a resolution of 1.67 ns. You can EXPAND the 8-bit bus to see each bit individually. You will notice that Bit[3] is delayed by ~1 ns. This is intentional to demonstrate the resolution of the 600 MHz timing mode (1.67 ns).

You can set the demo board switch to TOGGLE if you would like to see a 0x55/0xAA toggle pattern.

Using the Demo Board with 16753/54/55/56 in State Mode

State Mode allows you to Synchronously sample the data using the clock from the Device Under Test. The 16753A, 16754A, 16755A, and 16756A can latch data up to 600 MHz.

Again setup the demo board to the correct mode using the RED toggle switches. Set the switches to CNT, INT, and up arrow.

- Under the "Sampling" tab on the "Setup and Trigger" menu, set the sampling mode to "STATE Mode". Under Clock Setup, set the sampling clock to "J-Clock / Rising Edge".

- For best results, you should run EYE FINDER. This will automatically dial in the best sampling position. This allows you to get the best performance out of the analyzer.

- Click the "RUN" button (the green arrow in the top left of your screen).

Examine the results using either the WAVEFORM or LISTING window. Now you will see data patterns with clean transition regions (i.e., all bits change at the same time).

- The demo board can also provide STATE sampling on "Both Edges" of the system clock. Set the appropriate demo board switch to the "up arrow and down arrow" position.
- Under the "Sampling" tab on the "Setup and Trigger" menu, set the Clock Setup to "J-Clock / Both Edges".
- Run EYE FINDER to determine the best sampling position for this clocking mode.
- Click the "RUN" button (the green arrow in the top left of your screen).

Examine the results. You can set the demo board switch to TOGGLE if you would like to see a 0x55/0xAA toggle pattern.

While in State Mode, you can use Timing Zoom. See “Using Demo Board with 16753/54/55/56, 4 GHz Timing Zoom” on page 11

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**Using Demo Board with 16753/54/55/56, 4 GHz Timing Zoom**

Timing Zoom allows you to asynchronously sample data at a rate of 4 GHz while you simultaneously perform either a TIMING or STATE measurement.

- Leave the analyzer in STATE mode (see “Using the Demo Board with 16753/54/55/56 in State Mode” on page 10).
- Under the "Sampling" tab on the "Setup and Trigger" menu, click on the "Timing Zoom" button in the top right corner of the screen. Turn Timing Zoom ON.
- Click the "RUN" button (the green arrow in the top left of your screen).

Examine the results in the WAVEFORM window. You will see additional labels with the suffix '_TZ'. This is the Timing Zoom data. Expand the Timing Zoom results. Now you can see the transition of each bit with a resolution of 250 ps.

You will again see that Bit[3] is delayed ~1 ns. In addition you will see that Bit[4] is delayed ~500 ps. This is intentional to demonstrate the resolution of 4 GHz Timing Zoom (250 ps).
Using the Demo Board with 16753/54/55/56 in Eye Scan Mode

EYE SCAN allows the user to map out the eye diagram of probed data in time and voltage. This is a signal integrity measurement that gives the same insight as an oscilloscope but over a greater number of signals.

There are 5 bits on the demo board that are intentionally conditioned and brought out to the pin header (J10). They are as follows:

Bit[0] = Damped
Bit[1] = Peaked
Bit[2] = DC Offset
Bit[3] = 1 us delay
Bit[4] = 500 ps delay

The demo board can demonstrate the usefulness of EYE SCAN by showing the resultant eye diagram of these signals on the logic analyzer while simultaneously allowing the user to probe these signals with an oscilloscope. The results seen on the oscilloscope will match the results of the EYE SCAN measurement.

Demo Board Setup

Setup the demo board to the correct mode using the toggle switches. Set the switches to TOGGLE, INT, and Up Arrow.

Oscilloscope Setup

In order to see the high-bandwidth effects of these signals, you will need the following:

- 54845A Infiniium Oscilloscope, 1.5 GHz, 8 GSa/s
- and
- 1158A Active Probes, 10:1, 4 GHz (preferably 4 of these)
- or
- 1152A Active Probes, 10:1, 2.5 GHz (preferably 4 of these)
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- Connect three of the probes to the lower three bits of the pin header on the demo board (P10). Be sure to get a close ground. The silkscreen table on the demo board tells which pins are signals and which are ground. It also indicates which bits are damped, peaked, delayed, and DC-offset. The entire row of pins nearest the board edge are grounds.

- Connect the fourth probe to the 'Clock' bit of the pin header on the demo board.

- On the oscilloscope, set the following:
  Horizontal Scale 1 ns / div Horizontal Offset 4 ns
  All Channels: 200 mV / div Offset +2.0 V
  Trigger: Channel 4 (probing clock) Level +2.0v Edge Auto Rising
  Setup - Display - Connect Dots = OFF Setup - Display - Persistence = Infinite

- Now turn OFF Channel 4 (the trigger channel)

**Logic Analyzer Setup**

- Under the "Sampling" tab on the "Setup and Trigger" menu, set the sampling mode to "EYE SCAN Mode". Under Clock Setup, set the sampling clock to "J-Clock / Rising Edge"

- Under the "Format" tab on the "Setup and Trigger" menu, setup a label for the eight bits of the EVEN pod that you are probing on the demo board. Delete all other labels.

- Under the "Eye Scan" tab on the "Setup and Trigger" menu, setup the following:

  Scan Settings Tab - Time Min = -4 ns  
  Scan Settings Tab - Time Max = +6 ns  
  Scan Settings Tab - Scan Range = Fine

  - Under the "Eye Scan" Window, setup the following:

    Scale Tab - t/div = 1.0 ns/div  
    Scale Tab - mV/div = 200 mV/div  
    Scale Tab - t Position = 0 s  
    Scale Tab - V Offset = 2.0 V

    Display Tab - Display Mode = Color Graded  
    Display Tab - Aspect Ratio = Fixed 7:4
Run the Analyzer

Click the "RUN" button (the green arrow in the top left of your screen). Examine the correlation between the Oscilloscope measurement to the Eye Scan measurement.
Using the Demo Board with 16750/51/52 Logic Analyzers

Summary

This section will lead you through setting up the demo board and using state and timing modes with the 16750A/51A/52A logic analyzer card. You should plug your probe cable into the 3M connector (J2) on the demo board and press the reset button.

CAUTION

You must not connect to J1 and J2 at the same time. Doing so will short the +5 V power supplies of the analyzers together, possibly resulting in serious equipment damage.

Pod Assignments

Using the "Format" tab in the "Setup and Trigger" window, set up one label for the lower 8 bits of the pod that is connected to the probe cable plugged into the demo board. Also setup a label for the clock on this pod.

Setting the Threshold Voltages

Set the threshold voltage for all data bits and the clock to +1.4 V (LVTTL).

- “Using the Demo Board with 16750/51/52 in Timing Mode” on page 15
- “Using the Demo Board with 16750/51/52 in State Mode” on page 16

Using the Demo Board with 16750/51/52 in Timing Mode

Timing Mode allows you to Asynchronously sample the data using the analyzer clock. The 16750A, 16751A, and 16752A provide 400 MHz Full Channel Timing Mode or 800 MHz Half Channel Mode.
At this point you are ready to take an acquisition. First setup the demo board to the correct mode using the RED toggle switches. Set the switches to CNT, INT, and up arrow.

- Under the "Sampling" tab on the "Setup and Trigger" menu, set the analyzer sampling mode to "Timing Mode" and the Timing Mode Controls to "xM Sample Full Channel 400 MHz Conventional". Set your Sample Period to 2.5 ns.

- Click the "RUN" button (the green arrow in the top left of your screen).

Examine the results in the WAVEFORM window. You will see an 8-bit UP counter. You will also see an associated clock. The clock is toggling at 200 MHz and the data is changing every 5 ns.

Since you are in TIMING mode, you can see when the individual bits switch within the 8-bit counter to a resolution of 2.5 ns. You can set the demo board switch to TOGGLE if you would like to see a 0x55/0xAA toggle pattern.

Using the Demo Board with 16750/51/52 in State Mode

State Mode allows you to Synchronously sample the data using the clock from the Device Under Test. The 16750A, 16751A, and 16752A can latch data up to 400 MHz.

Again setup the demo board to the correct mode using the RED toggle switches. Set the switches to CNT, INT, and up arrow.

- Under the "Sampling" tab on the "Setup and Trigger" menu, set the sampling mode to "STATE Mode". Under Clock Setup, set the sampling clock to "J-Clock / Rising Edge"

- For best results, you should run EYE FINDER. This will automatically dial in the best sampling position. This allows you to get the best performance out of the analyzer.

- Click the "RUN" button (the green arrow in the top left of your screen).
Examine the results using either the WAVEFORM or LISTING window. Now you will see data patterns with clean transition regions (i.e., all bits change at the same time).

- The demo board can also provide STATE sampling on "Both Edges" of the system clock. Set the demo board switches to the "up arrow and down arrow" position.

- Under the "Sampling" tab on the "Setup and Trigger" menu, set the Clock Setup to "J-Clock / Both Edges".

- Run EYE FINDER to determine the best sampling position for this clocking mode.

- Click the "RUN" button (the green arrow in the top left of your screen).

Examine the results. You can set the demo board switch to TOGGLE if you would like to see a 0x55/0xAA toggle pattern.

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**Demo Board Connector Descriptions**

The following sections describe the connectors on the E5820A Demo Board.

- “Samtec Logic Analyzer Connector (J1)” on page 17
- “3M Logic Analyzer Connector (J2)” on page 18
- “3M Pattern Generator Connector (P11)” on page 18
- “Pin Header (P10)” on page 18

**Samtec Logic Analyzer Connector (J1)**

This connector can drive either the E5378A single-ended probe or E5379A differential Probe.

These probe cables are used on the 16753A, 16754A, 16755A, 16756A and 16760A logic analyzer modules.
When using the E5378A Single-Ended Probe, the demo board will drive 8-bits to each of the pods on the probe cable. It will also provide a synchronous clock to the ODD pod.

When using the E5379A Differential Probe, the demo board will drive 8 differential signals to the probe cable. It will also provide a synchronous clock.

The thresholds of the data signals on J1 are +2.0 V (LVPECL). The J1 clock threshold is differential.

**3M Logic Analyzer Connector (J2)**

This connector drives the 16715-61601 17-channel single-ended probe cable.

This probe cable is used on the 16715A, 16716A, 16717A, 16718A, 16719A, 16750A, 16751A, and 16752A logic analyzer modules.

The demo board will drive 8 bits to the pod on the probe cable. It will also provide a synchronous clock.

The thresholds of all signals on J2 are +1.4 V (LVTTL).

**3M Pattern Generator Connector (P11)**

This connector receives a pattern generator cable that uses the 10466A TRI-STATE TTL/3.3 V Data Pod.

When the pattern generator supplies the data pattern, the board acts as a straight pass-through to the logic analyzer connectors. The section on “Setting the Demo Board Configuration Switches” on page 19 describes this in more detail.

**Pin Header (P10)**

This connector brings out the 8 data bits and 1 clock that are being driven into the EVEN pod of the J1-Samtec connector. This header is used to demonstrate flying leads or Eye Scan. The silkscreen table on the board shows the signal mapping and signal conditioning of each pin.
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(pin 1) EVEN-D0 (Damped)  GND
EVEN-D1 (Peaked)  GND
EVEN-D2 (DC Offset)  GND
EVEN-D3 (1 ns Delay)  GND
EVEN-D4 (500 ps Delay)  GND
EVEN-D5  GND
EVEN-D6  GND
EVEN-D7  GND
CLOCK  GND

NOTE: If you want to see good correlation between the oscilloscope and Eye Scan, you need to use the Agilent 1158A 4 GHz active probe. This probe has the bandwidth required to see all of the discontinuities that Eye Scan will see.

Setting the Demo Board Configuration Switches

These switches (designated S1) set the mode of the demo board. The silkscreen labels on the board describe the operation of each switch.

"PG / INT Switch" - This switch tells the demo board whether to output an internal data pattern to the logic analyzer connectors or to pass the contents of the pattern generator to the logic analyzer connectors.

INT Mode - In this mode, the board uses an on-board oscillator to create either a count or toggle pattern and an associated clock.

PG Mode - In this mode, the board will pass the contents of the pattern generator directly to the logic analyzer connectors according to the following signal mapping: (NOTE: '#' means that the signal polarity will be inverted from what it is on the pattern generator.)

<table>
<thead>
<tr>
<th>Pattern Generator Pod</th>
<th>Samtec LA Connector (J1)</th>
<th>3M LA Connector (J2)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ODD</td>
<td>EVEN</td>
</tr>
<tr>
<td>D0</td>
<td>#D0</td>
<td>D0</td>
</tr>
<tr>
<td>D1</td>
<td>#D1</td>
<td>D1</td>
</tr>
<tr>
<td>D2</td>
<td>#D2</td>
<td>D2</td>
</tr>
<tr>
<td>D3</td>
<td>#D3</td>
<td>D3</td>
</tr>
<tr>
<td>D4</td>
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<td>D5</td>
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</tr>
<tr>
<td>D6</td>
<td>#D6</td>
<td>D6</td>
</tr>
<tr>
<td>D7</td>
<td>Clock</td>
<td>-</td>
</tr>
</tbody>
</table>

"CNT / TOGGLE" Switch - When the board is in "Internal Data" mode (described above), this switch will change the pattern that is being driven to the logic analyzer connectors.

COUNT MODE

<table>
<thead>
<tr>
<th>Samtec LA Connector (J1)</th>
<th>Samtec LA Connector (J1)</th>
<th>3M LA Connector (J2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(w/ Single-Ended Probe)</td>
<td>(w/ Differential Probe)</td>
<td></td>
</tr>
</tbody>
</table>
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<table>
<thead>
<tr>
<th>ODD</th>
<th>EVEN</th>
<th>ODD</th>
<th>EVEN</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xFF</td>
<td>0x00</td>
<td>0x00</td>
<td>0x00</td>
</tr>
<tr>
<td>0xFE</td>
<td>0x01</td>
<td>0x01</td>
<td>0x01</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x02</td>
<td>0xFD</td>
<td>0xFD</td>
<td>0xFD</td>
</tr>
<tr>
<td>0x01</td>
<td>0xFE</td>
<td>0xFE</td>
<td>0xFE</td>
</tr>
<tr>
<td>0x00</td>
<td>0xFF</td>
<td>0xFF</td>
<td>0xFF</td>
</tr>
</tbody>
</table>

TOGGLE MODE

Samtec LA Connector (J1)  Samtec LA Connector (J1)  3M LA Connector (J2)
(w/ Single-Ended Probe)   (w/ Differential Probe)

<table>
<thead>
<tr>
<th>ODD</th>
<th>EVEN</th>
<th>ODD</th>
<th>EVEN</th>
</tr>
</thead>
<tbody>
<tr>
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<td>0xAA</td>
<td>0x55</td>
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<tr>
<td>0x55</td>
<td>0xAA</td>
<td>0xAA</td>
<td>0xAA</td>
</tr>
</tbody>
</table>

"Up Arrow / Up and Down Arrow Switch" - When the board is in "Internal Data" mode (described above), this switch will change the clock edge on which data is sampled when the analyzer is in STATE mode. The switch changes the between "rising-edge clocking" and "both-edge clocking". All clocking on the Samtec logic analyzer connector (J1) occurs off of the ODD-Pod-Clock.

See Also “Reset Push Button” on page 20.

Reset Push Button

This push button (designated S2) will reset the board. Press the reset switch after connecting the cable to the Demo Board, or whenever you want to return the board to the reset condition.
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