

Agilent Technologies RF/IF-to-Digital Connected Solutions Bit Error Rate using the Advanced Design System

Application Note Number 1471

Introduction: Why Bit Error Rate and How Can Connected Solutions Help?

Designing and verifying designs to today's complex signal formats can present some interesting challenges. Designs can be verified in simulation and they can be verified after all of the hardware returns from fabrication – but an intermediate level of verification early in this design/fabrication cycle can be difficult to achieve due to the need for prototype hardware. Fabrication cycle time often results in inefficiencies while designers wait for hardware before performing verification testing. Add a couple of design iterations to this, and design time can really add up.

In particular, verifying Bit Error Rate (BER) can present a real challenge to RF engineers. RF engineers designing RF receivers may not have access to the baseband functionality required to perform coded Bit Error Rate measurements. This can present a barrier to verifying the performance of the RF hardware against a coded BER metric, which is frequently a key receiver design specification in today's digital communications signal formats.

Some receivers also have an Analog-to-Digital (A/D) converter at the output of the RF receiver, which adds additional complexity in both evaluating the RF performance after the Analog-to-Digital conversion process as well as evaluating BER for a mixed signal RF/digital signal path.

This application note discusses how Connected Solutions from Agilent Technologies can help for BER verification applications for RF/IF-to-digital receiver topologies.

This application note assumes that you have basic familiarity with digital communications concepts, with Advanced Design System, and with Agilent signal sources and logic analyzers. This application note expands upon the Connected Solutions fundamentals described in Application Note 1394, *Connected Simulation and Test Solution using the Advanced Design System*. Please refer to it (<http://literature.agilent.com/litweb/pdf/5988-6044EN.pdf>) for more information on the fundamentals of connecting Advanced Design System with Agilent signal sources and signal analyzers. Please contact your local Agilent Technologies representative for additional information. To find your local representative, visit www.agilent.com/find/assist. For more information about Advanced Design System, visit www.agilent.com/find/eesof.



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ADS Projects and Logic Analyzer Files In This Application

The ADS project, *RF_Digital_BER_AppNote_ADS2003C.zap*, and Logic Analyzer files described in this application note may be downloaded from http://eesof.tm.agilent.com/products/connected_solutions.html. Please use these project example files as a baseline to modify for your unique and specific applications.

Recommended hardware and software

This example project uses the following hardware and software:

- Advanced Design System (ADS) 2003C (E8900A/AN)
- Connection Manager (E5720A/AN)
- Communication Systems Designer E8850A/AN
- ADS 3GPP WCDMA Design Library E8875 A/AN (optional)
- ADS Wireless LAN Design Library E8874A/AN (optional)
- 16700 Logic Analysis System (16700A, 16700B, 16702A, or 16702B) with 167XX state/timing module
- E4438C ESG with option 002
- 89601A Vector Signal Analysis Software with options 100, AYA, 105 ; option B7N for 3GPP WCDMA; option B7R for WLAN

Note that ADS 2003C or later is required for this application.

Overview of Connected Solutions Bit Error Rate Measurements

Bit Error Rate, or BER, can be measured at various stages within a receiver design. Figure 1 shows a receiver example and the various locations for which BER measurements are meaningful.

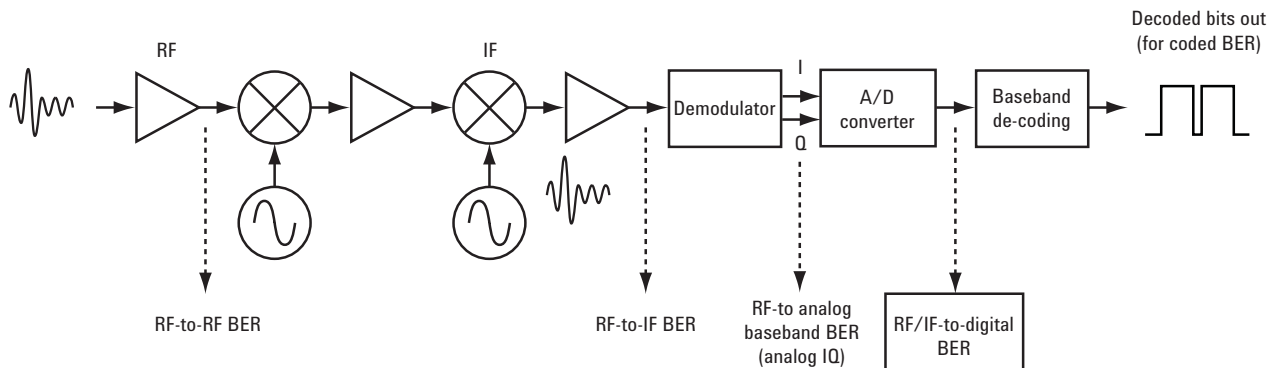


Figure 1. Various types of BER measurements.

This application note will discuss RF/IF-to-Digital BER measurements, where the receiver input is an RF or an IF signal, and the receiver output is digital (after an analog-to-digital converter).

Figure 1 shows a block labeled “Baseband De-Coding” after the analog-to-digital converter (A/D converter). Many digital communications signal formats include baseband functionality that impacts the coded bit-error-rate (BER) performance of an RF receiver.

As an example, a block diagram is shown in Figure 2 for a 3GPP WCDMA uplink signal. Note that this block diagram is for the uplink source, so the raw Data Traffic Channel (DTCH) bits on the upper-left corner would be used as the reference bits in a BER measurement involving an RF signal source and an RF receiver. Also note that baseband functionality, such as adding cyclic redundancy check (CRC) and tail bits, convolutional encoding, interleaving, frame segmenting, rate matching, and additional functionality are applied to the raw DTCH data bits before the I and Q signals are finally modulated onto an RF or IF carrier (not shown) to be used as the input signal into an RF receiver for BER testing.

On the receiver side, the inverse of this baseband functionality would be required to recover the raw DTCH data bits from the measured signal. Effectively, the measured signal would need to be de-scrambled, de-spread, de-interleaved, de-muxed, de-rate matched, de-segmented, de-interleaved, de-coded, and finally CRC and tail bits removed to recover the DTCH data bits from the RF or IF test signal into the RF receiver. Once recovered, the DTCH data bits can be compared to the original DTCH data bits transmitted to calculate the coded BER performance of the RF receiver.

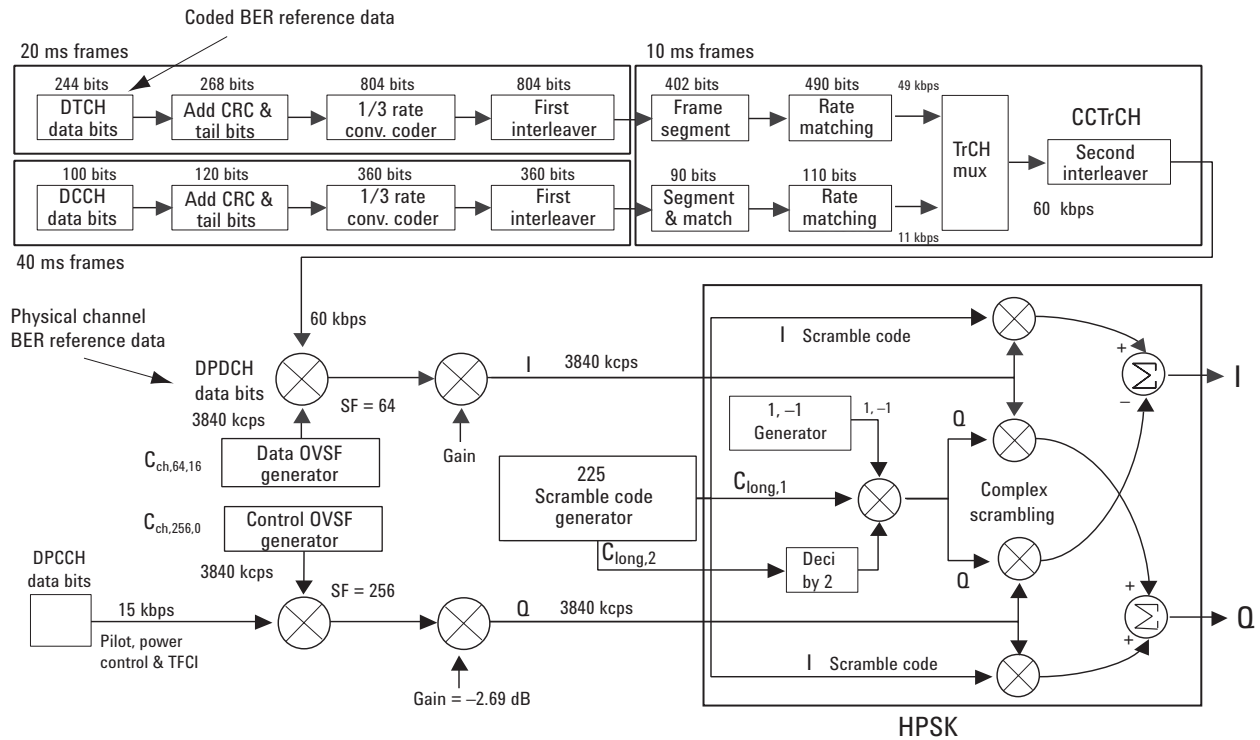


Figure 2. A block diagram for the 3GPP WCDMA uplink.

Coded BER measurements therefore require baseband functionality to post-process the signal to recover data bits from the RF or IF signal. But what if you are designing the RF portion of the receiver and don't have access to this baseband functionality? What if you would like to verify the RF BER performance of your receiver independent of the baseband section? Connected Solutions can help with this application by effectively emulating this baseband functionality so that coded BER measurements can be performed on RF hardware.

The fundamental concept in this approach is to use the Advanced Design System software, or ADS, to effectively extend the logic analyzer capabilities to perform the required baseband functionality in software, so that BER measurements can be performed. This is illustrated in Figure 3. The figure shows the conceptual process of downloading the ADS signal to the ESG Arbitrary Waveform Generator using the ADS-defined signal to stimulate the device-under-test (DUT), measuring the digital output from the A-to-D converter with the 16700 Series Logic Analyzer, and bringing measured Logic Analyzer data back into ADS to post-process the data with the baseband functionality in the ADS receiver to compute coded BER.

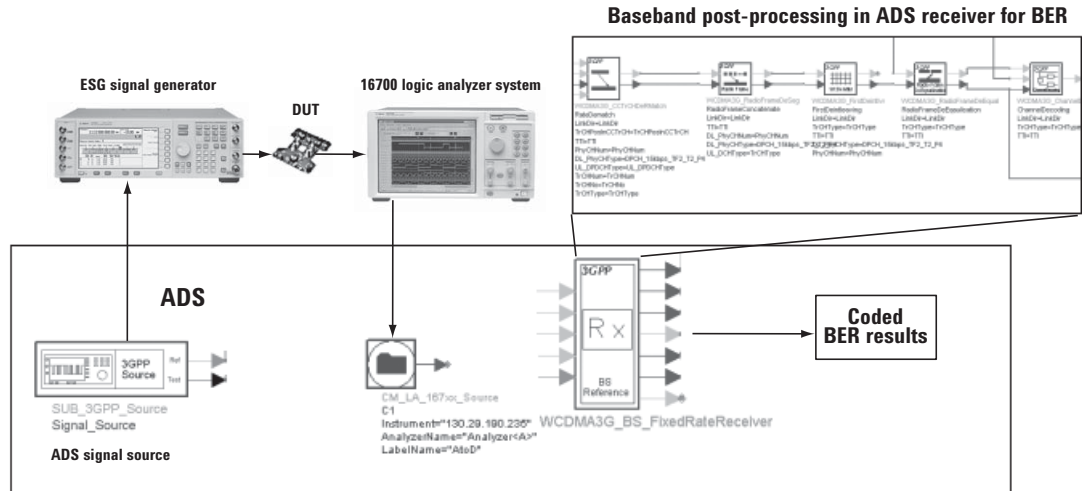


Figure 3. The connected solutions Bit Error Rate (BER) conceptual process.

Test setup and configuration

The general connected solutions test setup is shown in Figure 4. It consists of a laptop with ADS (upper right), 16700 Series Logic Analyzer (upper left), E4438C ESG for Connected Solutions signal generation (middle left), E4438C ESG for an Analog-to-Digital converter clock source (lower-right), and Analog-to-Digital DUT (sitting on top of ESG in the lower right).

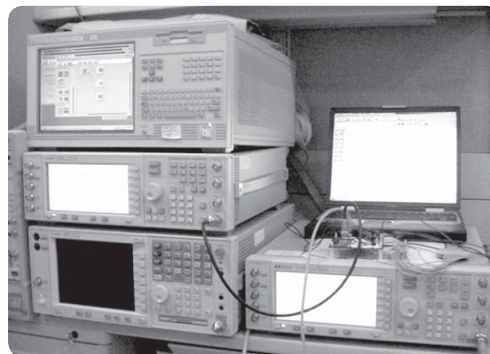


Figure 4. The connected solutions test setup.

IO Config and VISA Assistant should be run to establish LAN connectivity to the E4438C ESG and the 16700 Series Logic Analyzer. The ESG sink will also support a GPIB connection, so a LAN/GPIB gateway, USB-LAN converter, or direct GPIB connection can also be used after configuring with IO Config. The 16700 Series Logic Analyzer only supports a LAN connection.

The E4438C ESG has a rear panel BNC connector labeled "Event 1," which should be connected to the rear panel BNC connector on the 16702B, labeled "IN" with a BNC cable. This connection will allow the ADS data downloaded to the ESG arbitrary waveform generator to be time-synchronized with the measured data read from the Logic Analyzer, by enabling an Event1 marker pulse on the ESG and setting up the Logic Analyzer to trigger on the occurrence of that Event1 marker pulse.

Although not specifically shown, the digital outputs from the receiver's A/D should be connected to the Pod1 "flying leads" on the Logic Analyzer. Also, be sure to connect the black ground leads, or unpredictable results might be observed. When designing your own target for digital test and debug, many probing options exist, including connectors, "flying leads," and new connector-less methods. See www.agilent.com/find/logic for more information.

The connections and instrumentation settings for specific applications are shown in block diagrams for the WCDMA and WLAN case studies, and are discussed later in this application note.

Logic analyzer overview

The 16700 Series Logic Analysis system consists of a mainframe chassis and a series of plug-in cards for data acquisition. Logic analyzers capture data in either "state mode" (synchronously with the target device's clock) or in "timing mode" (asynchronous sampling). State mode is used for capturing digital signal data to ensure that signals are sampled during the stable period around the target clock edge (known as the setup-and-hold window). The appropriate choice of acquisition card for this application depends mainly on the data clock rate and number of bits. Agilent offers cards with state speeds of up to 1.5 Gb/sec. To choose the right model for your application, make sure the "state speed" of the card is at least as high as the target bus clock rate and channel count in each card is as high as the number of bits. In this application, we used a 16752B card, which is capable of synchronous sampling up to 200 Msa/sec with 68 channels. Another key specification to look for in an acquisition card is sample depth. The 16752B card can capture up to 32 million samples on each channel in state mode. The more depth, the longer the length of transmitted data you can capture and analyze in a single measurement.

Refer to Table 1 for a list of data acquisition cards and their operating specifications.

Model	Channels per card (Msa/sec)	Max state speed (State mode)	Max depth (State mode)
16710A	102	100	8K
16711A	102	100	32K
16712A	102	100	128K
16715A	68	167	2M
16716A	68	167	512K
16717A	68	333	2M
16740A	68	200	1M
16741A	68	200	4M
16742A	68	200	16M
16750B	68	400	4M
16751B	68	400	16M
16752B	68	400	32M
16753A	68	600	1M
16754A	68	600	4M
16755A	68	600	16M
16756A	68	600	32M
16760A	34	1500	64M

Table 1. Data acquisition cards and their key specifications.

16700 Series Logic Analyzers can also be configured with pattern generation cards and oscilloscope cards. The 16720A pattern generator card can also be used with ADS to generate test signals in baseband digital form.

Logic analyzer configuration

A special configuration file has been created for the 16700 Series Logic Analyzer to support this application. This configuration file, along with the ADS project (*RF_Digital_BER_AppNote_ADS2003C.zip*) can be obtained from http://eesof.tm.agilent.com/products/connected_solutions.html. The 16700 Series Logic Analyzer configuration file, *la_setup._A*, is located in the */data* subdirectory of the ADS project.

Create a directory on the Logic Analyzer by selecting File>New, typing a directory name (for example, BER), then clicking on the “Create Directory” tab on the Logic Analyzer. Place the configuration file from the */data* subdirectory of the *RF_Digital_BER_AppNote_ADS2003C_prj* ADS project into the Logic Analyzer directory which you just created. This can be done by either mapping the logic analyzer as a network drive, or using ftp.

To map the directory as a network drive:

1. On the logic analyzer, open the System Administration Window
2. Under the “Networking” tab, configure your network (IP Address, gateway, DNS Name Resolving, and so on)
3. Under the same tab, click “Share Analyzer Drive.”
4. Share the */logic* directory as share name “logic.”
5. From your PC’s Windows Explorer window, select Tools>Map Network Drive.
6. Map \\hostname\logic to a drive, where “hostname” is the network host name of the logic analyzer

To ftp:

1. Configure your logic analyzer on the network (refer to the section in this application note, “to map the directory as a network drive”).
2. From your system (if using DOS, reverse the slashes):
 - a. > cd /myadspath/data
 - b. > ftp hostname (where “hostname” is the name of the logic analyzer)
 - c. user: “ftp” or “anonymous”
 - d. password: any text at all
 - e. > bin
 - f. > prompt
 - g. > mput *la_setup._A*
 - h. > quit

Select the configuration file, and click on the “Load” tab on the Logic Analyzer to load the configuration file. This file sets up the Logic Analyzer to trigger the measurement on the occurrence of the Event1 marker pulse from the E4438C ESG. This enables the ADS-generated data to effectively be time-synchronized between ADS, ESG, and the Logic Analyzer, although some residual physical delay still exists in the measured data. The ADS WLAN and 3GPP WCDMA design library receivers can address these small residual delays for BER/PER measurements, however.

This configuration file is set up for a 14-bit A/D converter. To modify the number of bits measured, select “assign the appropriate channels on the Logic Analyzer” from the “Format” tab under the “Setup & Trigger” menu.

Logic analyzer simulation signal source and its configuration

A simulation signal source is created in ADS for the 16700 Series Logic Analyzer. This simulation signal source enables ADS to read the measured binary digital data directly from the Logic Analyzer's memory to use the measured data as a simulation signal source in ADS. An ASCII file-based transfer of the Logic Analyzer's data is also possible with existing elements in ADS, however, this memory-based simulation signal source has significant speed advantages over the file-based data transfer.

This ADS simulation signal source is shown in Figure 5, and is available in ADS 2003C or a later version of ADS. This Logic Analyzer simulation source requires a Connection Manager license to run it.

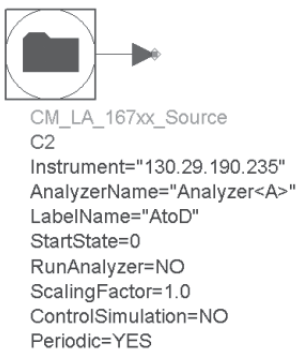


Figure 5. ADS simulation signal source for the 16700 Series Logic Analyzer.

The simulation signal source has the following parameters:

Instrument	used to specify the hostname or IP address of the Logic Analyzer
AnalyzerName	Logic Analyzer's module name inside the Logic Analysis system
LabelName	Label associated with the Logic Analyzer's measured data
StartState	Specifies which measurement sample to begin with when retrieving data from the Logic Analyzer's memory into ADS
RunAnalyzer	YES – performs a new measurement then retrieves the new measured data from Logic Analyzer upon ADS simulation; NO – retrieves existing measured data from Logic Analyzer memory upon ADS simulation
ScalingFactor	used to scale the logic analyzer data (represented as a "float" output) into a voltage. The scale factor may reflect the full-scale input range of the A/D and the number of bits output.
ControlSimulation	YES – the ADS simulation will run long enough to retrieve all of the data stored in the Logic Analyzer's memory; NO – only retrieves the amount of data stored in the Logic Analyzer's memory to correspond with the simulation length as determined by other sinks in the ADS schematic (may not retrieve all of the data in the Logic Analyzer's memory)
Periodic	NO – will pad measured data with zeros for the duration of the simulation length if the simulation length exceeds the amount of data stored in the Logic Analyzer's memory YES – will repeat the measured data for the duration of the simulation length if the simulation length exceeds the amount of data stored in the Logic Analyzer's memory

Connected Solutions BER Case Studies

Process overview

The general process of performing a Connected Solutions BER measurement is shown in Figure 6

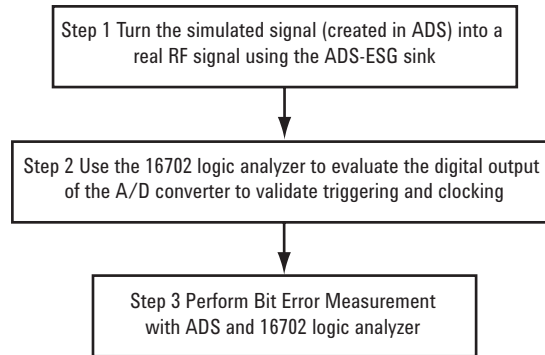


Figure 6. The connected solutions process flow.

The general process consists of performing an ADS simulation to download the simulated I and Q waveforms to the E4438C ESG arbitrary waveform generator. The ESG sink can be set up to enable the “Event 1” marker and to turn on the RF output on the ESG upon download.

After the 16700 Series Logic Analyzer is configured, the second step is to perform a measurement with the Logic Analyzer to ensure the A/D converter is clocking correctly and that the Logic Analyzer is reading the digital outputs from the A/D converter.

The last step is to run the ADS simulation which contains the 16700 Series Logic Analyzer simulation signal source and ADS design library receiver to post-process the measured data and compute BER.

Typically, it is useful to initially start this process with a minimal amount of data to establish and validate the test setup. After it is validated, an actual BER measurement can be performed with the desired amount of data downloaded from ADS to the ESG arbitrary waveform generator, and read from the 16700 Series Logic Analyzer to ADS.

Each of these steps is covered in detail in the following case study sections.

3GPP WCDMA case study

This case study is effectively an extension of the BER example shown in application note 1394, <http://literature.agilent.com/litweb/pdf/5988-6044EN.pdf>, except here the device-under-test output is a digital signal measured with the 16700 Series Logic Analyzer. The example device-under-test is a 14-bit analog-to-digital converter, which will convert the modulated WCDMA IF signal to a 14-bit digital output. The analog-to-digital converter is used to illustrate the concept, and typically would be replaced with a receiver that contains an analog-to-digital converter at its output.

A picture of the test setup is shown in Figure 7.

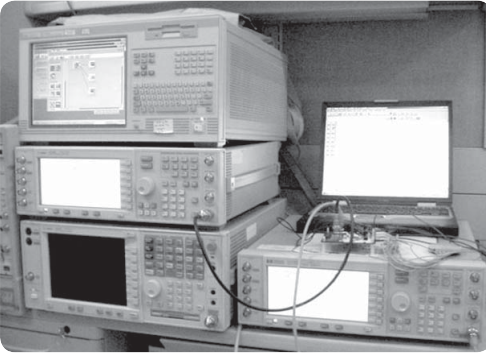


Figure 7. WCDMA connected solutions test setup.

ADS is installed on the PC laptop, which is connected to the E4438C ESG (middle left) and 16700 Series Logic Analyzer (upper left) using a LAN connection. The rear-panel Event1 marker output on this E4438C ESG is connected to the “Port In” BNC rear-panel input on the Logic Analyzer. The RF output of this E4438C ESG is connected to the analog input on the Analog-to-Digital evaluation board. The second E4438C ESG (lower-right) is being used to provide a CW clock signal and is connected to the clock input on the Analog-to-Digital evaluation board. (Note: this second ESG is optional, and is being used since there is not a system-clock available). It is not critical that an E4438C ESG is used to provide this clock signal for this application.

A block diagram of the test setup is shown in Figure 8.

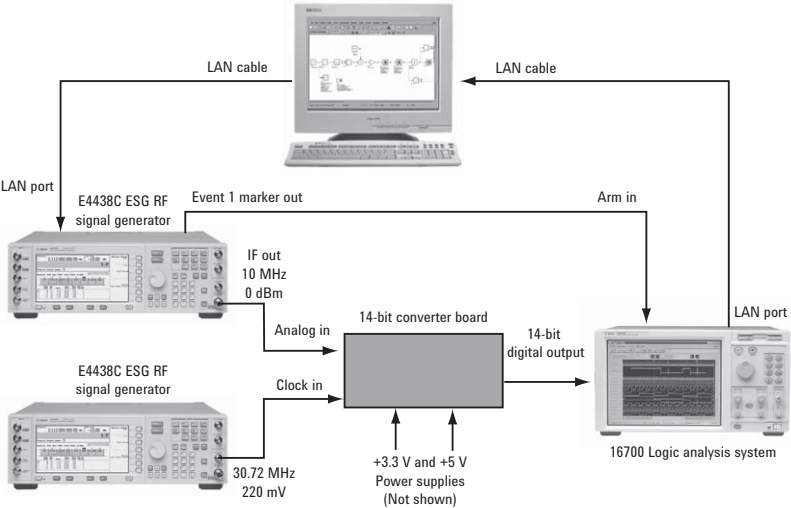


Figure 8. A block diagram of the 3GPP WCDMA BER test setup.

To configure your test setup for WCDMA BER, connect your PC and test equipment as shown in Figure 8. Also ensure that the 16700 Series Logic Analyzer configuration file, *la_setup__A*, has been loaded on the Logic Analyzer, as discussed previously.

The main steps for running the test follow.

Step 1. Download the ADS Waveform to the ESG Arb

First, open the design file *ADS_E4438C_Download_WCDMA.dsn*, which is shown in Figure 9. This schematic was created by copying and modifying the *WCDMA3G_BS_Rx_prj* project, which is included with the ADS 3GPP WCDMA design library (Agilent Part Number E8875A/AN).

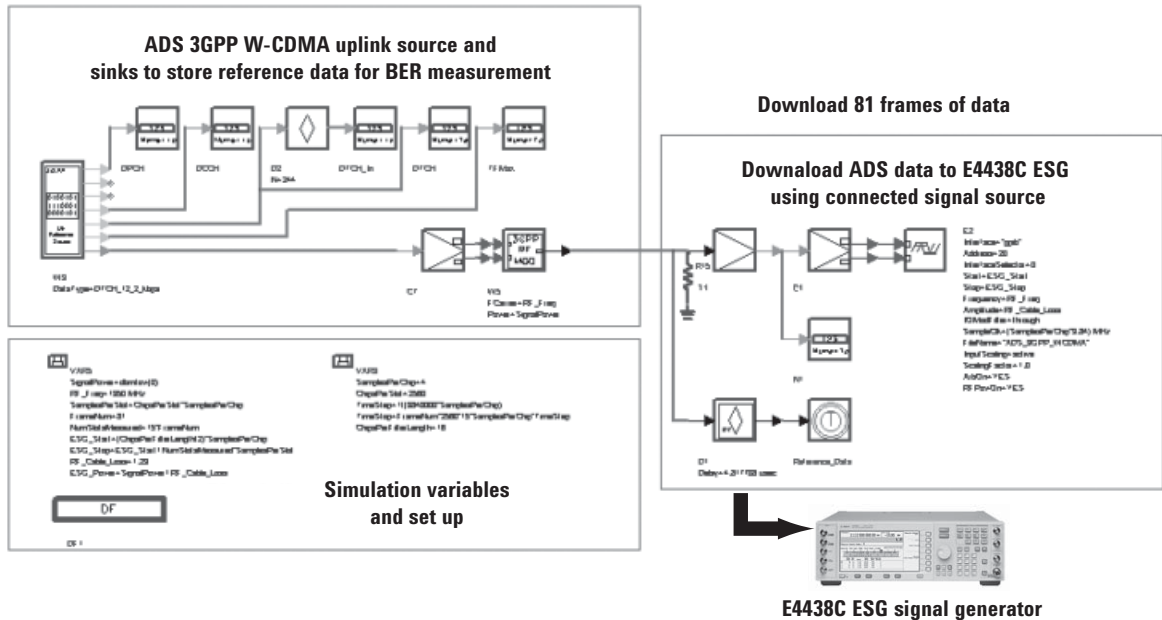


Figure 9. Downloading the ADS waveform to the ESG arbitrary waveform generator.

This schematic contains the ADS WCDMA simulation signal source (far left), and the E4438C ESG sink (far right) to download the simulated I and Q waveforms from ADS to the E4438C ESG Arbitrary Waveform Generator (Arb). The Start and Stop parameters on the ESG sink are set up to download 81 (10 mS) radio frames of data to the ESG Arb at four samples per chip

This does not fill the ESG’s Arb memory (32 Msamples with option 002), and the Stop parameter on the ESG sink can be later adjusted as needed for the given application. Specifically, 81 frames are being download which corresponds to 81 frames * 15 time-slots/frame * 2560 chips/timeslot * 4 samples/chip = 12,441,600 samples of ADS data being downloaded to the ESG Arb. (Note: 1GB of PC virtual memory is recommended to download this large amount of data to the ESG Arb.)

It can be useful to perform this BER measurement with less data initially, to speed this for debugging purposes. If desired, the variable “FrameNum” in the VAR5 variable block can be changed from 81 frames to 3 frames to facilitate this.

Note: There are five “Numeric Sinks” connected to various outputs on the ADS WCDMA signal source. These sinks will record the reference data bits into an ADS simulation dataset, where they will later be read into the ADS receiver to be compared with the measured data bits (recovered from the Logic Analyzer signal) to compute BER.

Perform the simulation to download the I and Q waveforms to the ESG Arbitrary Waveform Generator. You should see a message “Loading external file” on the front panel screen of the E4438C ESG along with a percent complete. Be sure to wait until the download is 100% complete.

Downloading the ADS data to the ESG arbitrary waveform generator took approximately 19 minutes for the 81 frames of data at 4 samples per chip on a 1.7 GHz PC with 512MB of RAM.

The ADS-created Arb signal, if not already active, is activated by pressing the following keys on the ESG front panel:

Local > Mode > Arb Waveform Generator > Dual Arb > Select Waveform> “ARBI: ADS_3GPP_WCDMA”

Note: *ADS_3GPP_WCDMA* is the name specified as the *FileName* parameter on the ADS-ESG sink.

Press the **Mod On/Off** and **RF On/Off** on the ESG front panel to turn on the RF output signal.

An event marker, if not already turned on, should be turned on to mark the beginning of the Arb sweep. Press the following keys on the ESG front panel:

Local > Mode > Arb Waveform Generator > Dual Arb >Waveform Segments>Waveform Utilities>Set Markers> “Set Marker On First Point”

This activates a pulse on the rear-panel Event1 marker BNC output to indicate the first sample point of the ESG Arb sweep, or the first sample point of the ADS simulation data downloaded to the Arb. The Logic Analyzer can then be set to trigger its measurement on the occurrence of this Event1 marker pulse to effectively time-synchronize the data between ADS, ESG, and the Logic Analyzer.

Step 2. Perform the Logic Analyzer Measurement

While not required for the actual BER measurement, it is often useful to perform a measurement with the Logic Analyzer to verify proper triggering setup and operation before simulating the ADS schematic for the actual BER measurement.

Set the Acquisition Depth on the 16700 Series Logic Analyzer to 32Msamples by double clicking on the Analyzer<A> icon and then clicking on the Acquisition Depth pull-down menu. For this application example, 81 frames of WCDMA data had been downloaded from ADS to the E4438C ESG.

To calculate the Acquisition Depth required to capture all of the data downloaded to the ESG Arb with an Analog-to-Digital clock rate of 30.72 MHz , or 8X over-sampling of the 3.84 MCps WCDMA data:

$81 \text{ frames} * 15 \text{ slots/frame} * 2560 \text{ chips/slot} * 8 \text{ samples/chip (A/D clock @ 30.72 MHz)} = 24.8832 \text{ Msamples of Acquisition Depth needed.}$

The 16752B card can capture up to 32 million samples on each channel.

To perform the Logic Analyzer measurement, load the configuration file provided (if not already loaded), and verify that you have reasonable data capture by performing the following steps:

1. Click the “Run” button (looks like the Play button on a CD Player)
2. Open the Chart window – click Window->Slot A:Analyzer<A>->Chart<1>. If you don’t have a Chart window, open the “Workspace” window, find the “Chart” tool in the palette on the left-hand side of the window, drag it onto the workspace, and drop it on the logic analyzer icon. Then open the window by double-clicking on its icon.
3. Look at the waveform. If it looks like something you would expect, your settings are probably good. In Two’s Complement (signed) notation, a 14-bit number can range from –8192 to 8191. Depending on the settings of your A/D converter you may need to adjust the amplitude of the signal from the ESG. For the best dynamic range, you want the highest amplitude possible without saturating the 14 bits.

Step 3. Perform the BER Measurement

Open the design file *Read_16702LA_ADS_Measure_WCDMABER.dsn*, as shown in Figure 10.

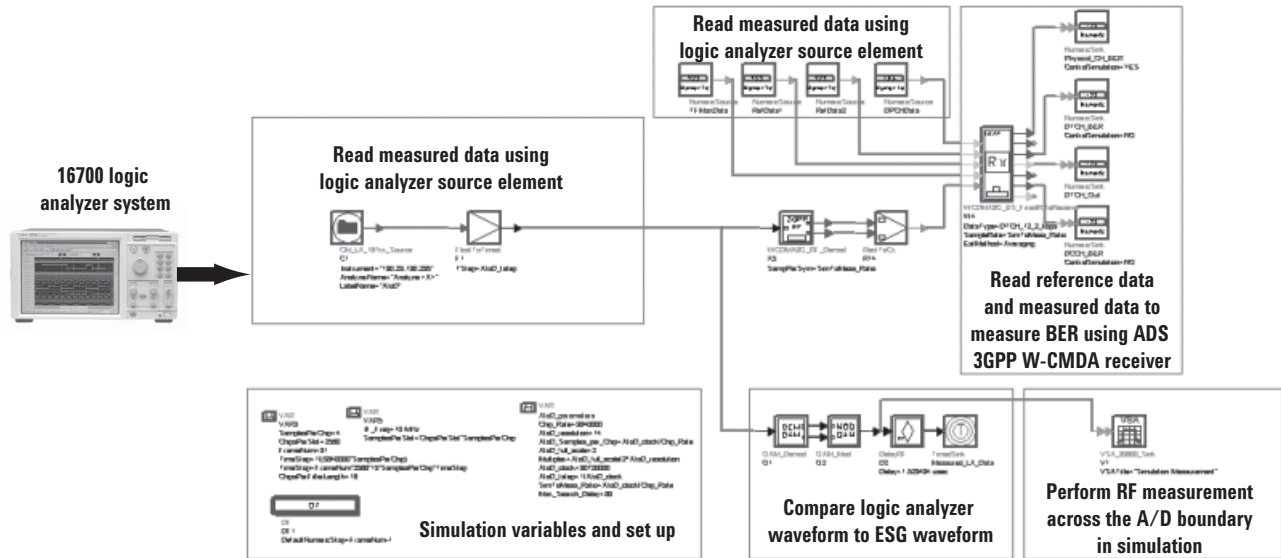


Figure 10. Performing the BER measurement.

This schematic contains the Logic Analyzer simulation signal source (far left), which reads the data from the Logic Analyzer’s memory and sources the measured data into the ADS WCDMA design library receiver (far right) to perform the baseband post-processing (illustrated in Figures 2 and 3) to compute BER. Notice that there are four “Numeric Source” elements also connected to the input of the ADS WCDMA receiver. The “Numeric Source” elements read the reference data bits previously stored by the Numeric sinks *ADS_E4438C_Download_WCDMA.dsn*, to use as the reference data for the BER measurement.

Also notice that there are two sinks connected in the lower right-hand corner of the schematic. The timed sink, labeled *Measured_LA_Data*, allows the measured data from the Logic Analyzer to be overlaid and compared to the ADS waveform that was downloaded to the ESG Arb. The (optional) *VSA_89600_Sink* is a Vector Analyzer simulation measurement. If the 89600 software is installed on the PC and licensed, then performing a simulation with this element will allow RF-type measurements to be performed (for example, EVM, spectrum) on the digital data measured with the Logic Analyzer.

For example, Figure 11 shows an RF measurement, performed with the *VSA_89600_Sink* in ADS on the measured digital data from the Logic Analyzer. Note that this can be very useful for evaluating RF performance across the analog-to-digital boundary in a receiver design, allowing the RF systems engineer to evaluate metrics such as Error Vector Magnitude (EVM) and spectral performance on the digital data measured with the Logic Analyzer. This effectively provides a method of providing demodulation capability for the 16700 Series Logic Analyzer by connecting it to ADS and the 89600 VSA simulation software.

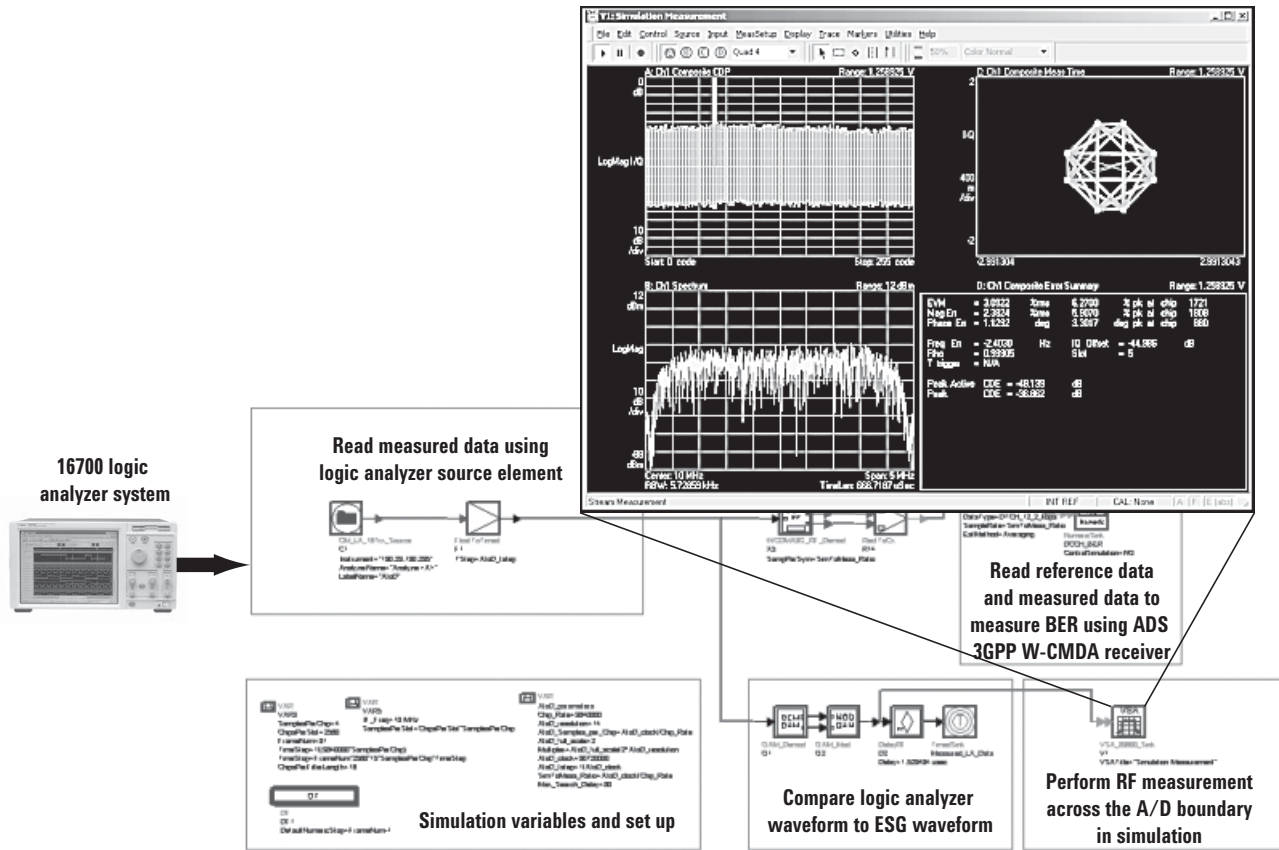


Figure 11. An example RF measurement on digital data using the VSA_89600_Sink Element in ADS. Measured EVM= 3.09%.

Modify the following parameters on the LA_16700_Source to reflect your 16702 Logic Analyzer setup:

- Instrument
- AnalyzerName
- LabelName

If performing the RF measurement shown in figure10, then select **MeasSetup > DemodProperties > Preset to Default**> Uplink from the 89600 VSA simulation measurement to pre-configure the measurement for a WCDMA uplink signal.

To perform the BER measurement, de-activate the VSA_89600_Sink by clicking on the activate/de-activate icon.

The VAR3 variable block contains a variable named "FrameNum," which by default is set to 81. This will allow 80 frames of data to be considered for the BER measurement. Modify the "FrameNum" variable, as needed, to reflect your application. Perform the simulation to start the BER measurement. When finished, open the data display *Read_16702LA_ADS_Measure_WCDMABER.dds*.

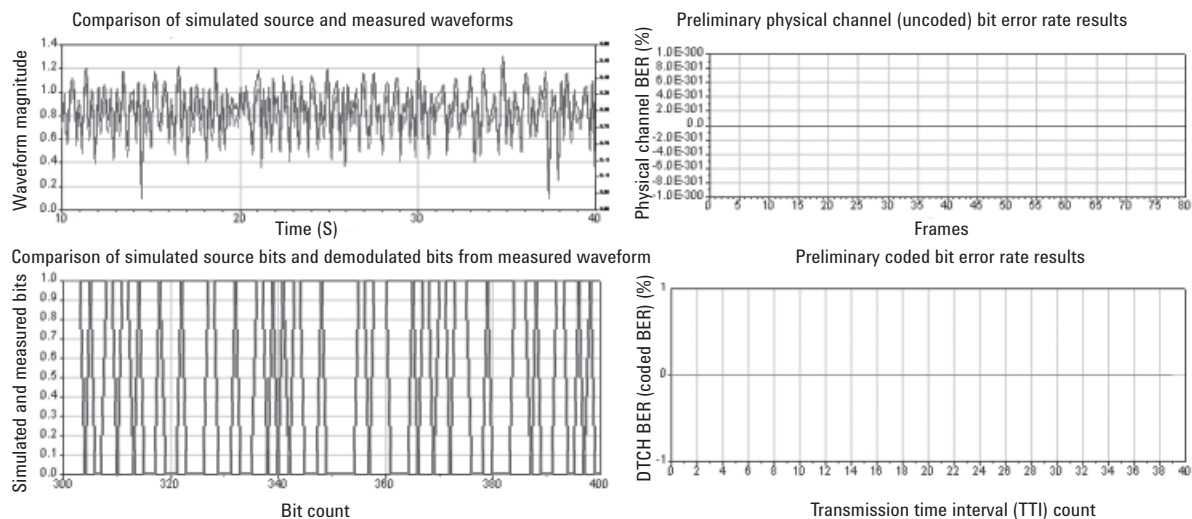


Figure 12. BER results using ADS with the Logic Analyzer.

The upper left-hand plot shows the waveform downloaded from ADS to the E4438C ESG Arb overlaid with the measured waveform read from the 16700 Series Logic Analyzer into ADS. The lower left-hand plot shows the reference data bits from the ADS simulation signal source (reference bits) overlaid with the output bits recovered by the ADS receiver (test bits) by post-processing the measured signal read from the 16700 Series Logic Analyzer. For the sample size shown, one can see that the reference bits and test bits are identical, indicating that the measured coded BER would be 0% for this small sample size. The physical uncoded BER results as a function of the number of frames is shown on the upper-right, while the coded BER results as a function of the Transmission Time Interval (TTI) is shown on the lower-right. For the 12.2kbps Data Traffic Channel (DTCH) data rate used in this example, there are two 10mS radio frames for each TTI, resulting in 40 TTI for the 80 frames measured.

Reading the measured data from the 16700 Series Logic Analyzer memory to compute BER in the ADS BER simulation took approximately 19.4 minutes for the 80 frames of data at 4 samples per chip on a 1.7 GHz PC with 512M of RAM. The 19.4 minutes does not include the simulation time to download the ADS waveform to the ESG.

WLAN 802.11a case study

This example is an extension of the previous WCDMA case study, in which an 802.11a WLAN signal is now input into the device-under-test (14-bit analog-to-digital converter) instead of a WCDMA signal. The 14-bit analog-to-digital converter is used to illustrate the concept, and typically would be replaced with a receiver that contains an analog-to-digital converter at its output.

The test setup is the same as the setup shown for the previous WCDMA case study. (Refer to Figure 7.)

ADS is installed on the PC laptop, which is connected to the E4438C ESG (middle left) and 16700 Series Logic Analyzer (upper left) using a LAN connection. The rear-panel Event1 marker output on this E4438C ESG is connected to the Port In BNC rear-panel input on the 16700 Series Logic Analyzer. The RF output of this E4438C ESG is connected to the analog input on the Analog-to-Digital evaluation board. The second E4438C ESG (lower right) is used to provide a CW clock signal and is connected to the clock input on the Analog-to-Digital evaluation board. (Note: This second ESG is optional, and is used here because a system clock is not available). It is not critical that an E4438C ESG is used to provide this clock signal for this application.

A block diagram of the test setup is shown in Figure 13.

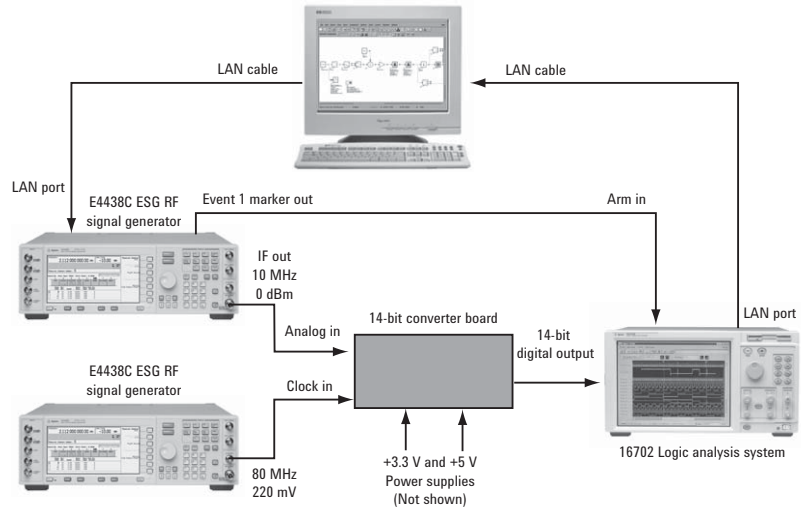


Figure 13. A block diagram of the WLAN BER test setup.

To configure your test setup for WLAN BER, connect your PC and test equipment as shown in Figure 13, and ensure that the 16702 Logic Analyzer configuration file, *la_setup._A* has been loaded on the Logic Analyzer, as discussed previously.

Step 1. Download the ADS Waveform to the ESG Arb

To begin the process, open the design file *ADS_E4438C_Download_WLAN.dsn*, which is shown in Figure 14. This schematic utilizes the ADS WLAN design library (E8874A/AN).

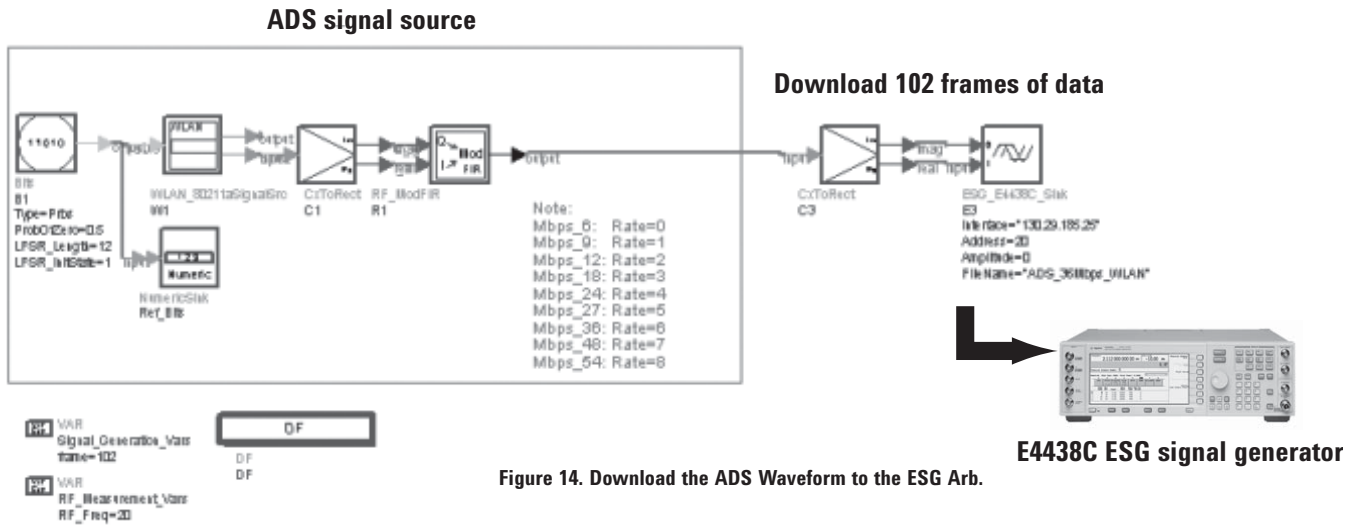


Figure 14. Download the ADS Waveform to the ESG Arb.

This schematic contains the ADS WLAN simulation signal source (far left), and the E4438C ESG sink (far right) to download the simulated I and Q waveforms from ADS to the E4438C ESG Arbitrary Waveform Generator (Arb). The Start and Stop parameters on the ESG sink are set up to download 102 bursts of WLAN 802.11a data at 36 Mbps. This does not fill the ESG's Arb memory (32Msamples with option 002), and the Stop parameter on the ESG sink can be later adjusted as needed for the given application. Specifically, 102 bursts are being downloaded, which corresponds to 2,056,320 samples of ADS data being downloaded to the ESG Arb. Note: 1GB of virtual memory is recommended on the PC to download this large amount of data to the ESG Arb.

It may be useful to perform this BER measurement with less data initially, to try this process in a more timely manner or for debugging purposes. If desired, the variable "Frame" in the "Signal_Generation_Vars" variable block can be changed from 100 frames to 5 frames to facilitate this.

Note that there is a "Numeric Sink" named "Ref_Bits" connected to various output of the Prbs bit source. This sink will record the reference data bits into an ADS simulation dataset, where it will later be read into the ADS receiver to be compared with the measured data bits (recovered from the Logic Analyzer signal) to compute BER.

Perform the simulation to download the I and Q waveforms to the ESG Arbitrary Waveform Generator. You should see a message "Loading external file" on the front panel screen of the E4438C ESG along with a percent complete. Please wait until the download is 100% complete.

Downloading the ADS data to the ESG arbitrary waveform generator took approximately 4 minutes for the 102 bursts of data on a 1.7 GHz PC with 512M of RAM.

The ADS-created Arb signal, if not already active, is activated by pressing the following keys on the ESG front panel:

Local >Mode >Arb Waveform Generator >Dual Arb >Select Waveform>"ADS_36Mbps_WLAN"

Note: *ADS_36Mbps_WLAN* is the name specified as the *FileName* parameter on the ADS-ESG sink.

Then press the **Mod On/Off** and **RF On/Off** on the ESG front panel to turn on the RF output signal.

An event marker, if not already turned on, should be turned on to mark the beginning of the Arb sweep by pressing the following keys on the ESG front panel:

Local >Mode >Arb Waveform Generator >Dual Arb >Waveform Segments>Waveform Utilities> Set Markers> "Set Marker On First Point"

This activates a pulse on the rear-panel Event1 marker BNC output to indicate the first sample point of the ESG Arb sweep, or the first sample point of the ADS simulation data downloaded to the Arb. The Logic Analyzer can then be set to trigger its measurement on the occurrence of this Event1 marker pulse to effectively time-synchronize the data between ADS, ESG, and the Logic Analyzer.

Step 2. Perform the Logic Analyzer Measurement

While not required for the actual BER measurement, it is often useful to perform a measurement with the Logic Analyzer to verify proper triggering setup and operation before simulating the ADS schematic for the actual BER measurement.

Set the Acquisition Depth on the Logic Analyzer to 32 Msamples by double-clicking on the Analyzer<A> icon and then clicking on the Acquisition Depth pull-down menu. For this application example, 102 bursts of WLAN data was downloaded from ADS to the E4438C ESG.

To calculate the Acquisition Depth required to capture all of the data downloaded to the ESG Arb with an Analog-to-Digital clock rate of 80 MHz , or 4X over-sampling of the 20 MHz subcarrier bandwidth:

102 Frames * (55 Symbols * 4 μSec/Symbol+20 μSec+8 μSec) * 80 MHz = 2.0368 MSamples of Acquisition Depth needed. The 16752B card can capture up to 64 million samples on each channel.

Notes:

- The 4 μSec/Symbol is dependent on the data rate.
- The 20 μSec is for the preamble + signal field
- The 8 μSec in the above equation is the Idle time from the number of Idle symbols. The number of Idle symbols can be modified in the "Signal_Generation_Vars" VAR block in *ADS_E4438C_Download_WLAN.dsn*. For this example, it is set to $2 * 1.25 * 2^8 * (1/80\text{MHz}) = 8 \mu\text{Sec}$

To perform the Logic Analyzer measurement, load the configuration file provided (if not already loaded), and verify that you have reasonable data capture by performing the following steps:

1. Click the "Run" button (looks like the Play button on a CD Player)
2. Open the Chart window – click **Window->Slot A:Analyzer<A>->Chart<1>**. If you don't have a Chart window, open the "Workspace" window, find the "Chart" tool in the palette on the left-hand side of the window, drag it onto the workspace, and drop it on the logic analyzer icon. Then open the window by double clicking on its icon.
3. Look at the waveform. If it looks like something you would expect, your settings are probably good. In Two's Complement (signed) notation, a 14-bit number can range from -8192 to 8191. Depending on the settings of your A/D converter you may need to adjust the amplitude of the signal from the ESG. For the best dynamic range, you want the highest amplitude possible without saturating the 14 bits.

Step 3. Perform the BER Measurement

Open the design file *Read_16702LA_ADS_Measure_WLANBER.dsn*, as shown in Figure 15.

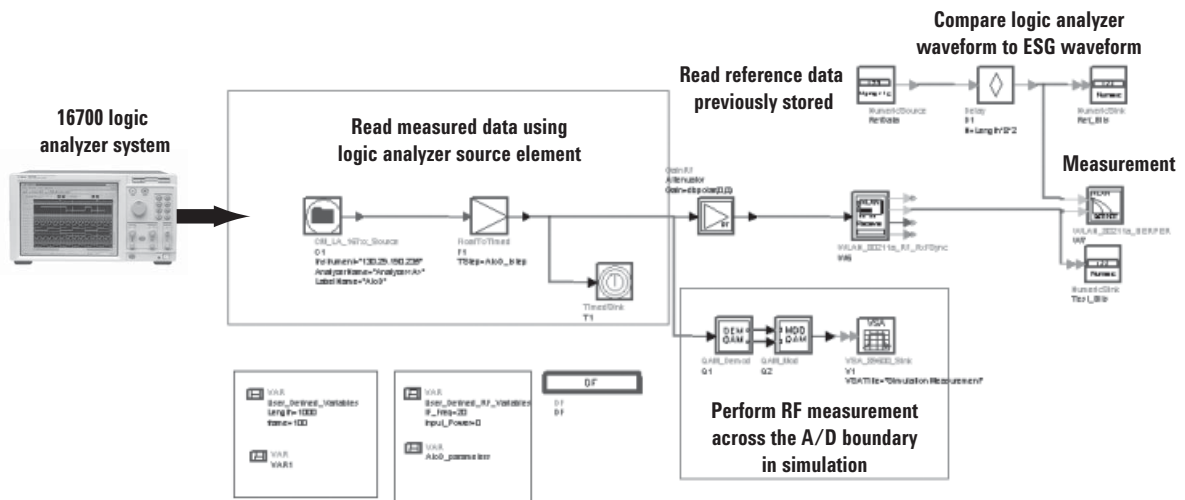


Figure 15. Performing the RF measurement and the BER/PER measurement.

This schematic contains the Logic Analyzer simulation signal source (far left), which reads the data from the Logic Analyzer’s memory and sources the measured data into the ADS WLAN design library receiver (far right) to perform the baseband post-processing (illustrated in Figures 2 and 3 for WCDMA) to compute BER. Notice that there is a “Numeric Source” element also connected to the input of the ADS WLAN BER measurement. The “Numeric Source” elements read the reference data bits previously stored by the Numeric sinks *ADS_E4438C_Download_WLAN.dsn*, to use as the reference data for the BER measurement.

Also notice that there are two numeric sinks connected on the right-hand side of the schematic. The sink labeled “Test_Bits” allows the measured data from the Logic Analyzer to be overlaid and compared to the ADS waveform which was downloaded to the ESG Arb (sink labeled “Ref_Bits”). The (optional) *VSA_89600_Sink* is a Vector Analyzer simulation measurement. If the 89600 software is installed on the PC and licensed, then performing a simulation with this element will allow RF-type measurements to be performed (for example, EVM, spectrum) on the digital data measured with the Logic Analyzer.

For example, Figure 16 shows an example of an RF measurement performed with the *VSA_89600_Sink* in ADS on the measured digital data from the Logic Analyzer. Note: This can be very useful in evaluating RF performance across the analog-to-digital boundary in a receiver design, allowing the RF systems engineer to evaluate metrics such as Error Vector Magnitude (EVM) and spectral performance on the digital data measured with the Logic Analyzer. This effectively provides a method of providing demodulation capability for the Logic Analyzer by connecting it to ADS and the 89600 VSA simulation software.

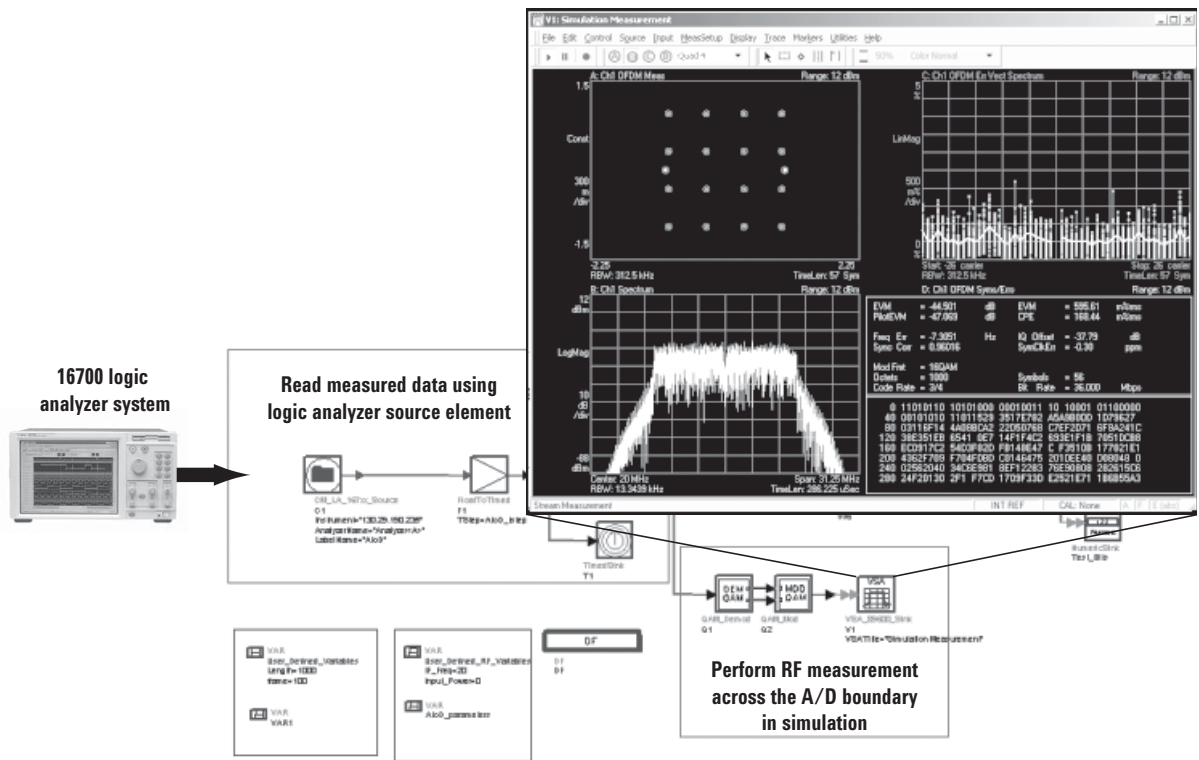


Figure 16. An example of performing an RF measurement on digital data using the *VSA_89600_Sink* Element in ADS. Measured EVM = 0.59%.

Modify the following parameters on the LA_16700_Source to reflect your 16702 Logic Analyzer setup:

- Instrument
- AnalyzerName
- LabelName

If you are performing the RF measurement shown in Figure15, then select **MeasSetup>DemodProperties>Preset to Standard>IEEE802.11a/g OFDM** from the 89600 VSA simulation measurement to pre-configure the measurement for a WLAN uplink signal.

To perform the BER measurement, de-activate the VSA_89600_Sink by clicking on the activate/de-activate icon.

The “user_Defined_Variables” variable block contains a variable named “Frame,” which by default is set to 100. This will allow 100 bursts of data to be considered for the BER measurement. Modify the “Frame” variable as needed to reflect your application. Perform the simulation to start the BER measurement. When finished, open the data display *Read_16702LA_ADS_Measure_WLANBER.dds*.

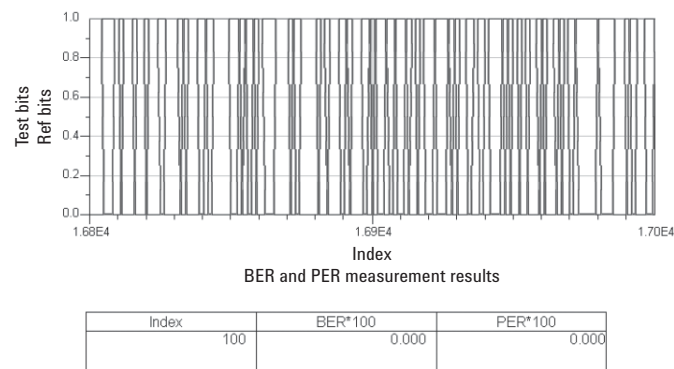


Figure 17. BER results using ADS with the Logic Analyzer.

The plot at the top shows the reference data bits from the ADS simulation signal source (reference bits) overlaid with the output bits recovered by the ADS receiver (test bits) by post-processing the measured signal read from the Logic Analyzer. For the sample size shown, one can see that the reference bits and test bits are identical, indicating that the measured coded BER would be 0% for this small sample size. Note that the table at the bottom shows the measured BER and Packet-Error-Rate (PER) is 0% for the 100 bursts measured.

Reading the measured data from the Logic Analyzer memory to compute BER in the ADS BER simulation took approximately 7 minutes for the 100 bursts of data on a 1.7 GHz PC with 512 M of RAM. The 7 minutes does not include the simulation time to download the ADS waveform to the ESG.

A similar process was followed using 20 bursts of data and adjusting the RF power level on the E4438C ESG signal generator to generate a waterfall curve as shown below in Figure 18. A limited number of bursts were used (only 20 bursts) at each power level for illustration.

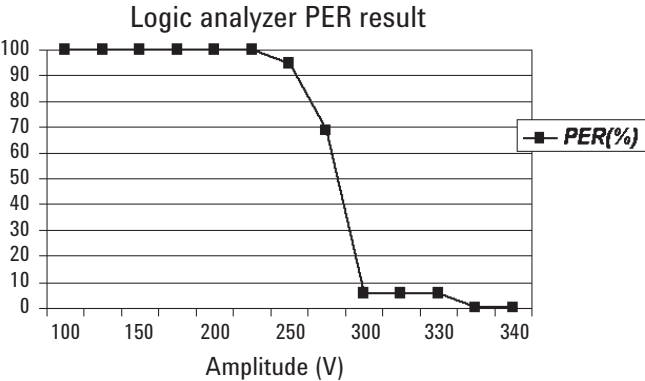


Figure 18. Waterfall BER results using ADS with the 16702B Logic Analyzer, setting ESG to various power levels

Summary

This application note shows how mixed-signal RF/Digital BER measurements can be performed using Advanced Design System, the E4438C ESG, and the 16700 Series Logic Analyzer connected solution. These measurements are useful for RF receiver applications where an Analog-to-Digital converter is used at the receiver's output. ADS design libraries (for example, WCDMA, WLAN) help extend the capabilities of the Logic Analyzer by providing the baseband post-processing needed to perform coded BER and PER measurements. In addition, RF measurements such as EVM and spectral measurements can be performed on digital signals at the output of an Analog-to-Digital converter by connecting the Logic Analyzer to ADS, and running the 89600 VSA simulation software from within ADS.

Product Information

ADS products and wireless design libraries:

www.agilent.com/find/eesof

Logic analyzers:

<http://www.agilent.com/find/logic>

Agilent solution brochures:

Wireless 2G/3G Solutions:

www.agilent.com/find/3G

Solutions for Designing and Manufacturing Base Transceiver Stations and Their Components:

www.agilent.com/find/basestationtest

Solutions for Designing and Manufacturing Wireless Appliances:

www.agilent.com/find/wirelessdesign

Application Notes:

Connected Simulation and Test Solutions using the Advanced Design System

<http://literature.agilent.com/litweb/pdf/5988-6044EN.pdf>

ADS Application Information/Papers/Application Notes:

<http://contact.tm.agilent.com/tmo/eesof/applications>

3G Application Notes:

www.agilent.com/find/3G

ADS Wireless Networking Seminar Papers and ADS Projects:

http://contact.tm.agilent.com/tmo/eesof/news/wireless_networking.html

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Acronyms and Abbreviations used in this Application Note

3GPP	Third Generation Partnership Project
ADS	Advanced Design System
Arb	ESG Signal Generator Arbitrary Waveform Generator
BER	Bit Error Rate
CRC	Cyclic Redundancy Check
CW	Continuous Wave
DAC, D/A	Digital to Analog Converter
DSP	Digital Signal Processing
DTCH	Data Traffic Channel
DUT	Device Under Test
ESG	E4438C ESG Signal Generator
EVM	Error Vector Magnitude
VSA	Vector Signal Analyzer
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
LA	Logic Analyzer

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