Keysight Technologies

FPGA Circuit Design: Overcoming Power-Related Challenges

Application Note

KEYSIGHT TECHNOLOGIES

Introduction

When you are designing, field-programmable gate array (FPGA) circuits, it is important to pay attention to power issues so you can create a final product that is defect free and optimized under all possible operating conditions. FPGA circuit power considerations can be broken into two categories: FPGA circuit power-on requirements and FPGA circuit power analysis. This application note explores these two areas, discusses the challenges you are likely to face and offers solutions that will help you overcome them.

Powering on an FPGA circuit

FPGA circuits have multiple power inputs. To optimize current draw at turn on, to prevent latch-up, or to prevent permanent circuit damage, these power inputs require precise sequencing and/or correctly timed voltage slew rates. Power turn-on can become even more complicated if the FPGA circuit consists of one or more application-specific integrated circuits (ASICs) or configuration devices that communicate with the FPGA. In this situation, you may want to sequence the power to the other devices to come on before or after the FPGA has fully configured itself. This is necessary to prevent glitches at turn-on and to reduce turn-on power consumption.

FPGA circuit power analysis

How much power an FPGA circuit consumes depends on a number of factors and is highly dependent on its design. These factors include such things as how well the hardware-defined language (HDL) used to configure the FPGA was optimized, the interfaces that are connected to the I/O, and the frequency of the I/O traffic. You need to test power consumption for the FPGA circuit under all possible operating conditions to determine the maximum amount of power a supply design must deliver. You need to capture accurate profiles of high-current spikes and time stamp them to identify at what point in operation they occurred. You may have to continually optimize your FPGA designs to fit product designs that have limited power resources available (for example, battery-powered devices). FPGA circuit power analysis is also important for thermal management of the design. Overheating can damage silicon devices, and you may need to adjust the size of your overall product design to allow larger surface areas or more airflow for cooling.

Problems with present solutions

Power-on solutions

Engineers use two common methods to power FPGA circuits: fixed regulator circuits and single-output programmable power supplies. Fixed regulator circuits employ inhibit features for proper sequencing and have RC networks to achieve proper slew rates. This method makes little sense as a solution early in the design process because it is inflexible. Such a solution leaves FPGA circuit designers little room to optimize turn-on power consumption through fine tuning of sequencing and slew rates within the FPGA's allowable ranges. If the FPGA circuit is experiencing a problem during power-on, such as latch-up, the regulator circuit provides little insight into the problem to assist with debugging.

Programmable power supplies are an alternative solution to avoid the headaches of fixed regulator circuits early in the design process. The programming required to set up strict turn-on time sequencing and slew rates for FPGA circuits on a non-real-time operating system such as Windows can be difficult or impossible without some type of hardware support.

Typically, as your company's projects evolve, your FPGA circuit design goals change, which can be a problem if you are using programmable power supplies. If your timing requirements and power demands change, your power supply's hardware ranges and software settings also change. The cost in time, money, and human resources associated with programmable power supplies that must be reconfigured with each changing FPGA circuit design is high. The ideal solution would come in a single versatile unit that would provide hardware-based output sequencing and ramp rate support inside the unit.

Power analysis

Power analyses of preliminary FPGA circuit designs are done with estimation algorithms. You can find these algorithms in the documentation provided by the FPGA's manufacturer. The accuracy of these estimation algorithms is low. Their main purpose is to give the power distribution designer a starting point by providing estimates of average and worst-case FPGA circuit power consumption. Some FPGA manufacturers take these preliminary estimation algorithms a step further and provide a software tool for power consumption calculations.

Once you complete a preliminary FPGA configuration, you can use FPGA circuit simulation software for power analysis. Simulation software is offered by either the FPGA manufacturer or a third-party software developer. Setting up simulations can be time consuming, depending on the amount of I/O traffic the FPGA circuit handles. Just imagine how long it would take and how tedious it would be to try to set up an accurate simulation for the large amount of I/O traffic an FPGA circuit in a high-speed Ethernet switch would encounter. The accuracy of the simulation is another concern -- it is highly dependent on how meticulously the simulation is set up. As with any software simulation, you cannot realistically achieve total accuracy.

Solution

The problems engineers face with FPGA circuit power-on requirements and power consumption analysis can be solved with the N6705A DC power analyzer. The N6705A DC power analyzer provides four DC power outputs. Each of the four output's characteristics is determined by which plug-in DC power module is used for that output. There are 21 different power modules available for the N6705A. Below is a list of N6705A features that make it an ideal solution for addressing power problems in FPGA circuit testing. You can easily set all of the following features from the instrument front panel or Web interface without any programming:

- Each output can deliver up to 300 W and up to 20 A. The output power and up/down programming speed are dependent on the power module used for that output. For greater power and current capabilities, outputs can be paralleled together to form a single virtual output. These features ensure that all FPGA circuits, as well as any interface power inputs, will have a more than adequate amount of power available to them.
- The DC power outputs have output sequencing capabilities. Delay can range between 0 and 1.023 s in 1-ms steps. Precision slew rate control on each channel, as fast as 20 us per volt, allows voltage ramp up times to be set on a per-channel basis. If you need sequencing of more than four power outputs, multiple mainframes can be sequenced together. These features ensure you will be able to satisfy various turn-on sequencing requirements and ramp rates of different FPGA circuit designs.
- The N6705A provides an oscilloscope-like display that can show voltage, current, and power versus time on multiple channels. This feature allows FPGA circuit designer to view in real time the voltage, current, and power events of their designs.
- The N6705A's built-in data logger continuously logs timestamped data to a large color display and to a file. You can log data on all four outputs at the same time. Data log files can be saved to internal memory or to an external USB memory drive.
- Table 1 lists the N6705A power modules that would be a good solution for FPGA testing and applicable specifications:

Table 1. Suggested N6705A power modules for FPGA testing

		N6751A/52A	**N6754A**	**N6761A/62A**
DC output ratings	Voltage	50V	60 V	50 V
	Current	5 A/10 A	20 A	1.5 A/3 A
	Power	50 W/100 W	300 W	50 W/100 W
Max up-programming time with full R load (time from 10% to 90% of total voltage)	Voltage change	0 to 10 V	0 to 15 V	0 to 10 V
	Time	0.2ms	0.35 ms	0.6 ms
	Voltage change	0 to 50 V	0 to 60 V	0 to 50 V
	Time	1.5 ms	2.0 ms	2.2 ms
Voltmeter/ammeter measurement accuracy (at 23°C ±5°C) voltage	Voltage high range	0.05% + 20 mV	0.05% + 25 mV	0.016% + 6 mV
	Voltage low range (5.5 V)	N/A	N/A	0.016% + 1.5 mV
	Current high range	0.1% + 4 mA	0.10% + 8 mA	0.04% + 160 µA
	Current low range (^{2} 100 mA, at 0 - 7 V)	N/A	N/A	0.03% + 15 µA
	(^{2} 100 mA, at 0 - 50 V)	0.05% + 20 mV	0.03% + 55 µA	

Example: Properly powering on a Xilinx Spartan-3 FPGA circuit

The correct power-on requirements for the FPGA example circuit and the power-on setup are shown in Figure 1.

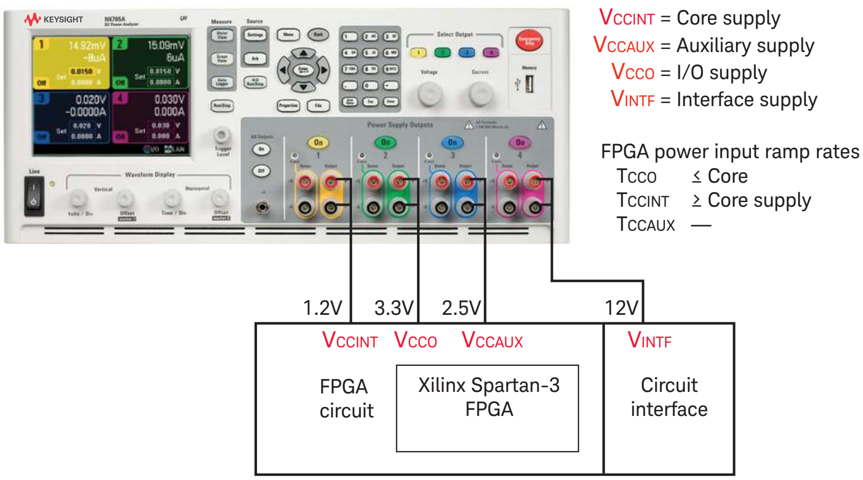


Figure 1. FPGA circuit test setup

For our example, we will let the interface supply (VINTF) represent the power supply for a configuration device such a NOR Flash PROM or microcontroller. For proper FPGA configuration, VINTF will be turned on 1 ms before the FPGA is powered up to simulate a real life configuration scenario. This turn-on delay ensures the configuration device has completed powered on and is ready to feed the FPGA its configuration from memory.

The Spartan-3 series of FPGAs does not have strict sequencing requirements. However, if the VCCINT is turned on before or at the same time as VCCAUX, the FPGA will draw a surplus core current. The surplus current draw can wear down a battery faster and could force the power distribution designer to use a higher current handling power-hungry regulator. Figure 2 shows the sequencing, or Output On/Off Delay, setup screen. Notice VCCINT is sequenced to turn on 1 ms before VCCAUX, on the N6705A. As a result, an undesirable surplus current spike occurs at the core supply (VCCINT) during turn-on because it was powered on before VCCAUX.

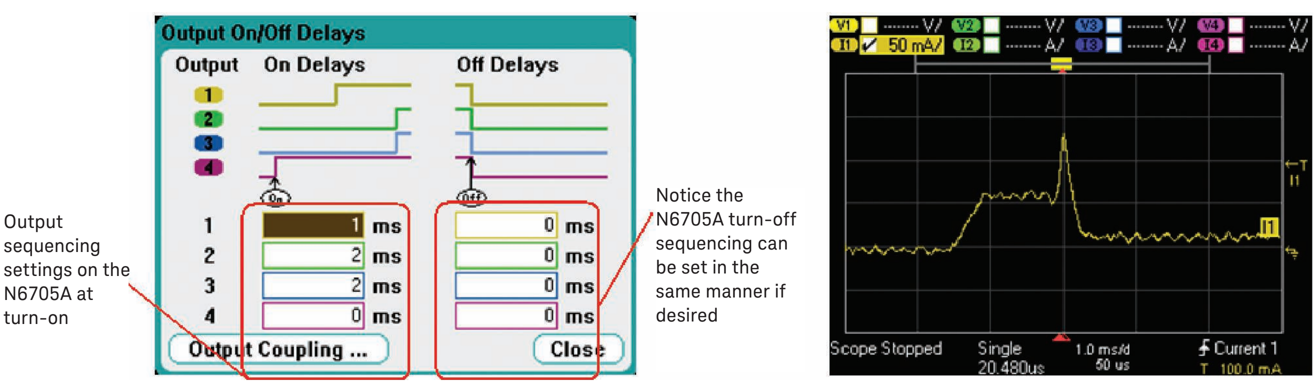


Figure 2. Output sequencing settings and surplus core current at turn-on

Example: Properly powering on a Xilinx Spartan-3 FPGA circuit (continued)

Figure 3 shows the proper sequencing to avoid the surplus current spike of ICCINT at turn-on (left) and the output core current.

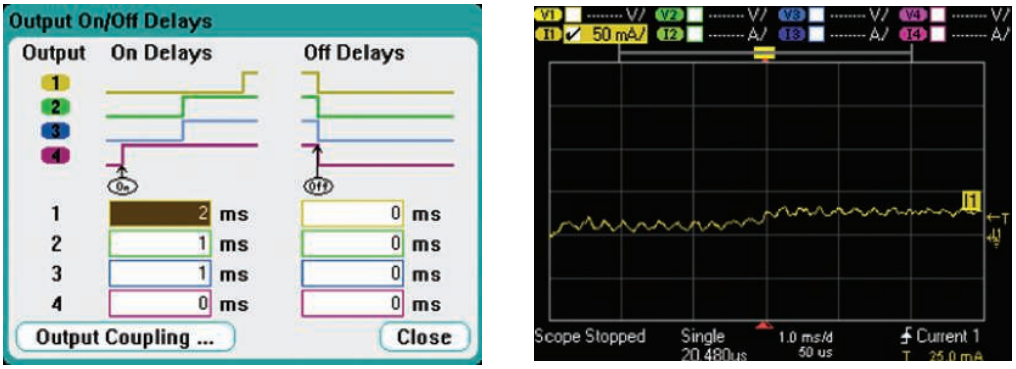


Figure 3. Output sequencing settings and core current at turn-on

To achieve the ramp rate requirements for VCCINT and VCCO (see Figure 1), the slew rates for channels 1 and 2 were adjusted. Figure 4 shows the N6705A display for changing a channel's slew rate, which is expressed in volts per second (V/s).

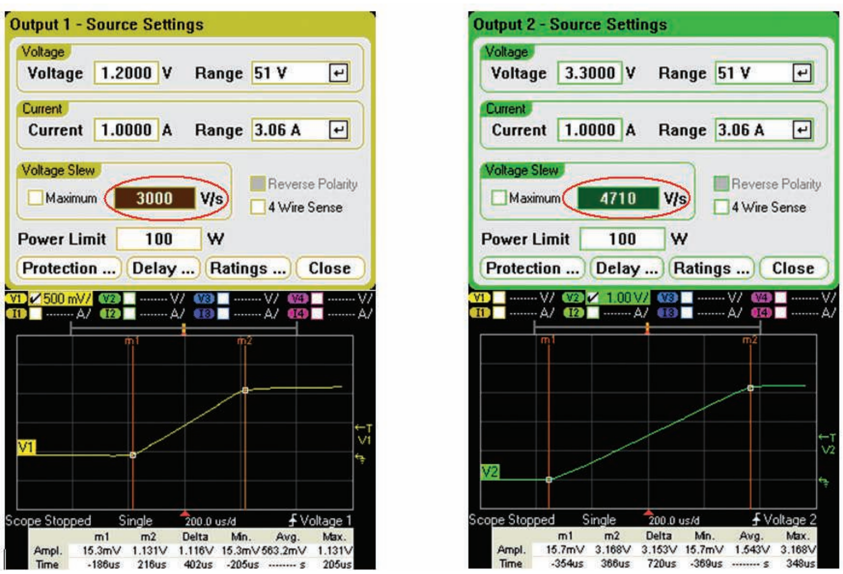
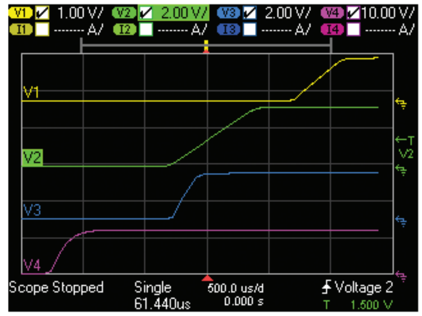


Figure 4. Core voltage and I/O voltage slew rate settings

Example: Properly powering on a Xilinx Spartan-3 FPGA circuit (continued)

To ensure successful power-on, the FPGA circuit supplies must raise through their respective threshold-voltage ranges with no dips. Figure 5 displays each output from the N6705A with proper sequencing and ramp rates at turn-on time. Each output presents a smooth rise of voltage that is free of dips and other erratic behavior. Figure 5 also lists the power modules used for the example FPGA circuit tests. Since the example circuit uses low power (< 2A), any module from the N675xA Series or N676xA Series is a good fit for this demonstration. Up/down output speed, measurement accuracy, and output power capabilities are the main features you need to consider when choosing the proper N6705A power modules for your specific FPGA circuit needs. Refer to Table 1 on page 3 for information regarding recommended power modules and their specifications.



Power Modules used	
Chan 1:	N6762A
Chan 2:	N6762A
Chan 3:	N6752A
Chan 1:	N6752A

Figure 5: Power module voltages at turn-on

Analyzing power consumption of a Xilinx Spartan-3 FPGA circuit

You can use the N6705A DC power analyzer to analyze the power consumption of an FPGA circuit using its built-in data logger function without having to write code. With the data logger in continuously sampled mode, the built-in digitizer of the DC power modules run continuously at 50,000 readings per second. You can specify a sample period, which is the period of time during which these continuous readings will be accumulated. For each sample period, one average reading (and optionally, a minimum and maximum value) will be saved. In this mode, the digitizer runs continuously as the readings are averaged and stored; therefore, the digitizer is always making measurements and no data is missed. The sample period is programmable from 1 millisecond to 60 seconds. Figure 6 below shows the Data Logger Properties screen on the N6705A.

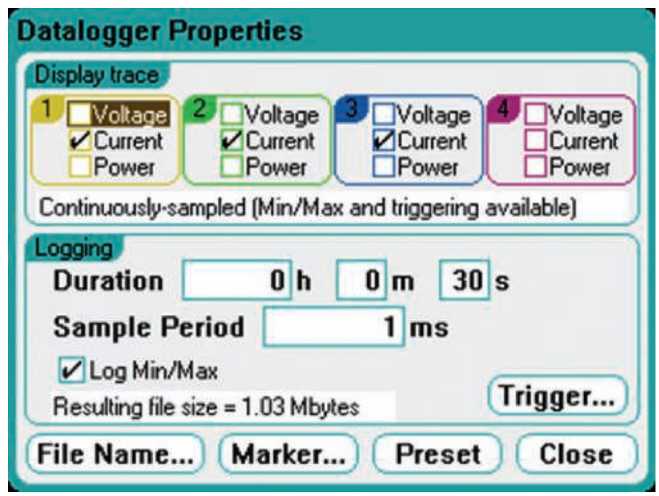


Figure 6. Data logger set up

Example: Properly powering on a Xilinx Spartan-3 FPGA circuit (continued)

Analyzing power consumption of a Xilinx Spartan-3 FPGA circuit

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Figure 7 shows a three-channel current output (ICCINT, ICCO, ICCAUX) capture using the N6705A's data logger. Notice at the bottom of the display capture on the left, you can see the file name under which the data file will be stored. The display capture on the right features the marker capability of the N6705A.

The N6705A's maximum data log file size is 2 gigabytes using extended memory capabilities, which amounts to 500 million readings. You can store the logged data file on the N6705A's internal non-volatile RAM or save it externally on a USB memory device. After you save the logged data, you can view it at a later time. You also can export logged data to a CSV file that can be read by most common data analysis software packages such as Microsoft® Excel.

Sequencing power on more than four supplies

If the FPGA test circuit requires more than four separate power supply inputs, you can sequence multiple N6705A mainframes together. You can do this using the user-configurable digital I/O ports located on the back of the mainframe. The latency involved when communicating between multiple mainframes is trivial compared to the rise time of the power modules and the 1-ms sequencing step size. No programming or code writing is needed to take advantage of this feature.

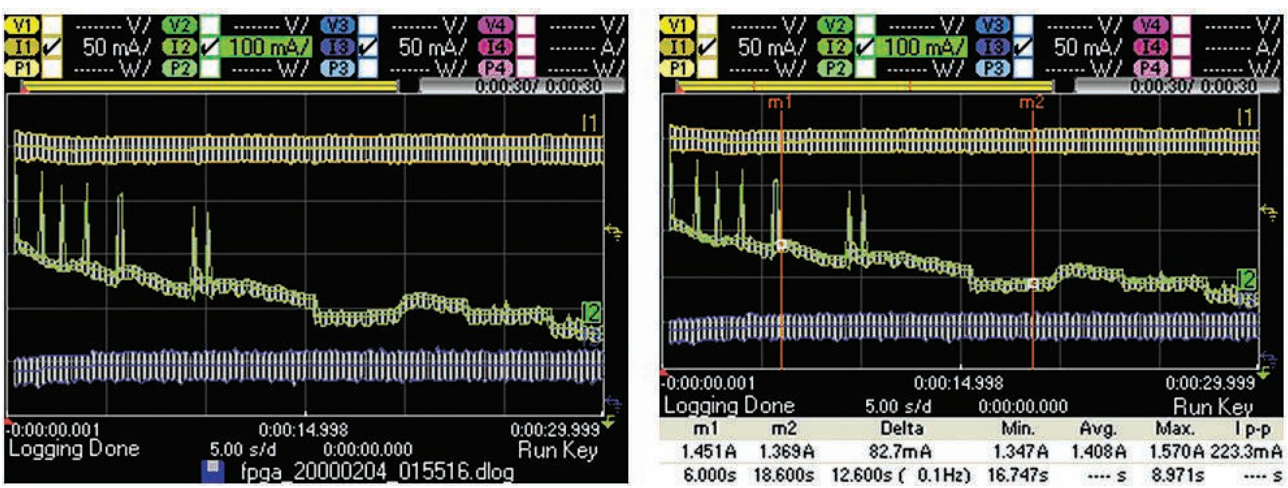

Figure 7. Two N6705A data logger displays. The display on the right features the instrument's marker capability.

Conclusion

The N6705A DC power analyzer is a total solution for all FPGA circuit power testing needs. With four outputs on a single unit that allows sequencing as well as slew rate control, the N6705A can optimally power on FPGA circuits. The N6705A offers flexibility and accuracy and saves time over existing FPGA power-on solutions such as fixed regulator circuits and multiple programmable power supplies. Combining the features just mentioned with multiple channel data logging, a scope view, and deep, expandable memory, the N6705A provides the ability to analyze FPGA circuit power consumption. The N6705A offers greater accuracy, ease of use, and a much faster setup time for analyzing power consumption compared to complicated software simulation and inaccurate power consumption algorithms.

Related Applications

- ASIC circuits
- PC motherboards
- Microcontroller circuits
- Controlled sequenced shutdown upon fault

Related Literature

Keysight DC Power Analyzer, Product Overview,
Publication Note 5989-6319EN

Keysight N6700 MPS Low-Profile Modular Power System,
Product Overview,
Publication Note 5989-1411EN

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