Keysight N5106A
PXB Baseband Generator
and Channel Emulator

Data Sheet
Definitions

Specification (spec): Represents warranted performance. Because this instrument is primarily digital in nature, there are no analog performance specifications.

Typical (typ): Represents characteristic performance that is non-warranted. Describes performance that will be met by a minimum of 80% of all products.

Nominal (nom): Represents characteristic performance that is non-warranted. Represents the value of a parameter that is most likely to occur; the expected mean or average.

Measured (meas): Represents characteristic performance that is non-warranted. Represents the value of a parameter measured during the design phase.

Note: All graphs contain measured data from several units at room temperature (approximately 25 °C) unless otherwise noted.
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N5106A PXB baseband generator and channel emulator

Supported use cases and configurations

<table>
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<tr>
<th>Use cases</th>
<th>Configurations</th>
</tr>
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<tr>
<td>Baseband generation</td>
<td>1, 2, 4, 6 channels</td>
</tr>
<tr>
<td>Baseband generation and sum</td>
<td>2, 4 channels</td>
</tr>
<tr>
<td>Baseband generation and fading</td>
<td>1, 2 channels</td>
</tr>
<tr>
<td>Single-user MIMO</td>
<td>1x2, 1x4, 1x8, 2x1, 2x2, 2x4, 2x6, 2x8, 4x2, 4x4</td>
</tr>
<tr>
<td>Multi-user MIMO</td>
<td>2x2, 2x4, 4x2, 4x4</td>
</tr>
<tr>
<td>RF and digital I/Q fading</td>
<td>1, 2 channels, 1 channel with interferer</td>
</tr>
<tr>
<td>MIMO RF and digital I/Q fading</td>
<td>1x2, 2x2, 2x4, 2x6, 2x8, 4x2, 4x4</td>
</tr>
<tr>
<td>Signal capture</td>
<td>1 channel</td>
</tr>
<tr>
<td>E5515C (8960) fading</td>
<td>1, 2 channels, 1x2 (Rx diversity), 1 channel with interferer</td>
</tr>
</tbody>
</table>

1. This use case supports RF output with vector MXG/ESG and digital I/Q output with N5102A.
2. This use case supports RF input with PXA/MXA/EXA and digital I/Q input with N5102A.
3. MXGs and ESGs cannot be used together for MIMO configurations.
Baseband Generator Characteristics
(Requires Option EFP)

Number of baseband generators Up to 6

Signal bandwidth

<table>
<thead>
<tr>
<th>PXB output interface</th>
<th>Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog I/Q outputs(^2)</td>
<td>160 MHz(^3)</td>
</tr>
<tr>
<td>Digital bus(^5)</td>
<td>N5102A digital signal interface module 120 MHz</td>
</tr>
<tr>
<td></td>
<td>N5162/82A MXG vector signal generators(^5) 100 MHz</td>
</tr>
<tr>
<td></td>
<td>E4438C ESG vector signal generators(^6) 80 MHz</td>
</tr>
</tbody>
</table>

Arbitrary waveform memory 512 Msa (2 GB) per baseband generator

Sample rate 1 kSa/sec to 150 MSa/sec\(^1\)

Resolution 14 bits\(^7\)

Baseband frequency offset range –80 MHz to 80 MHz\(^8\)

Compatible signal formats Signal Studio, E4438C, N5162/82A, Advanced Design System (ADS), SystemVue 2008, custom I/Q waveforms\(^9\)

Numeric formats Two’s complement, offset binary

Waveform length 256 samples to 512 Msa

Waveform loading speed\(^10\) LAN to PXB hard drive: 4 MB/s (nom) PXB hard drive to arbitrary waveform memory: 20 MB/s (nom) External eSATA hard drive to PXB arbitrary waveform memory: 20 MB/s (nom)

RMS values for power control Measured, previous RMS, user entered, waveform header RMS

When connected to the MXG/ESG via the digital bus, the PXB has negligible contribution to RF flatness, EVM, and ACP. See MXG/ESG data sheet for performance details.

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1. Each baseband generator can individually set sample rate.
2. The PXB connected to the E4438C ESG via analog I/Q provides automatic power calibration at RF up to 120 MHz. RF power management when connected via the PXB’s analog I/Q outputs to all other signal generators requires manual power calibration.
3. 60 MHz I and 60 MHz Q.
4. When the PXB output is connected via digital bus to the MXG/ESG, bandwidth is limited by the vector signal generator.
5. Requires MXG firmware revision A.01.44 or later.
6. Requires ESG firmware revision C.05.23 or later. Contact division for demo firmware.
7. 16-bit I/Q waveforms created for the E4438C and N5162/82A are compatible with the PXB. For optimal performance, PXB waveforms should be created with 16-bit resolution. Refer to the online documentation for more information.
8. Baseband offset range is limited by output instrument when connected via digital bus.
9. Users load waveforms into the PXB baseband generator for playback. See online documentation for details on custom waveform format.
10. Performance varies depending on external PC and LAN connection.
Simulate real-world conditions to test multi-format receivers more quickly and validate design robustness earlier in the development cycle with the PXB.

Number of faders: Up to 8

Fading bandwidth

<table>
<thead>
<tr>
<th>Internal baseband generation and fading</th>
<th>Maximum bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog I/Q outputs&lt;sup&gt;1&lt;/sup&gt;</td>
<td>160 MHz&lt;sup&gt;2&lt;/sup&gt;</td>
</tr>
<tr>
<td>Digital bus&lt;sup&gt;3&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td>N5102A digital signal interface module</td>
<td>120 MHz</td>
</tr>
<tr>
<td>N5162/82A MXG vector signal generators&lt;sup&gt;4&lt;/sup&gt;</td>
<td>100 MHz</td>
</tr>
<tr>
<td>E4438C ESG vector signal generators&lt;sup&gt;5&lt;/sup&gt;</td>
<td>80 MHz</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>External RF input for fading</th>
<th>Maximum bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital bus&lt;sup&gt;6&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td>N9010A EXA&lt;sup&gt;7&lt;/sup&gt;, N9020A MXA&lt;sup&gt;7&lt;/sup&gt;, and N9030A PXA&lt;sup&gt;8&lt;/sup&gt; vector signal analyzer</td>
<td>40 MHz&lt;sup&gt;11&lt;/sup&gt;</td>
</tr>
<tr>
<td>N5102A digital signal interface module</td>
<td>120 MHz</td>
</tr>
<tr>
<td>E5515C (8960) wireless communications test set&lt;sup&gt;9&lt;/sup&gt;</td>
<td>Standard dependent&lt;sup&gt;10&lt;/sup&gt;</td>
</tr>
</tbody>
</table>

RF input: -40 dBm to 15 dBm with EXA/MXA/PXA

RF output: -115 dBm to 0 dBm with MXG
-115 dBm to -10 dBm with ESG

Paths per fader:
- 6 paths @ 160 MHz
- 12 paths @ 80 MHz
- 24 paths @ 40 MHz

Paths per fader with fader interleaving for:
- 6 paths @ 80 MHz
- 12 paths @ 40 MHz
- 24 paths @ 20 MHz (Option 169)

Power accuracy: When connected to the MXG/ESG via the digital bus, the PXB has negligible contribution to power accuracy. This is in comparison to the signal generators set to the same conditions separately. See MXG/ESG data sheet for performance details.

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1. The PXB connected to the E4438C ESG via analog I/Q provides accurate power calibration at RF up to 160 MHz. RF power management when connected via the PXB’s analog I/Q outputs to all other signal generators requires external power calibration.
2. 80 MHz I and 80 MHz Q.
3. When the PXB output is connected via digital bus to the MXG/ESG, bandwidth is limited by the vector signal generator.
4. Requires MXG firmware revision A.01.44 or later.
5. Requires ESG firmware revision C.05.23 or later.
6. When the PXB input is connected via digital bus to the PXA/MXA/EXA, fading bandwidth is limited by the vector signal analyzer.
7. Requires MXA firmware revision A.01.61 or later, EXA firmware revision A.04.26 or later.
8. Requires PXA firmware revision A.06.06 or later.
9. Requires E5515C-004 and the relevant Lab Application(s). Review online documentation or the configuration guide for Lab Application revision requirements.
10. EGPRS2-A and downlink dual carrier GSM requires RF fading.
11. Requires Option B25 for 25 MHz or B40 for 40 MHz bandwidth.
Fader Characteristics (Requires Option QFP) continued...

Predefined channel models

W-CDMA, HSDPA, HSUPA, COST 259, TD-SCDMA, cdma2000®, cdmaOne, 1xEV-DO, GSM, EDGE, WLAN, TETRA, 802.16 OFDM, 802.16 OFDMA, LTE (includes high speed train), MBRAI models for DVB-T and DVB-H

Predefined MIMO channel models

LTE: 3GPP standard 36.101 Annex B, modified SCME urban micro-cell, SCME urban micro-cell, SCME urban macro-cell, WINNER II, single cluster EPA, single cluster SCME, 2D uniform (requires Option TFP) Mobile WiMAX™ channel model for MTG RCT (requires Option RFP)

Repetition interval

> 7 days

Random seed

89 bits

Fading types

Pure Doppler, Rayleigh, Rician, Suzuki, log normal

Spectral shape

Classical 3 dB, classical 6 dB, flat, rounded, Jakes classical, Jakes rounded, Gaussian

Rayleigh distribution

0.5 dB from –30 to + 10 dB of mean power level
Deviations from CDF, filtered noise

Rician

Power ratio (k) range

–84 dB to 84 dB

LOS AoA

0 to 360°

Path delay

Resolution

0.1 ns

Accuracy

±(0.4 ns + 0.2% path delay) (meas)

Phase shift

Resolution

0.01°

Path loss

Resolution

0.01 dB

Accuracy

0.1 dB (meas)

Vehicle speed

Resolution

0.01 km/h

Doppler frequency

Resolution

0.001 Hz

Accuracy

0.05% (meas)

Angle of arrival (AoA)

Resolution

0.01°

Angle of departure (AoD)

Resolution

0.01°

AoA Azimuth spread

Resolution

0.01°

AoD Azimuth spread

Resolution

0.01°

Log normal

Standard deviation

0 to 12 dB

Decorrelation length

1 m to 1 km

MIMO correlation source

From wireless standard, from custom antenna setup, from custom correlation matrix

Custom correlation matrix

Channel to channel, path to path

Path configuration source

From wireless standard, custom

Antenna patterns

Omni-directional, three-sector, six-sector, uncorrelated, user specified (2D and 3D antenna models from EMPro or equivalent)

Antenna spacing

–20 to 20 wavelengths in X and Y coordinates

1. Doppler frequency of vehicle speed is coupled to the carrier frequency setting in the Fader Setup view.

2. Implemented as filtered noise.
Dynamic Fading

- Number of dynamic paths: Up to 24
- Number of states: 1 to 5000
- Requested dwell time: 10 ms to 1000s
  - Resolution: 10 ms
- Path loss: 0 to 84 dB
  - Resolution: 0.01 dB
- Path delay: 0 to 2 ms
  - Resolution: 0.1 ns
- Path UE speed: 0 to 1726.8/carrier frequency in km/hr
  - Resolution: 0.01 km/hr
- Number of channels: Up to 1

Signal Capture Characteristics (Requires Option FFP)

- Signal capture sample rate: 1 kSa/sec to 150 MSa/sec
- Signal capture depth: 256 samples to 512 Msa (2 GB) per channel
- Signal capture duration: Signal capture depth / sample rate
  - Resolution: 14 bits
- Trigger type: Free run, master trigger, magnitude
- Trigger value: 0 to 46340
- Trigger time delay: 0 to 2147483.647 seconds
- Trigger sample delay: 0 to 2147483647 samples
- Trigger position: 0 to 100%
- AWGN bandwidth: Up to 120 MHz
- Signal to noise (S/N) ratio: -20 dB to +40 dB
  - Resolution: 0.1 dB
  - Accuracy: 0.3 dB (meas)
- Crest factor: 12.88 dB
- Units: SNR, Eb/No
  - Optimization: Constant signal power, constant noise power, constant SNR
  - Output MUX: Signal + noise, signal only, noise only
- Repetition interval: > 7 days

1. States are defined in Microsoft Excel. The Excel template is included with the firmware installation.
2. Actual dwell time is calculated based on requested dwell time and UE speed. Refer to the help system for details.
3. When the PXB input is connected via digital bus, signal capture bandwidth is limited by the input device.
4. Each signal capture channel supports an independent sample rate, depth, and duration.
5. For magnitude trigger only.
6. Trigger time delay is variable, based on sample rate. It is the trigger sample delay/sample rate.
7. Requires Option B25 for 25 MHz or B40 for 40 MHz bandwidth.
Test baseband chipsets with the PXB and the N5102A digital signal interface module.

**Digital I/O Characteristics**

| Logic types (requires N5102A) | Single-ended: LVTTL, CMOS (1.5 V, 1.8 V, 2.5 V, 3.3 V)  
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Differential: LVDS</td>
</tr>
<tr>
<td><strong>Number of I/O ports</strong></td>
<td>2 per I/O card, up to 8 total</td>
</tr>
<tr>
<td><strong>Resolution</strong></td>
<td>14 bits</td>
</tr>
<tr>
<td><strong>Baseband frequency offset</strong></td>
<td>-80 MHz to 80 MHz</td>
</tr>
<tr>
<td><strong>I/Q skew</strong></td>
<td>-2 ns to 2 ns</td>
</tr>
<tr>
<td></td>
<td>Resolution: 1 ps</td>
</tr>
<tr>
<td><strong>I/Q gain balance</strong></td>
<td>-4 dB to 4 dB</td>
</tr>
<tr>
<td></td>
<td>Resolution: 0.01 dB</td>
</tr>
<tr>
<td><strong>Delay</strong></td>
<td>0 to 500 ns</td>
</tr>
<tr>
<td></td>
<td>Resolution: 1 ps</td>
</tr>
<tr>
<td><strong>Quadrature skew</strong></td>
<td>-30 to 30°</td>
</tr>
<tr>
<td></td>
<td>Resolution: 0.01°</td>
</tr>
</tbody>
</table>

1. Logic types available when connected to N5102A digital signal interface module.
2. Each output port must be designated as analog or digital in the PXB user interface. The same port cannot be used for both simultaneously.
3. Baseband offset range is limited by output instrument when connected via digital bus.
### Analog Output Characteristics

<table>
<thead>
<tr>
<th>Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port type</td>
<td>Analog I/Q, single-ended and differential</td>
</tr>
<tr>
<td>Number of analog I/Q ports</td>
<td>2 per I/O card, up to 8 total</td>
</tr>
<tr>
<td>Level</td>
<td>1.0 Vpp single-ended, 2.0 Vpp differential; 50 Ω</td>
</tr>
<tr>
<td>Resolution</td>
<td>14 bits</td>
</tr>
<tr>
<td>Baseband frequency offset</td>
<td>–80 MHz to 80 MHz²</td>
</tr>
<tr>
<td>I/Q skew</td>
<td>–2 ns to 2 ns</td>
</tr>
<tr>
<td>Resolution</td>
<td>1 ps</td>
</tr>
<tr>
<td>I/Q gain balance</td>
<td>–4 dB to 4 dB</td>
</tr>
<tr>
<td>Resolution</td>
<td>0.01 dB</td>
</tr>
<tr>
<td>Delay</td>
<td>0 to 500 ns</td>
</tr>
<tr>
<td>Resolution</td>
<td>1 ps</td>
</tr>
<tr>
<td>Quadrature skew</td>
<td>–30 to 30°</td>
</tr>
<tr>
<td>Resolution</td>
<td>0.01°</td>
</tr>
<tr>
<td>Common I/Q offset</td>
<td>–2.5 V to 2.5 V</td>
</tr>
<tr>
<td>Resolution</td>
<td>10 mV</td>
</tr>
<tr>
<td>Differential I offset</td>
<td>–25 mV to 25 mV</td>
</tr>
<tr>
<td>Resolution</td>
<td>1 mV</td>
</tr>
<tr>
<td>Differential Q offset</td>
<td>–25 mV to 25 mV</td>
</tr>
<tr>
<td>Resolution</td>
<td>1 mV</td>
</tr>
<tr>
<td>I/Q peak level</td>
<td>0 V to 1 Vpk</td>
</tr>
<tr>
<td>Resolution</td>
<td>10 mV</td>
</tr>
</tbody>
</table>

1. Each output port must be designated as analog or digital in the PXB user interface. The same port cannot be used for both simultaneously.
2. Baseband offset range is limited by output instrument when connected via digital bus.
Analog Output Characteristics continued...

Maximum reverse power
Max DC voltage 20 VDC (nom)
250 kHz to 500 MHz 1 W (nom)

Flatness$^1$
1 dB (typ)

Spurious free dynamic range$^1$
< −76 dBc (typ)

Harmonics$^1$

Phase noise$^1$
−147 dBc/Hz (typ)
10 MHz sinewave at 10 kHz offset

Noise floor$^1$
−152 dBc/Hz (typ)
10 MHz sinewave at 1.9 MHz offset

Flatness$^{1,2}$

Analog I/Q outputs harmonic distortion

Analog I/Q outputs flatness vs. frequency

1. These values apply at the PXB analog I/Q outputs only. When connected to the MXG/ESG via the digital bus, the PXB has negligible contribution. See MXG/ESG data sheet for performance data.

2. These values apply to SN MY50460000 and higher.
**Frequency Reference Characteristics**

Internal time base reference
OCXO, 10 MHz, stability ±0.01 ppm,
from +20 to +30 °C
Aging ±0.1 ppm/year for the first year
Aging ±0.15 ppm/year for the first 2 years
Operating temperature range is from
0-40 °C

External reference input
1 MHz to 100 MHz, –5 to +10 dBm;
50 Ω

Reference output
10 MHz, 0.9 Vpp ±10%; 50 Ω

**Clock, Trigger, and Marker Characteristics**

Channel synchronization
< 21 ns

Trigger source
Software, hardware, bus (GPIB, LAN)

External trigger in
3.3 V CMOS (nom)

Trigger delay
0 to 100 ms

Trigger jitter
5 ns

Trigger to analog I/Q out latency
250 ns (nom)

Trigger to RF latency
N5182A MXG: 600 ns (nom)
E4438C ESG: 1.3 us (nom)

N5102A latency
500 ns @ 100 MHz sample rate, 60 us @ 1 MHz
400 ns @ 100 MHz sample rate, 25 us @ 1 MHz

N5102A synchronization
N5102A and PXB operate on independent (non-transparent) clock domains. Best case synchronization between multiple N5102A units and PXB is ± 1 sample (with re-sampling off)

RF to RF latency
N5182A MXG through digital bus: 33 us (nom)
N5182A MXG through analog I/Q: 22 us (nom)
E4438C ESG through digital bus: 27 us (nom)
E4438C ESG through analog I/Q: 22 us (nom)

Marker outputs
3 markers per I/O port
3.3V CMOS (nom)

Marker source
Separate marker file, markers embedded in waveform, dynamic marker generation

Marker delay
0 to 1,024 samples (settable in time)

Marker polarity
Positive, negative

---

1. Does not include PXB and RF latency.
2. Latency is measured from the signal analyzer's RF input to the signal generator's RF output.
3. Power calibration not performed when connecting the PXB to the MXG through analog I/Q.
4. Markers are labeled 1, 3, and 4. Marker 2 is reserved for internal use only.
### General Chassis Characteristics

<table>
<thead>
<tr>
<th>Feature</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dynamic marker type</td>
<td>Periodic, range detect, zero detect</td>
</tr>
<tr>
<td>Operating system</td>
<td>Windows® XP for Embedded Systems</td>
</tr>
<tr>
<td>Programming language</td>
<td>SCPI(^1)</td>
</tr>
<tr>
<td>Connectivity</td>
<td>Gigabit LAN, IEEE 488 GPIB</td>
</tr>
</tbody>
</table>
| Non-volatile storage         | 160 GB hard drive total  
90 GB available for waveform and user data on D: partition  
(supplemented by external USB drives) |
| Available chassis slots      | Up to 6 baseband cards (or 12 DSP blocks)  
and up to 4 I/O cards                                                        |
| Power requirements           | 100 to 120 VAC 50 to 60 Hz, or  
200 to 240 VAC 50 to 60 Hz  
(automatically selected);  
< 875 W typical, 1075 W maximum                                      |
| Operating temperature        | 10 to 40 °C                                                            |
| Acoustic noise               | Idle: 57 dBA (nom)  
Normal: 60 dBA (nom)  
Worst case: 70 dBA (nom)  
Typical Keysight equipment:  
Normal = 54 dBA (nom)                                                     |
| Weight                       | Fully loaded: < 33 kg (72 lb)                                           |
| Dimensions                   | 222 mm H x 426 mm W x 584 mm D  
(8.75 in H x 16.8 in W x 23 in D)                                       |

#### System clock rear panel connectors

<table>
<thead>
<tr>
<th>Connector</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>EXT I/O CLK IN</td>
<td>Reserved for future use</td>
</tr>
<tr>
<td>EXT SYNC</td>
<td>Reserved for future use</td>
</tr>
</tbody>
</table>
| EXT TRIG IN     | External trigger signal used to trigger the start of the FPGA process 3.3 V CMOS [male SMB]  
Damage level: < 0 V and > 3.3 V     |

\(^1\) Does not apply to Signal Studio programming control.
**General Chassis Characteristics continued...**

<table>
<thead>
<tr>
<th>Connector</th>
<th>Description</th>
<th>Notice</th>
</tr>
</thead>
</table>
| **EXT REF IN**  | Input for an external frequency reference signal 1 MHz to 100 MHz, −5 to +10 dBm; 50 Ω [male SMB]  
Lock range: ±5 ppm  
Damage level: < 0 V and > 3.3 V |                                                                                                                   |
| **10 MHz OUT**  | 10 MHz reference output used to lock the frequency reference of other test equipment to the PXB  
900 mVpp; 50 Ω [male SMB]  
Damage level: < 0 V and > 3.3 V |                                                                                                                   |
| **100 MHz SYS CLK OUT** | 100 MHz system clock output  
2 Vpp; 50 Ω [male SMB]  
Damage level: < 0 V and > 3.3 V |                                                                                                                   |
| **I/O CLK OUT** | Reserved for future use                                                                                                                                                                                    |                                                                      |
| **TRIGGER OUT** | Routed from hardware or software trigger input TTL; 100 Ω [male SMB]  
Damage level: < 0.5 V and > 5.5 V |                                                                                                                   |
| **AUX I/O**     | Provides additional digital signal interface and feedback 3.3 V CMOS [male 20 pin mini delta]  
Damage level: < 0 V and > 3.3 V |                                                                                                                   |

**CPU host controller rear panel connectors**

<table>
<thead>
<tr>
<th>Connector</th>
<th>Description</th>
<th>Notice</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>MONITOR</strong></td>
<td>VGA connection of an external monitor</td>
<td></td>
</tr>
<tr>
<td><strong>USB SLAVE (top)</strong></td>
<td>Standard USB 2.0 ports, Type A connect to external peripherals such as a mouse, keyboard, printer, DVD drive, or hard drive</td>
<td></td>
</tr>
<tr>
<td><strong>USB MASTER (top)</strong></td>
<td>USB 2.0 port, Type B USB TMC (test and measurement class) connects to an external PC controller to control the PXB and for data transfers over a 480 Mbps link</td>
<td></td>
</tr>
<tr>
<td><strong>LAN</strong></td>
<td>Network interface used to control the PXB remotely</td>
<td></td>
</tr>
<tr>
<td><strong>GPIB</strong></td>
<td>A general purpose interface bus (IEEE 488 GPIB) connection that can be used for remote operation</td>
<td></td>
</tr>
<tr>
<td><strong>INTERCONNECT 1 &amp; 2</strong></td>
<td>Reserved for future use</td>
<td></td>
</tr>
<tr>
<td><strong>eSATA</strong></td>
<td>This port provides access to external eSATA Hard Disk Drive (HDD) storage devices to increase system file storage capacity with higher transfer rates than the USB port</td>
<td></td>
</tr>
<tr>
<td><strong>PCle x4 FROM UPSTREAM</strong></td>
<td>Reserved for future use</td>
<td></td>
</tr>
<tr>
<td><strong>PCle x4 TO DOWNSTREAM</strong></td>
<td>Reserved for future use</td>
<td></td>
</tr>
<tr>
<td><strong>USB (bottom)</strong></td>
<td>Reserved for future use</td>
<td></td>
</tr>
</tbody>
</table>
### I/O card(s) rear connectors

<table>
<thead>
<tr>
<th>Connector</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLOCK IN</td>
<td>Reserved for future use</td>
</tr>
<tr>
<td>TRG IN</td>
<td>Reserved for future use</td>
</tr>
<tr>
<td>MKR OUT</td>
<td>Marker outputs for each I/O board channel numbered 1, 3 and 4 (marker 2 is reserved for internal use)</td>
</tr>
<tr>
<td>3.3 V CMOS</td>
<td>[male SMB] Damage level: &lt; 0 V and &gt; 3.3 V</td>
</tr>
<tr>
<td>CLOCK OUT</td>
<td>Reserved for future use</td>
</tr>
<tr>
<td>DIGITAL BUS</td>
<td>Digital bus connectors enable operation with other test equipment such as the PXA/MXA/EXA signal analyzer, MXG and ESG vector signal generator, and N5102A digital signal interface module</td>
</tr>
<tr>
<td>I+, I–</td>
<td>Analog I/Q modulation from the internal baseband generator 2 Vpp; 50 Ω [male SMB] Damage level: &lt; –15 V and &gt; 15 V</td>
</tr>
<tr>
<td>Q+, Q–</td>
<td>Analog I/Q modulation from the internal baseband generator 2 Vpp; 50 Ω [male SMB] Damage level: &lt; –15 V and &gt; 15 V</td>
</tr>
</tbody>
</table>

### Literature

- **Keysight N5106A PXB Baseband Generator and Channel Emulator,** Photo Card, 5989–8969EN
- **Keysight N5106A PXB Baseband Generator and Channel Emulator,** Configuration Guide, 5989–8972EN
- **MIMO Channel Modeling and Emulation Test Challenges,** Application Note, 5989–8973EN
- **Solutions for Validation of LTE Devices – Testing MIMO Over-the-Air Using the Two-Stage Method,** 5990–8898EN
- **Theory, Techniques and Validation of Over-the-Air Test Methods for Evaluating the Performance of MIMO User Equipment,** 5990–5858EN
- **Ten Things You Should Know About MIMO SM (Spatial Multiplexing),** Poster, 5989–9618EN
- **GPS Receiver Testing,** Application Note, 5990–4943EN
- **Keysight CMMB Conformance Testing Using the PXB with N7623B Signal Studio for Digital Video,** Application Note, 5990–4978EN
Additional Resources

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