

Agilent EEsof EDA

**Presentation on Simulating Phase Locked Loops
using ADS**

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Simulating Phase Locked Loops Using ADS

Outline

What ADS is able to simulate, concerning PLLs

Basic concepts about Envelope simulation and PLL component behavioral modeling

Deriving sensitivity of a transistor-level phase/frequency detector and charge pump

An all-behavioral-model PLL

How to add phase noise from various components

Open- and closed-loop phase noise and spurs

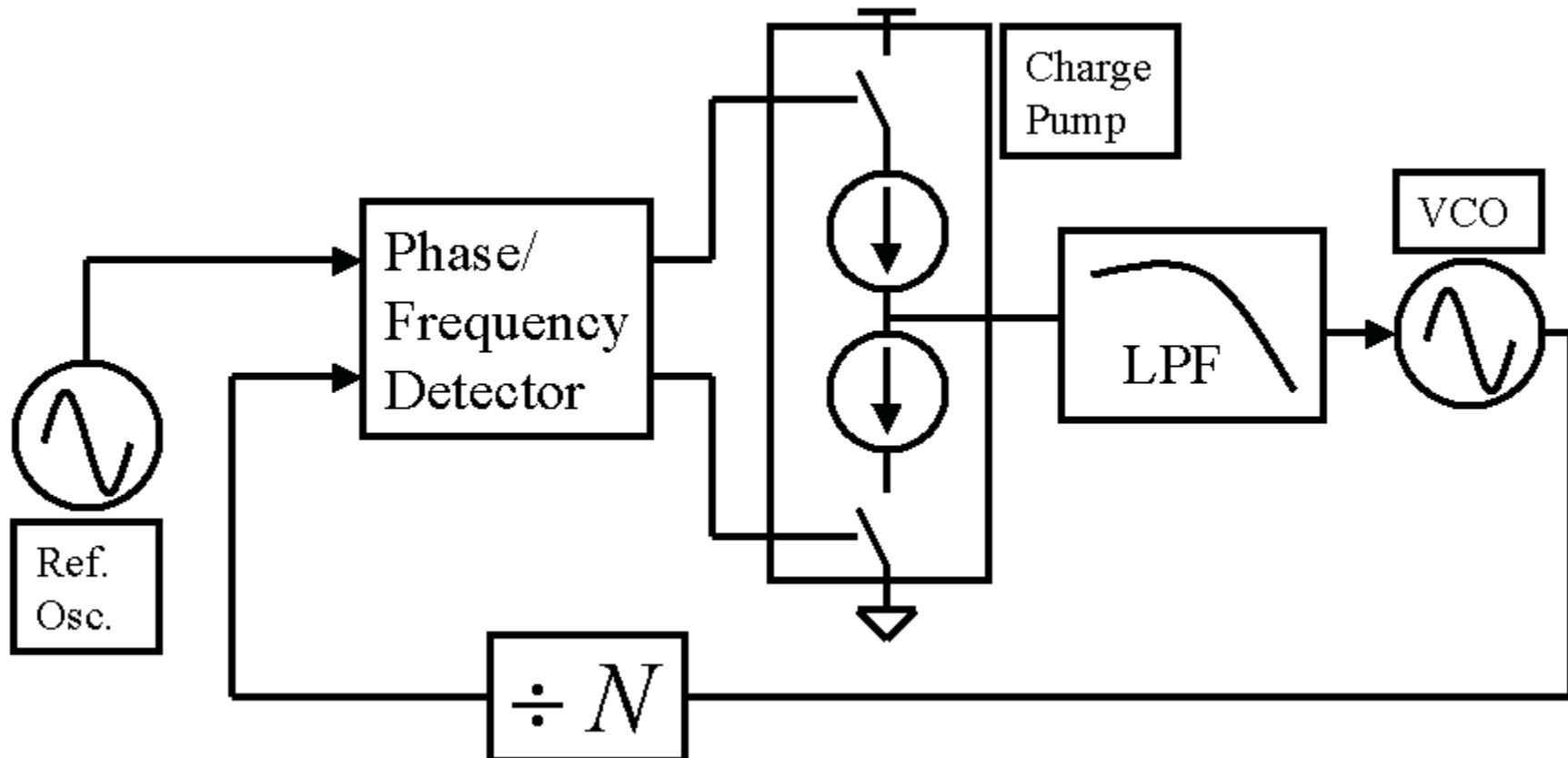
Running a fractional-N simulation

Using a sigma delta modulator to generate the divide ratio

Summary

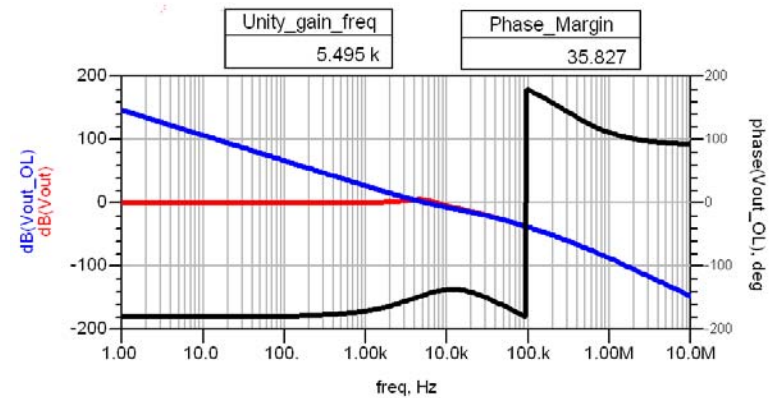
The PLL simulation problem (at transistor level)

With purely time-domain simulator, need small time step to sample VCO signal and capture digital signals in PFD and divider. Transient response may require milliseconds => millions of time points

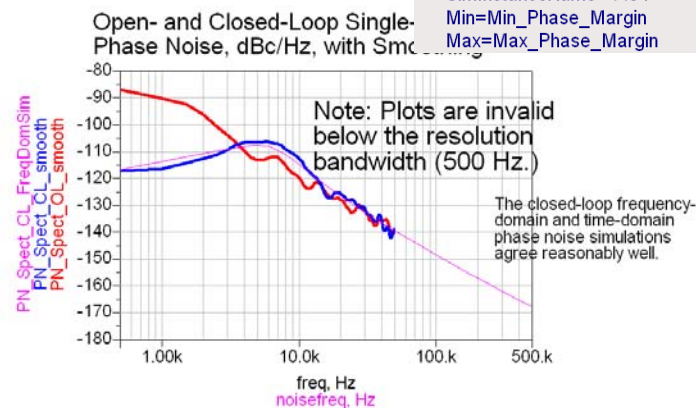
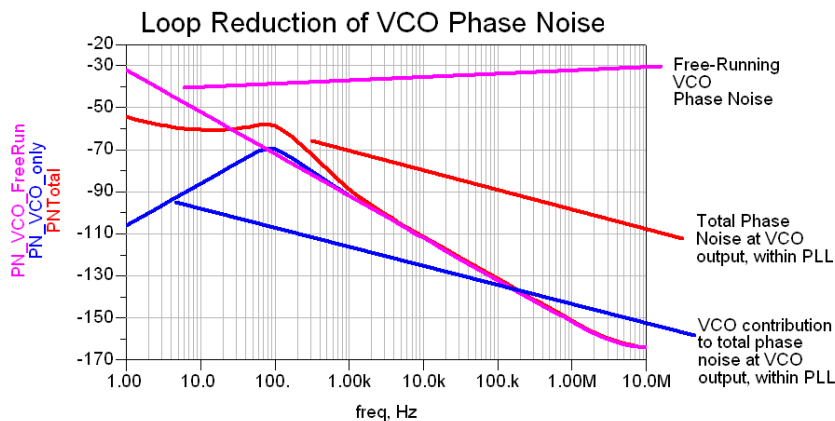


What ADS is able to simulate (utilizing mostly behavioral models)

- Open- and closed-loop frequency responses
- Optimization of unity-gain frequency and phase margin
- Phase noise – two methods: frequency domain and time domain

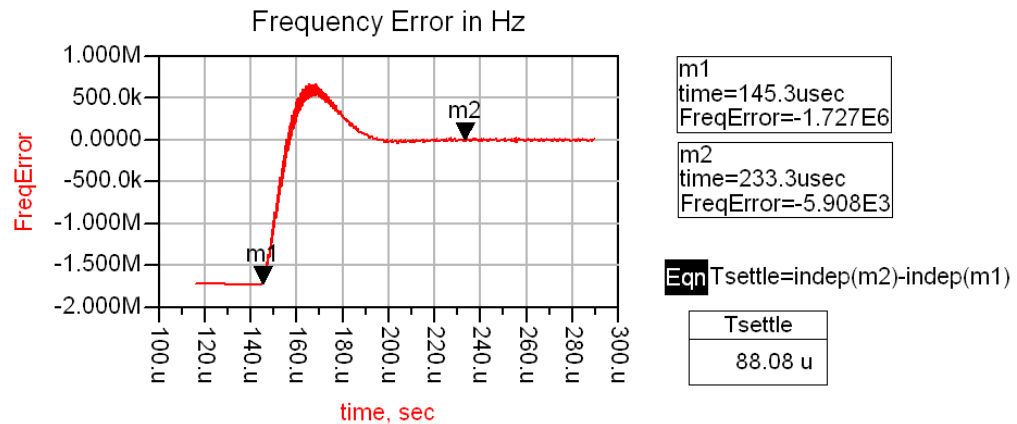
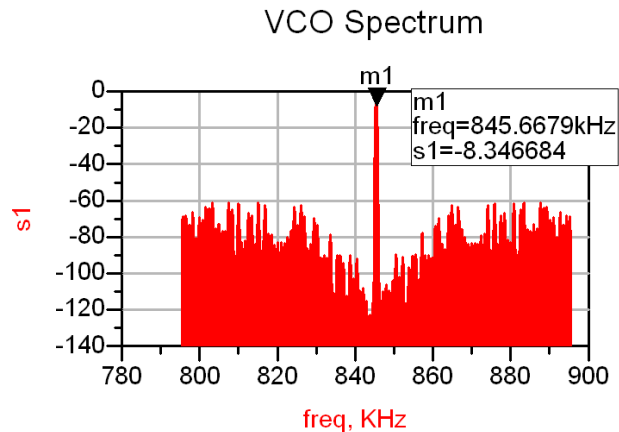
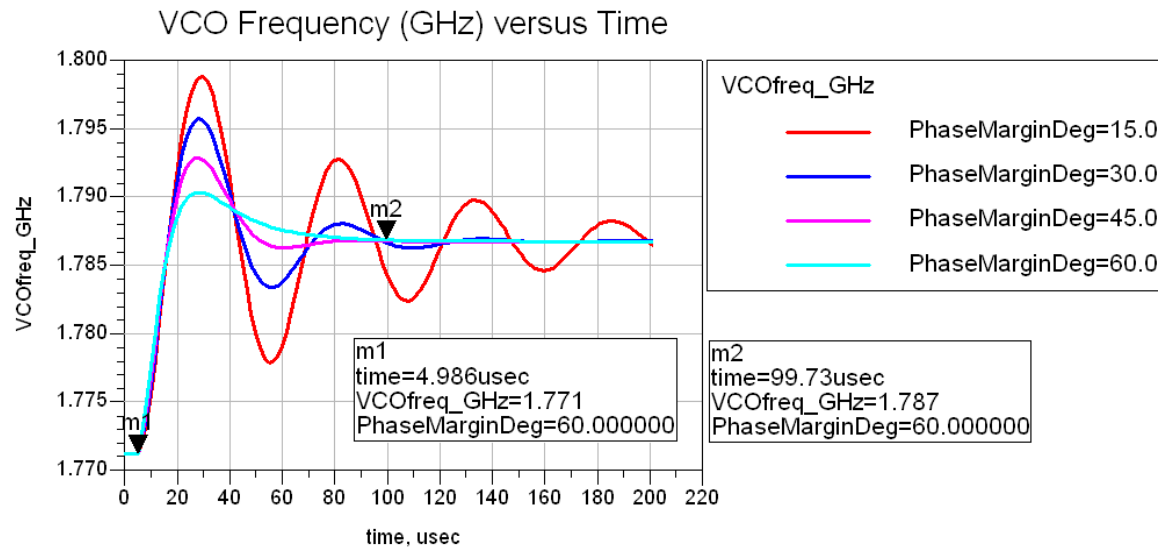


VAR VAR2 UnityGainFreq=20000 Min_Phase_Margin=43 Max_Phase_Margin=47 SpurFreq=1 MHz SpurAtten=60_dB	AC AC AC1 Freq=UnityGainFreq
GOAL Goal OptimGoal2 Expr="Phase_Margin" SimInstanceName="AC1" Min=Min_Phase_Margin Max=Max_Phase_Margin	GOAL Goal OptimGoal1 Expr="OLgain" SimInstanceName="AC1" Min=0.99 Max=1.01

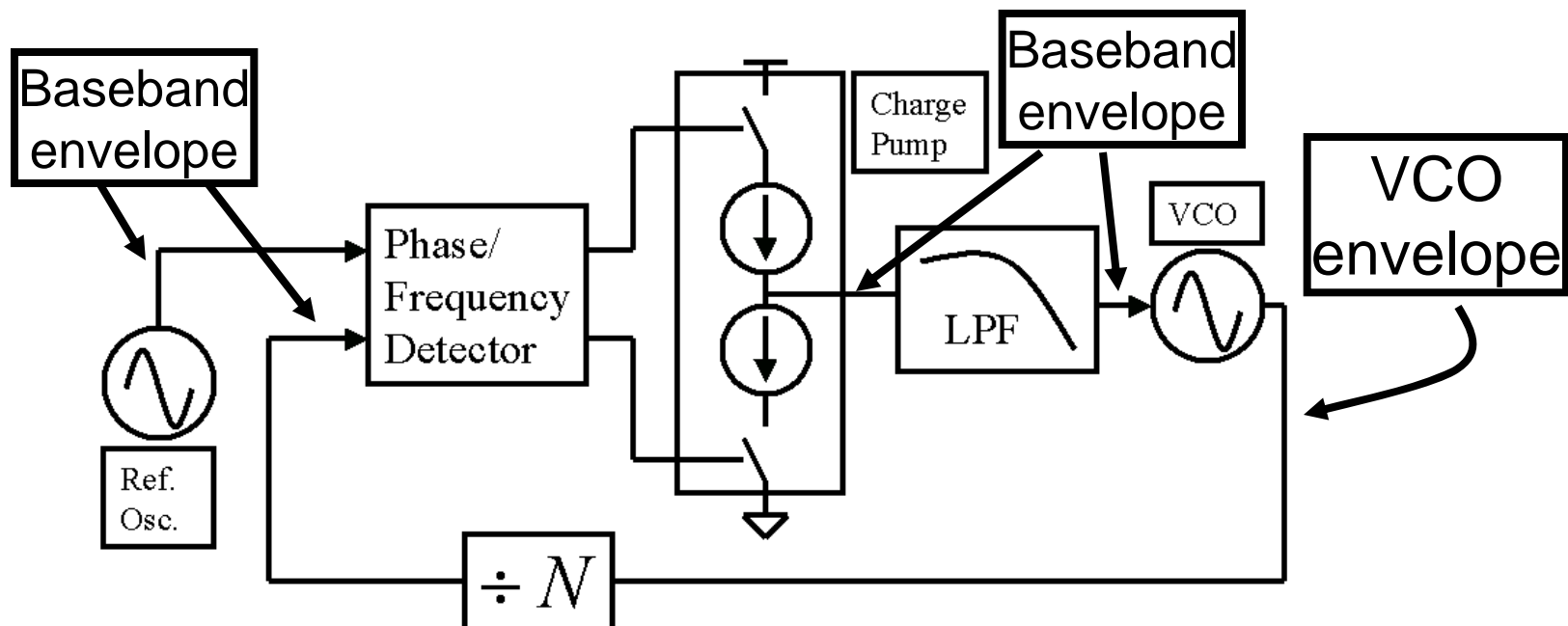
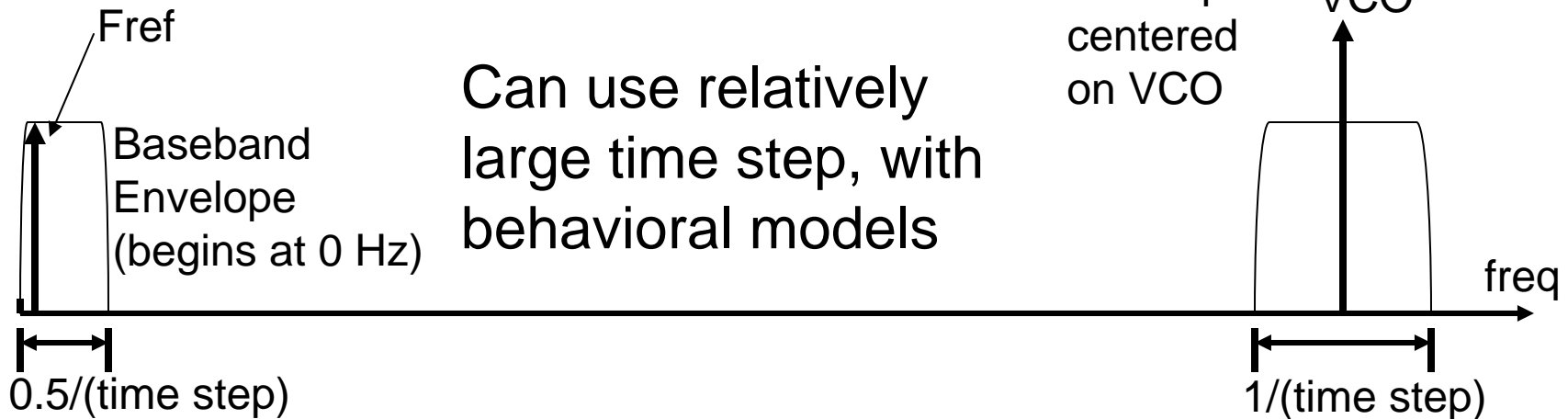


What ADS is able to simulate (2)

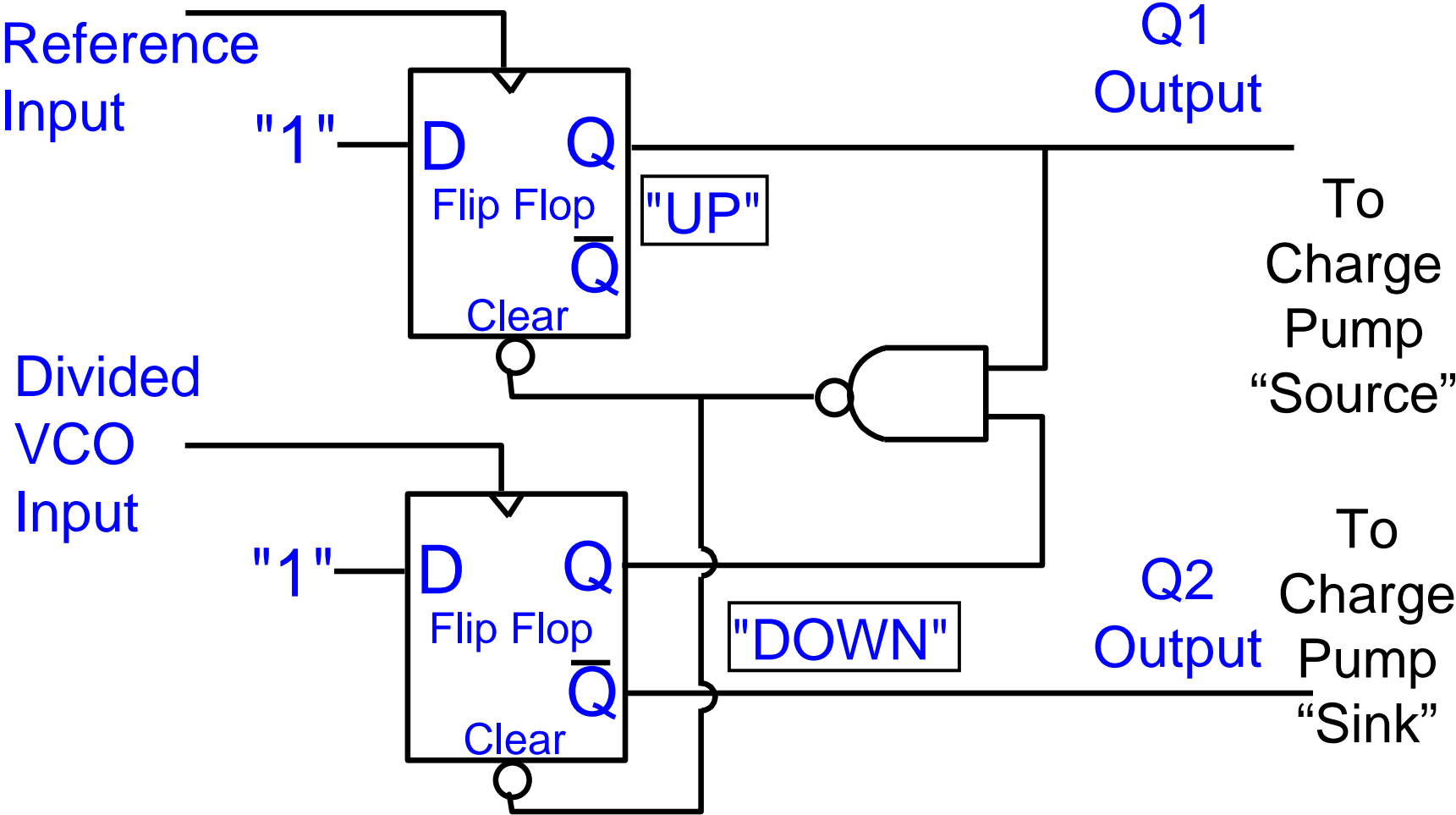
- Applying modulation within the loop
- Transient responses
- Co-simulation with a behavioral sigma-delta modulator



About Circuit Envelope

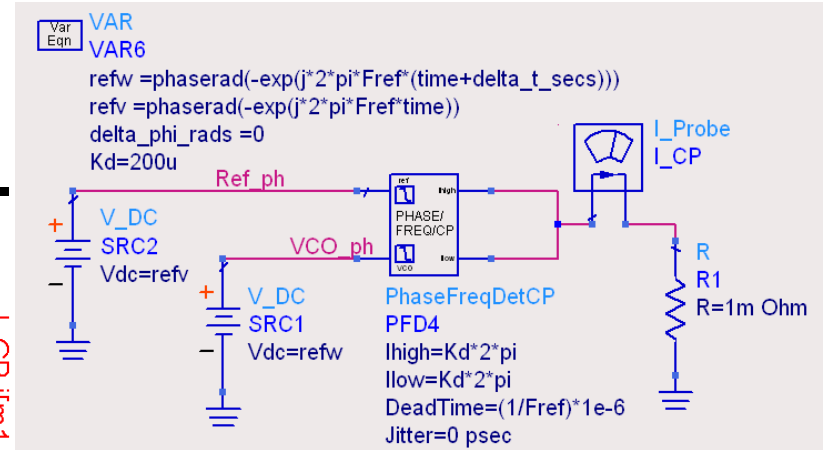
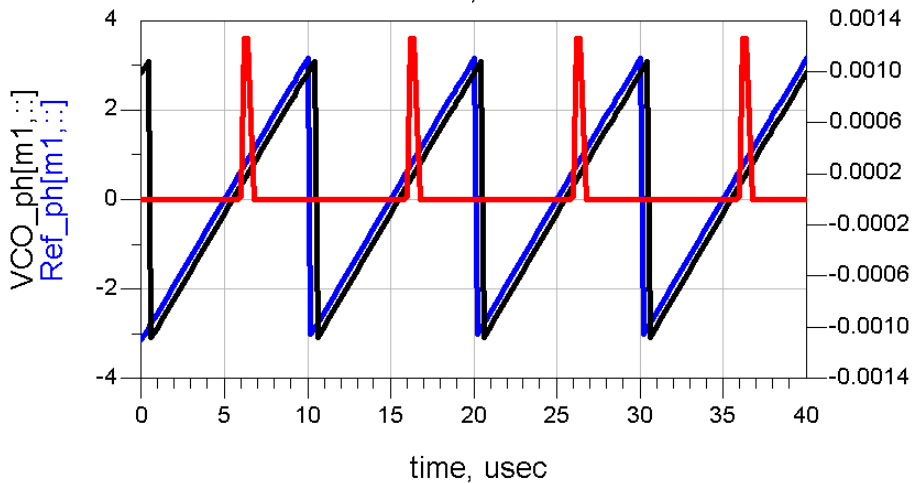
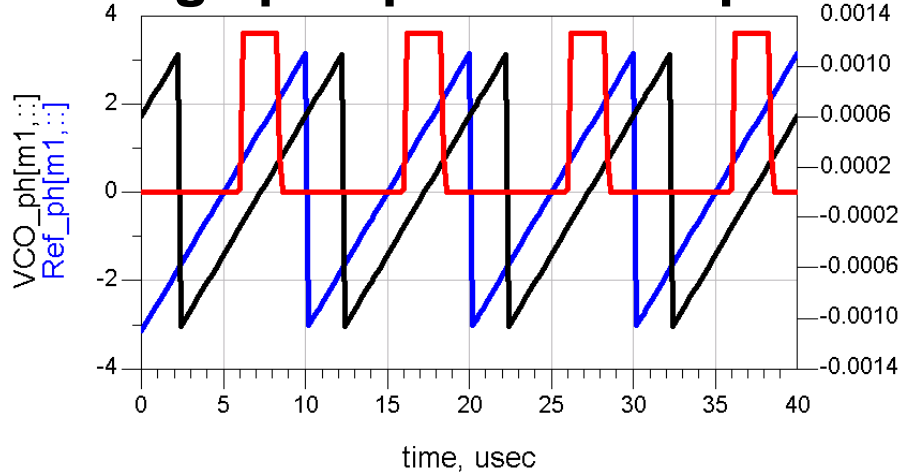


Phase/Frequency Detector Behavioral Model

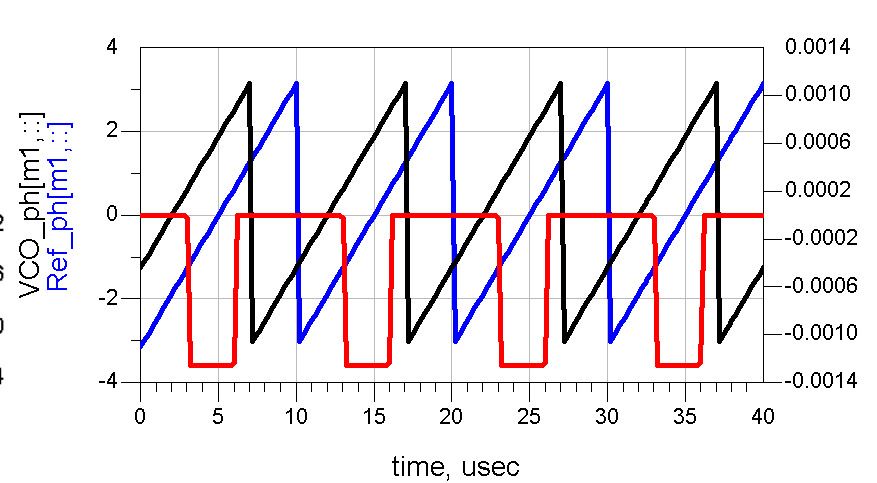


PFD Input and Charge Pump Waveforms

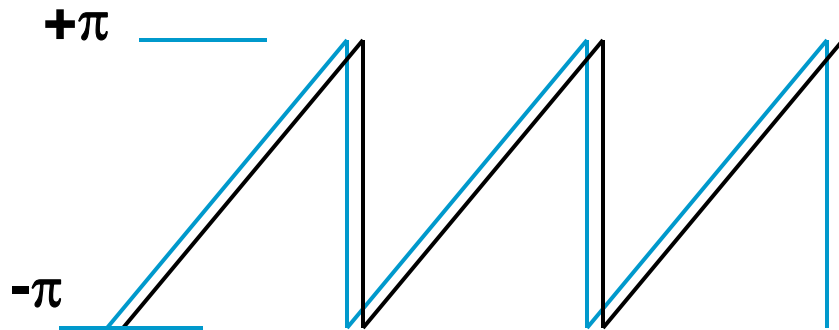
**Reference leads divided VCO.
Charge pump current is positive.**



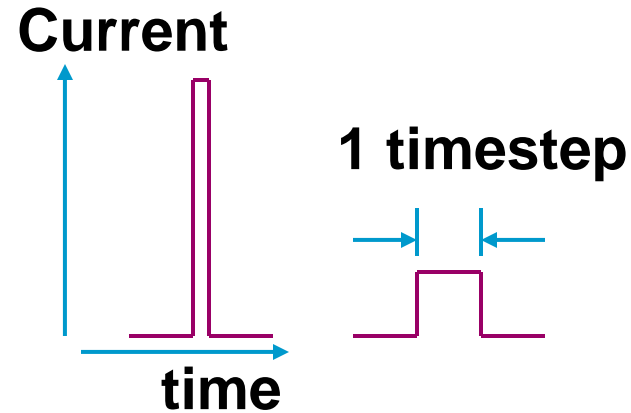
**Divided VCO leads reference.
Charge pump current is negative.**



Why are Reference and Divided VCO Signals Sawtooth Waves?



Ideally, charge pump current pulse width is equal to time difference between PFD input signals. But in simulation, this width must be a multiple of the timestep. Envelope uses interpolation to get finer resolution than the timestep. Sawtooth waves are easiest to interpolate.

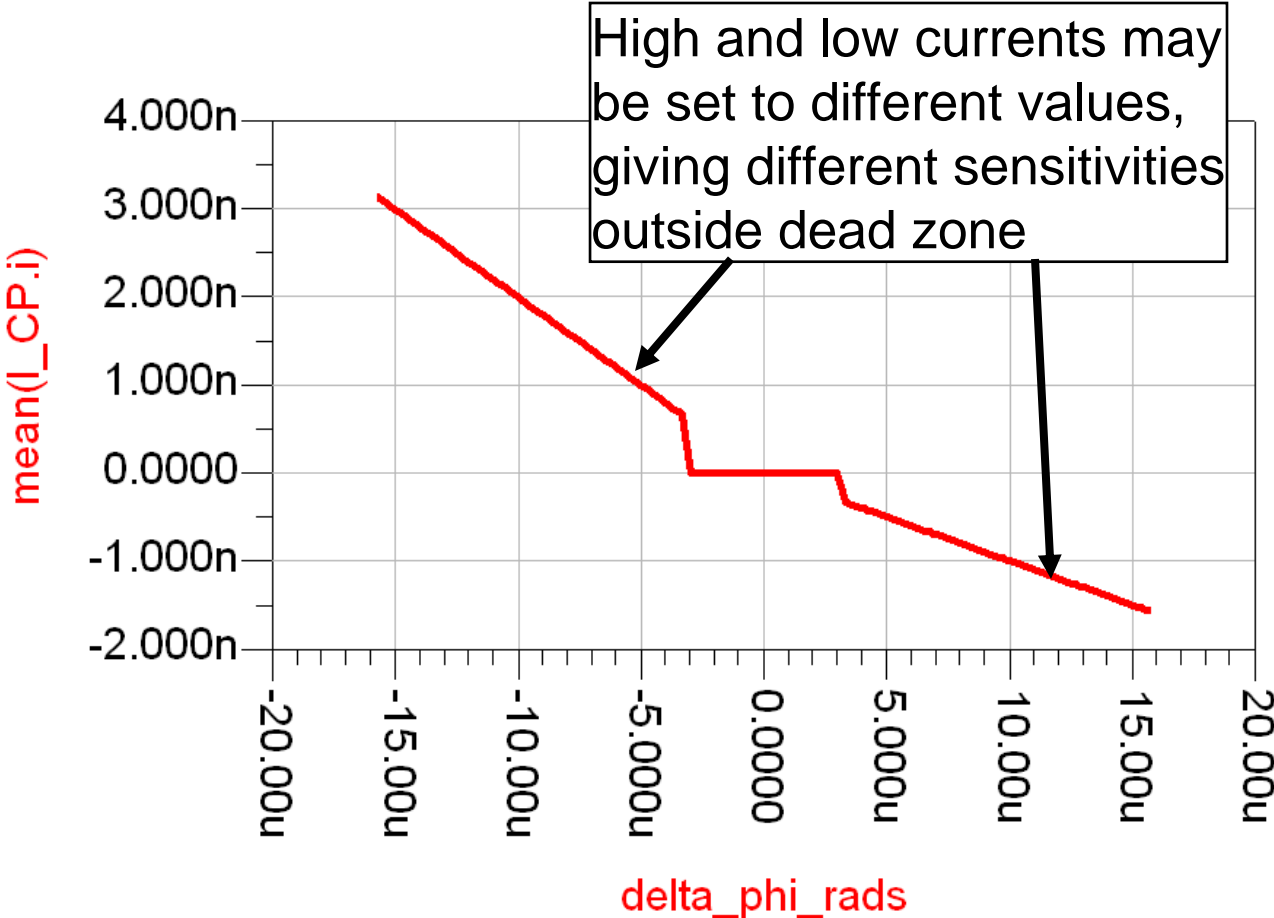


Ideal current pulse (can't be simulated)

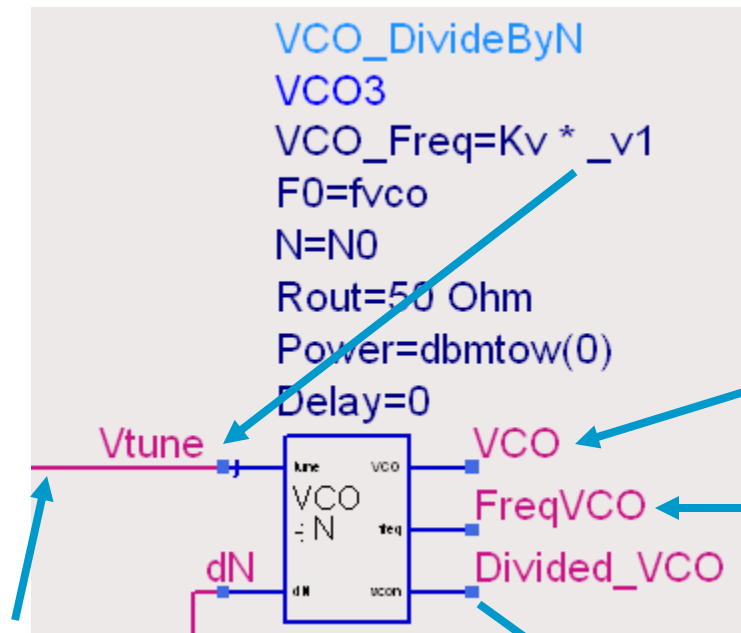
Current pulse, 1 timestep wide, amplitude reduced to give same area as ideal pulse

Phase/Frequency Detector Dead zone

Mean charge pump current versus phase difference between two input signals



VCO/Divide-By-N Behavioral Model



_v1 is the tuning voltage

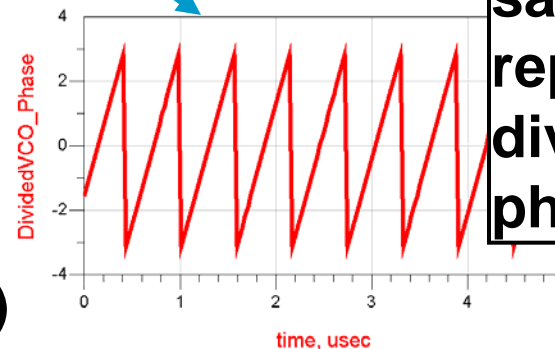
VCO output is a time-varying phasor

VCO frequency is $F0 + VCO_Freq$

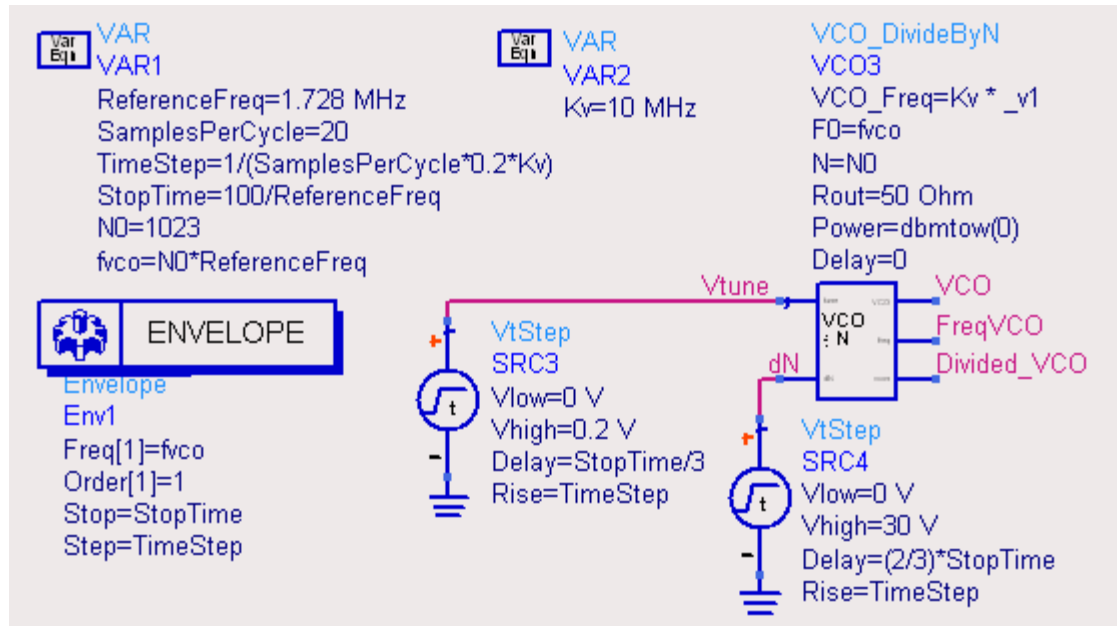
Tuning voltage output from lowpass filter

Divided VCO output frequency is $(F0 + VCO_Freq) / (N0 + dN)$

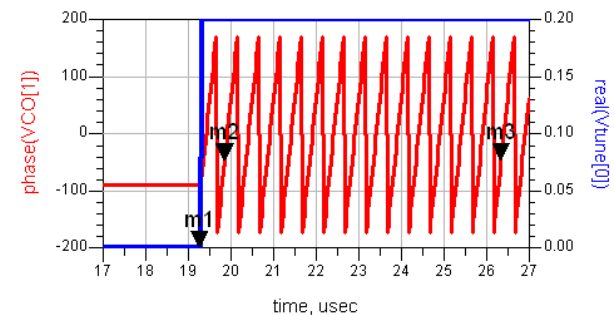
Divided output is saw tooth wave representing the divided signal phase in radians



VCO/Divide-By-N Behavioral Model



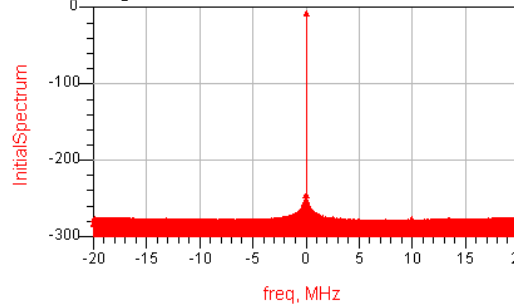
Step in Vtune, and VCO phase indicating 2 MHz increase in frequency



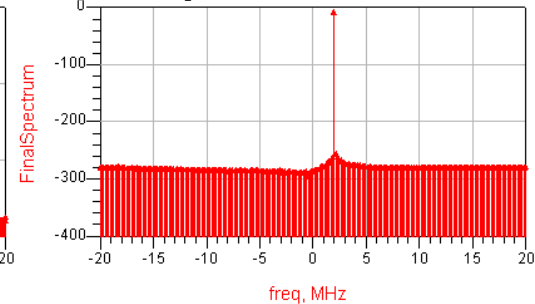
0.2 V step in Vtune forces VCO freq. to increase by 0.2 X 10 MHz

For VCO_DivideByN_Pulse component, dN inputs must be clocked.

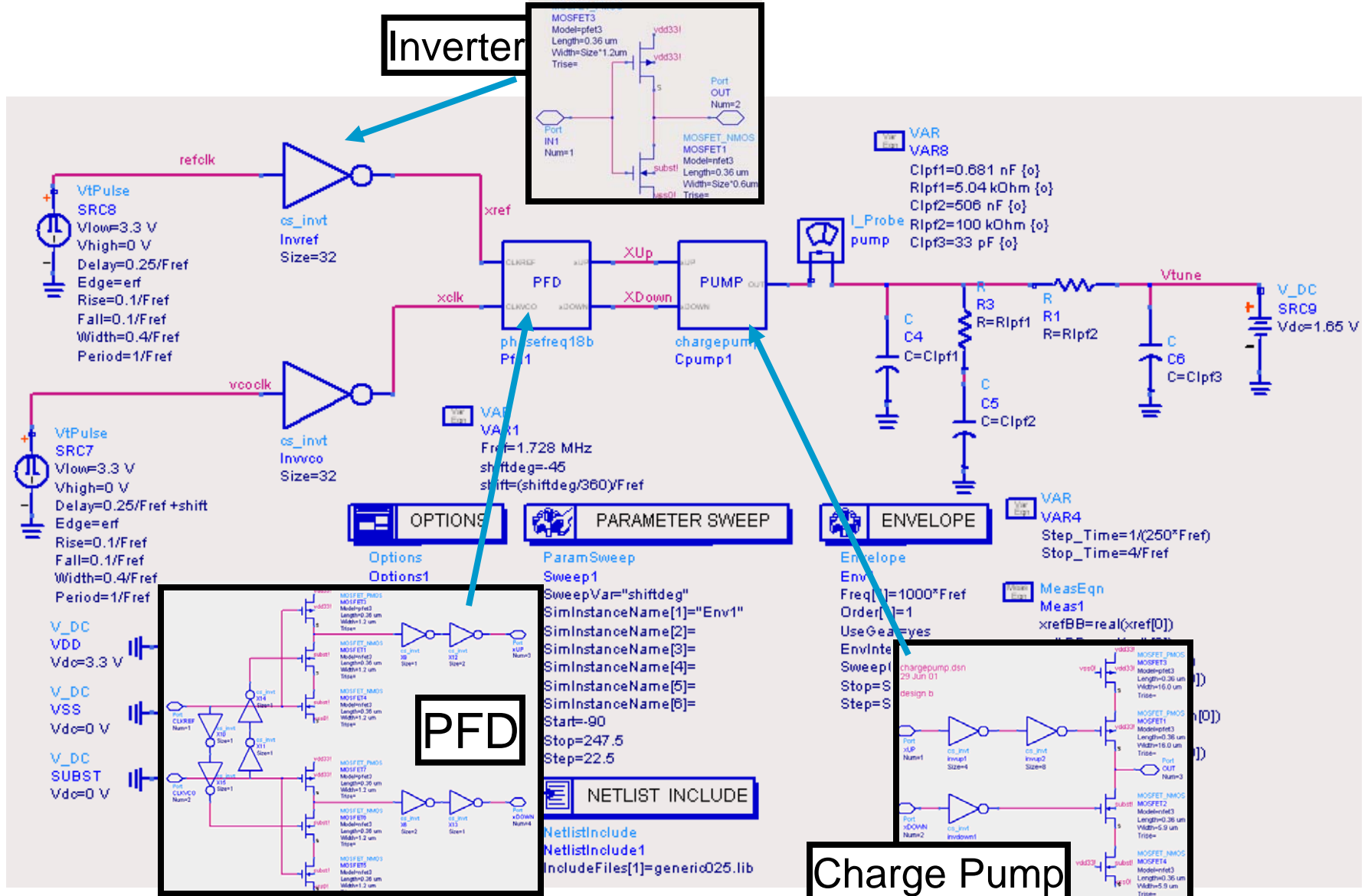
VCO spectrum w/Vtune=0



VCO spectrum w/Vtune=0.2



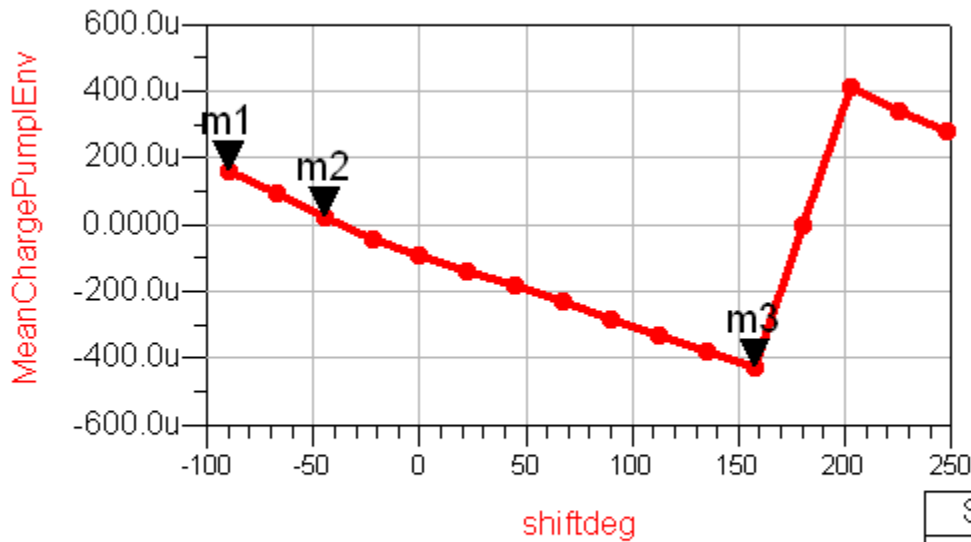
Deriving sensitivity of PFD and charge pump



Computing average sensitivity using markers

Used in behavioral PFD on next slide

Eqn MeanChargePumpEnv=mean(pumpI)



m1
shiftdeg=-90.000
MeanChargePumpEnv=1.629E-4

m2
shiftdeg=-45.000
MeanChargePumpEnv=2.174E-5

m3
shiftdeg=157.500
MeanChargePumpEnv=-4.306E-4

Sensitivity
-3.137 u

Sensitivity2
-2.234 u

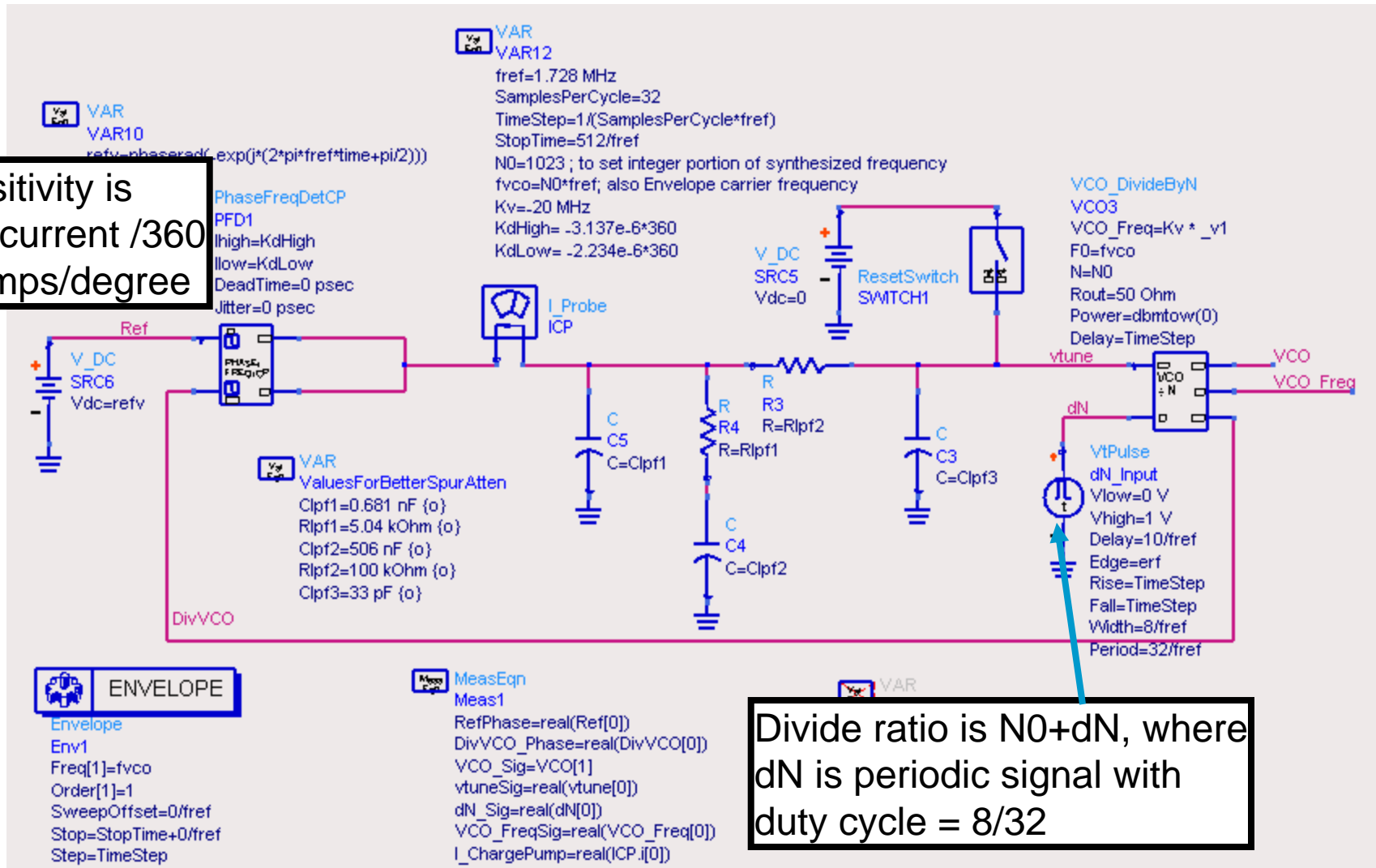
These are the average PFD/CP sensitivities in Amps/degree, computed between markers m2 and m1 and between m3 and m2.

Eqn Sensitivity=(m2-m1)/(indep(m2)-indep(m1))

Eqn Sensitivity2=(m3-m2)/(indep(m3)-indep(m2))

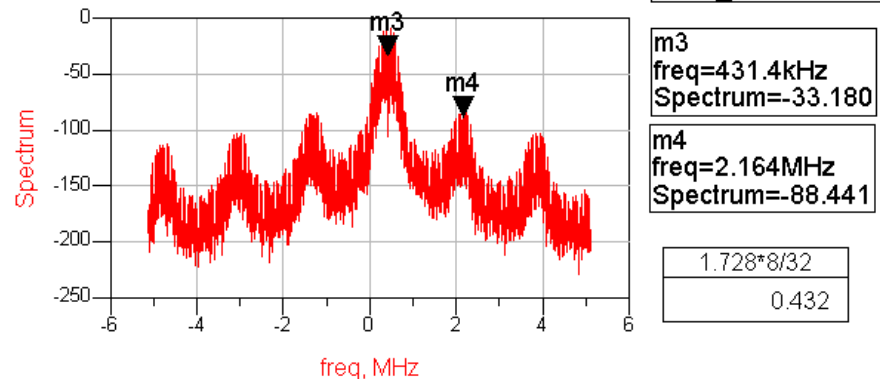
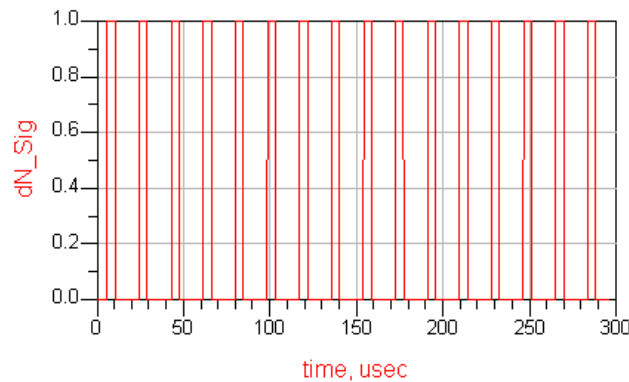
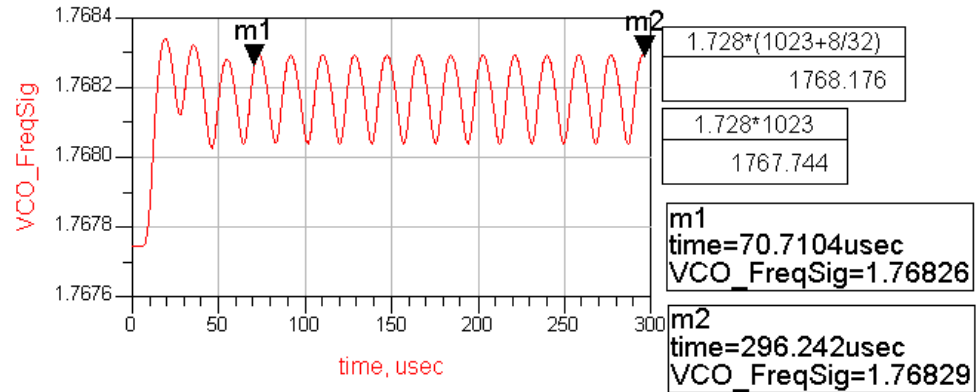
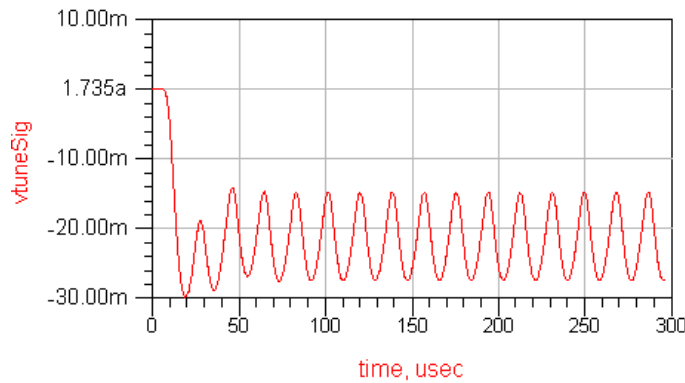
An all-behavioral-model, fractional-N PLL

Sensitivity is
“on” current /360
in Amps/degree



Divide ratio is $N0+dN$, where
 dN is periodic signal with
duty cycle = $8/32$

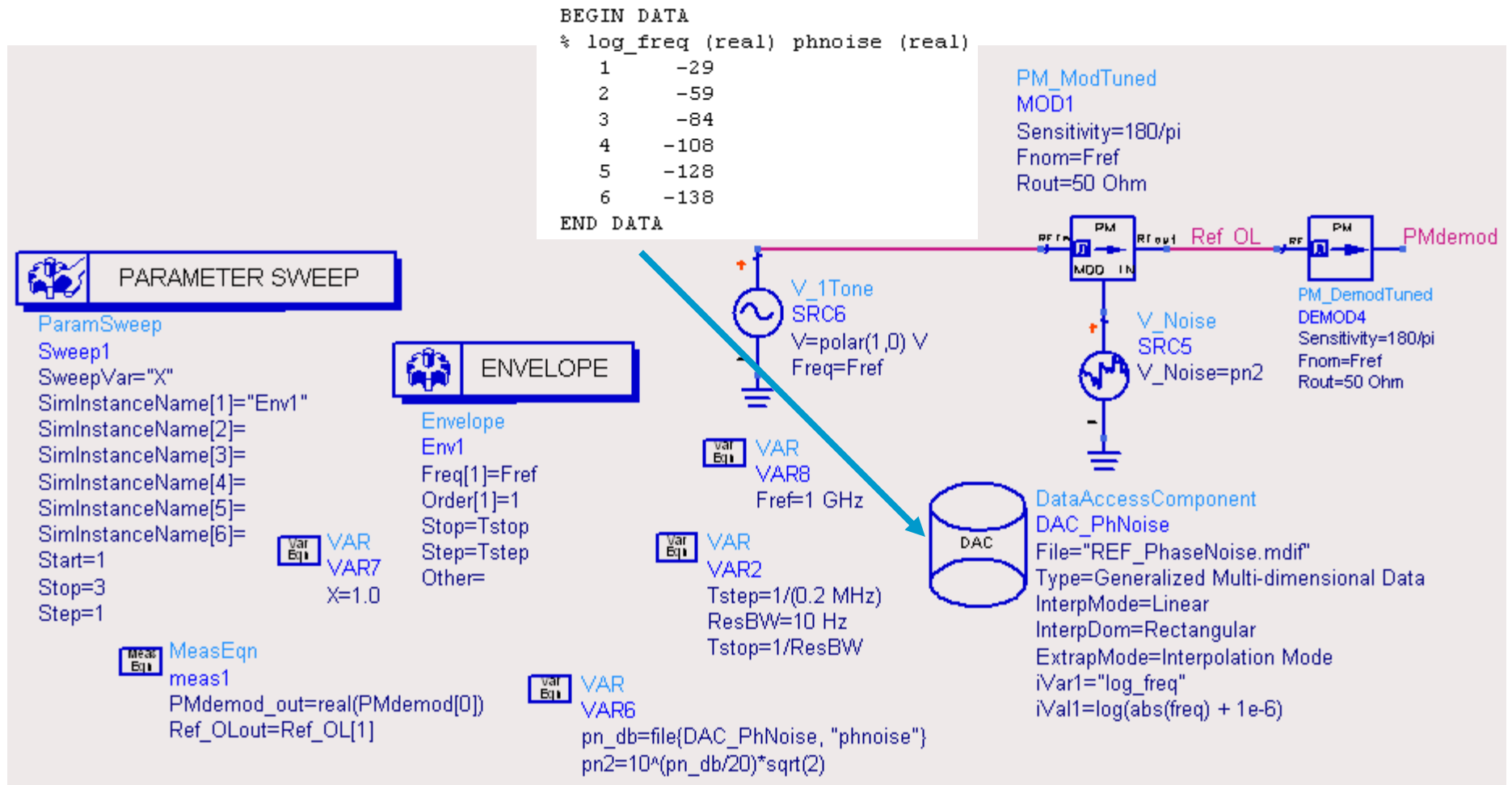
VCO spectrum has large spurs



$\text{Eqn } F_{sp} = 10.24 \text{ MHz}$ $\text{Eqn } F_{center} = 0$

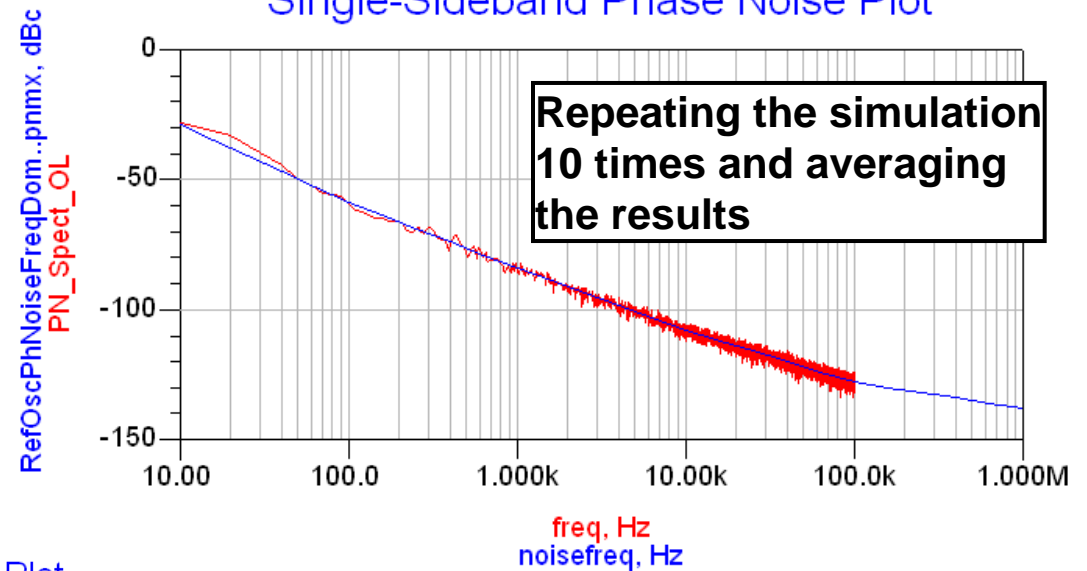
$\text{Eqn } \text{Spectrum} = \text{dB}(\text{fs}(\text{VCO_Sig}, F_{center} - F_{sp}/2, F_{center} + F_{sp}/2, 4 \cdot 1024, \text{"Hanning"}, \text{indep}(m1), \text{indep}(m2)))$

Including VCO phase noise in the simulation

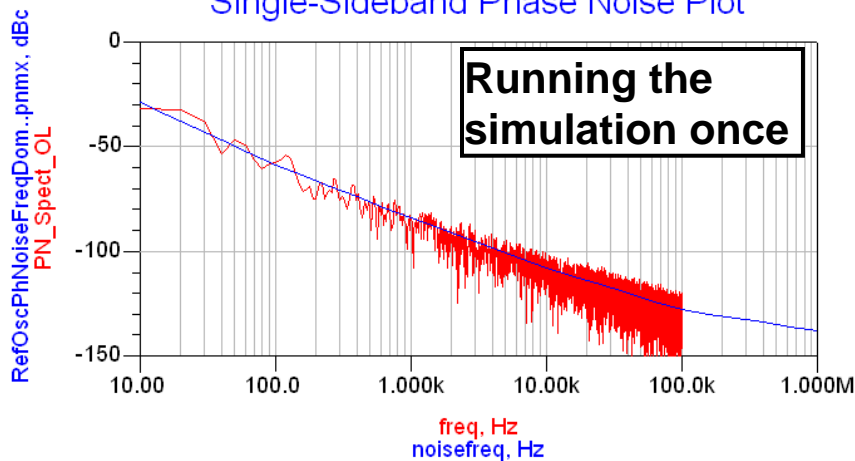


Simulation results, VCO only

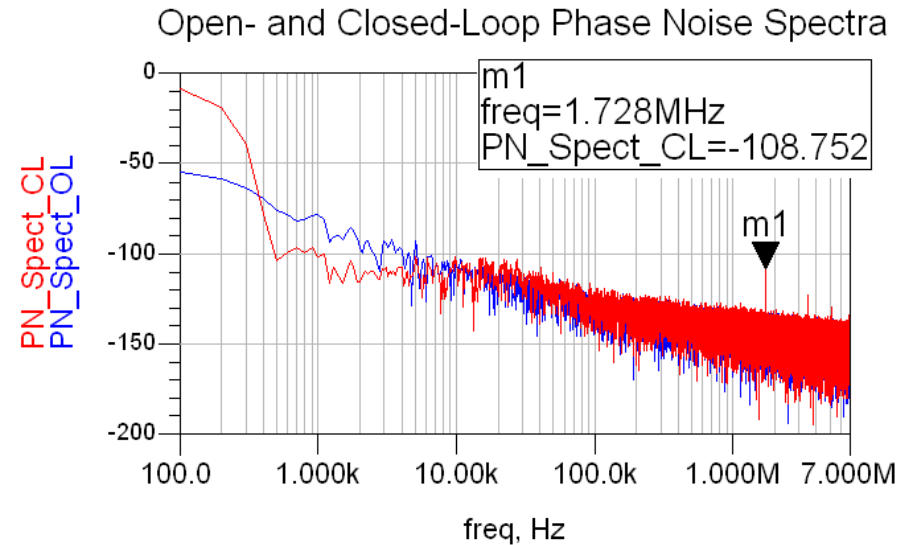
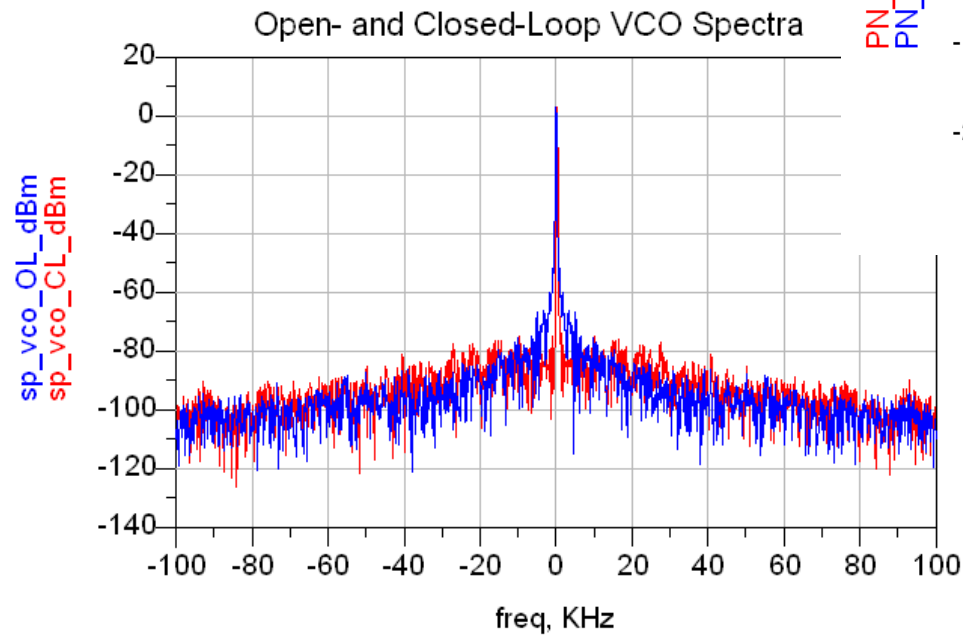
Single-Sideband Phase Noise Plot



Single-Sideband Phase Noise Plot

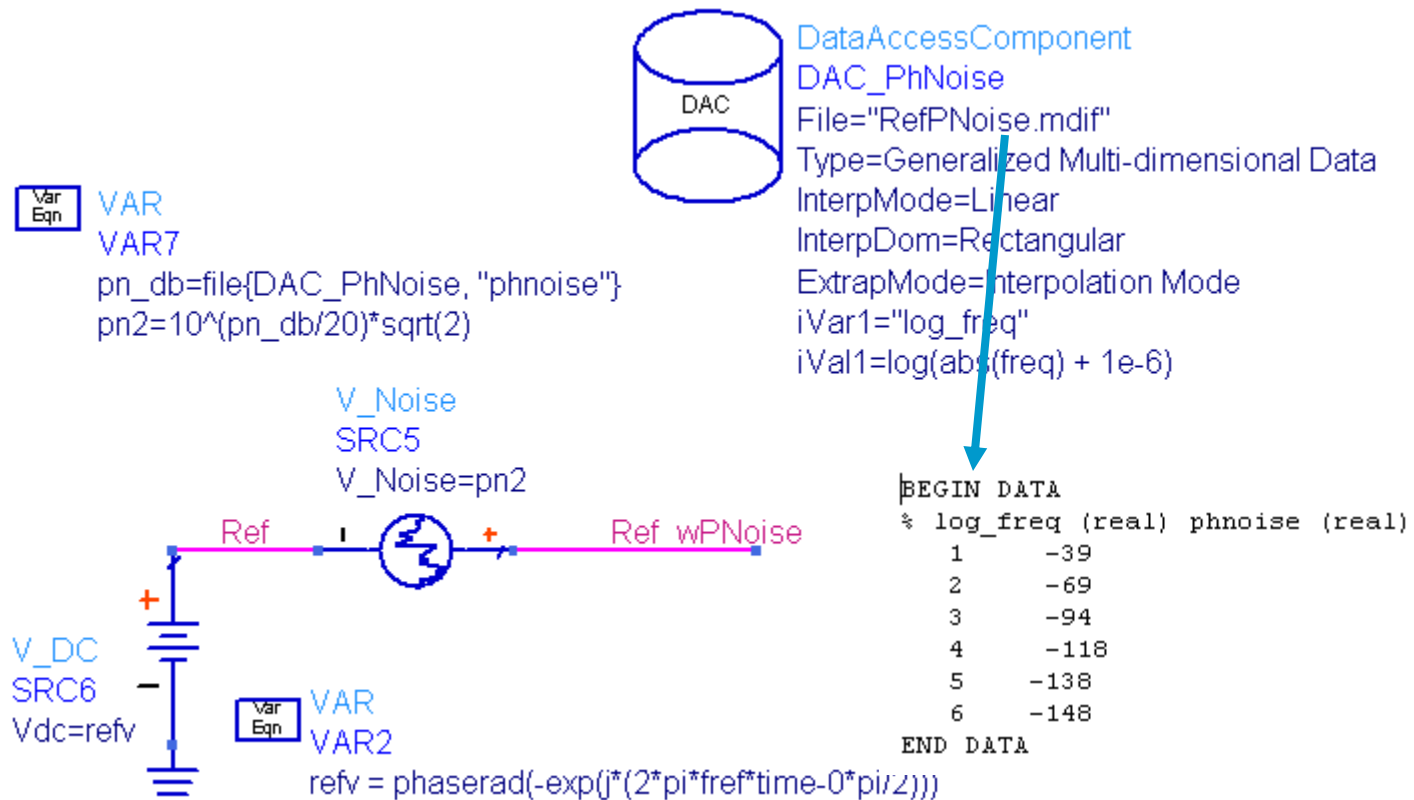


Open- and closed-loop phase noise results with reference spurs

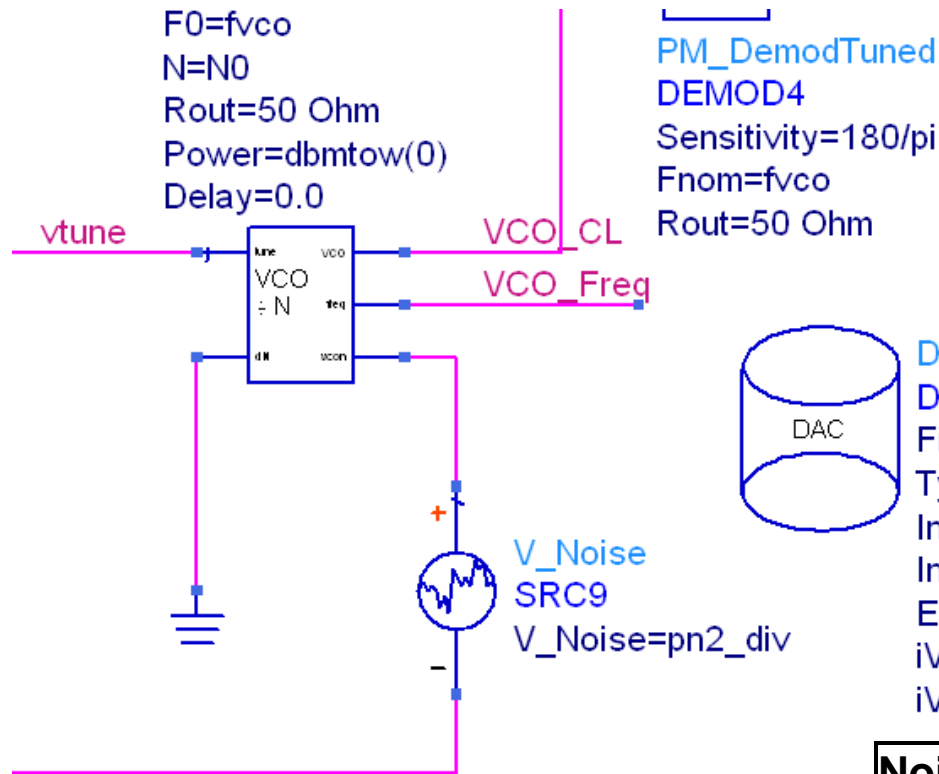


Adding phase noise to the reference source

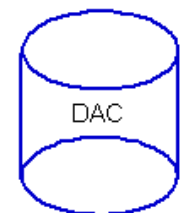
This is simpler, because the reference “signal” is actually the phase of the reference source. Just add the phase noise to the reference phase.



Adding the frequency divider phase noise (2)



Since the divided output is a phase, can just sum the phase noise at the output.



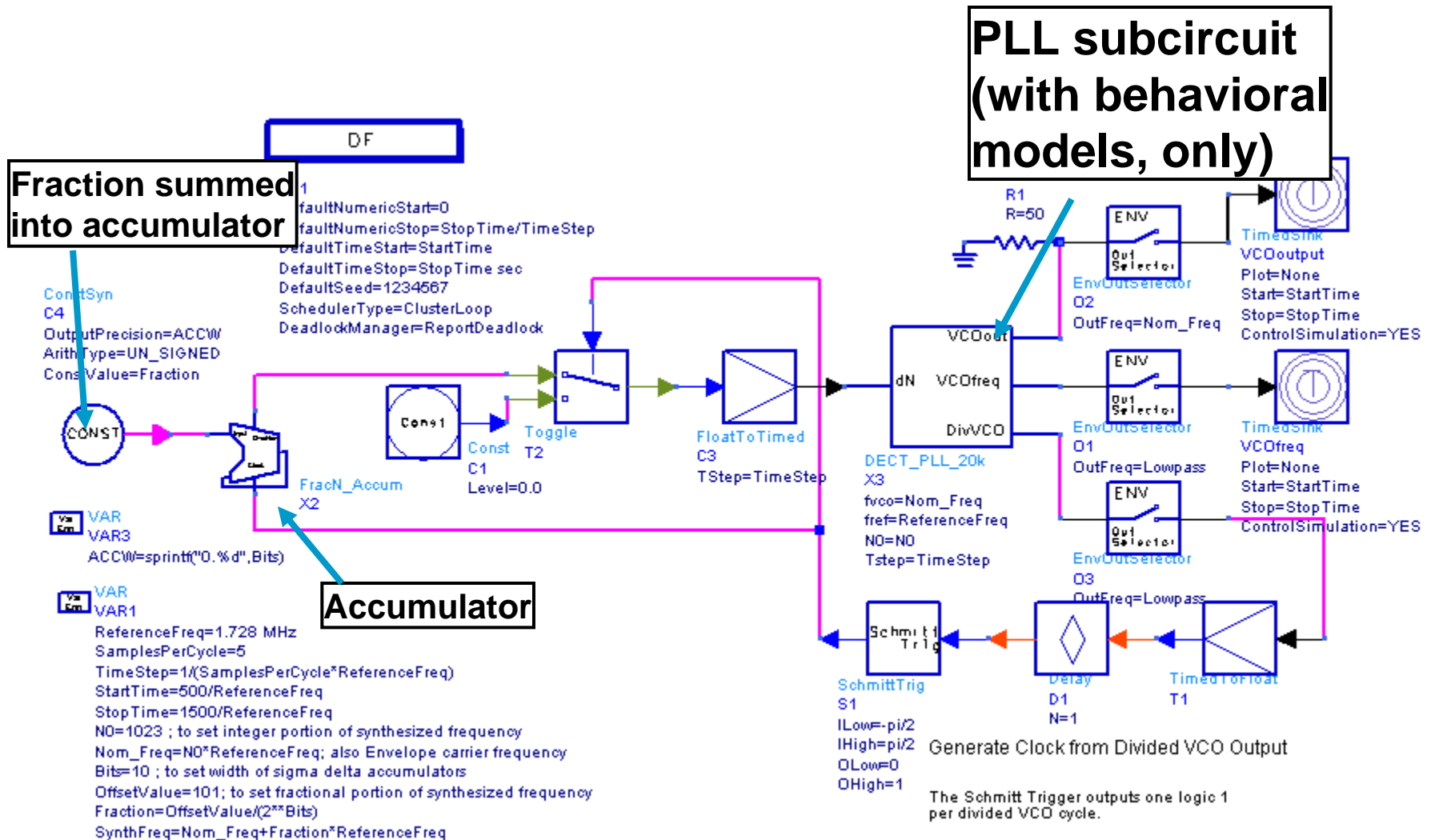
DataAccessComponent
 DAC_DivPhNoise
 File="DivPNoise.mdif"
 Type=Generalized Multi-dimensional Data
 InterpMode=Linear
 InterpDom=Rectangular
 ExtrapMode=Interpolation Mode
 iVar1="log_freq"
 iVal1=log(abs(freq) + 1e-6)

Noise is not multiplied by the divide ratio.

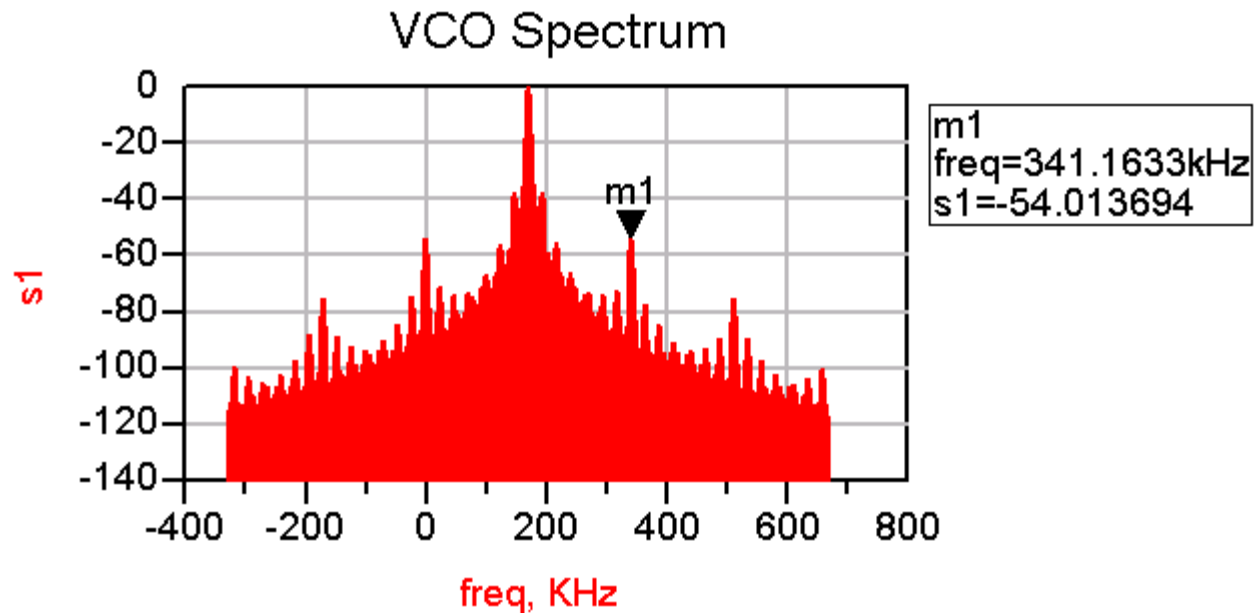
Var Eqn

VAR
 VAR10
 $pn_div_db=file\{DAC_DivPhNoise, "phnoise"\}$
 $pn2_div=10^{(pn_div_db/20)}*sqrt(2)$

Fractional-N Synthesizer PLL Top-Level Ptolemy Schematic



Fractional-N Simulation Results

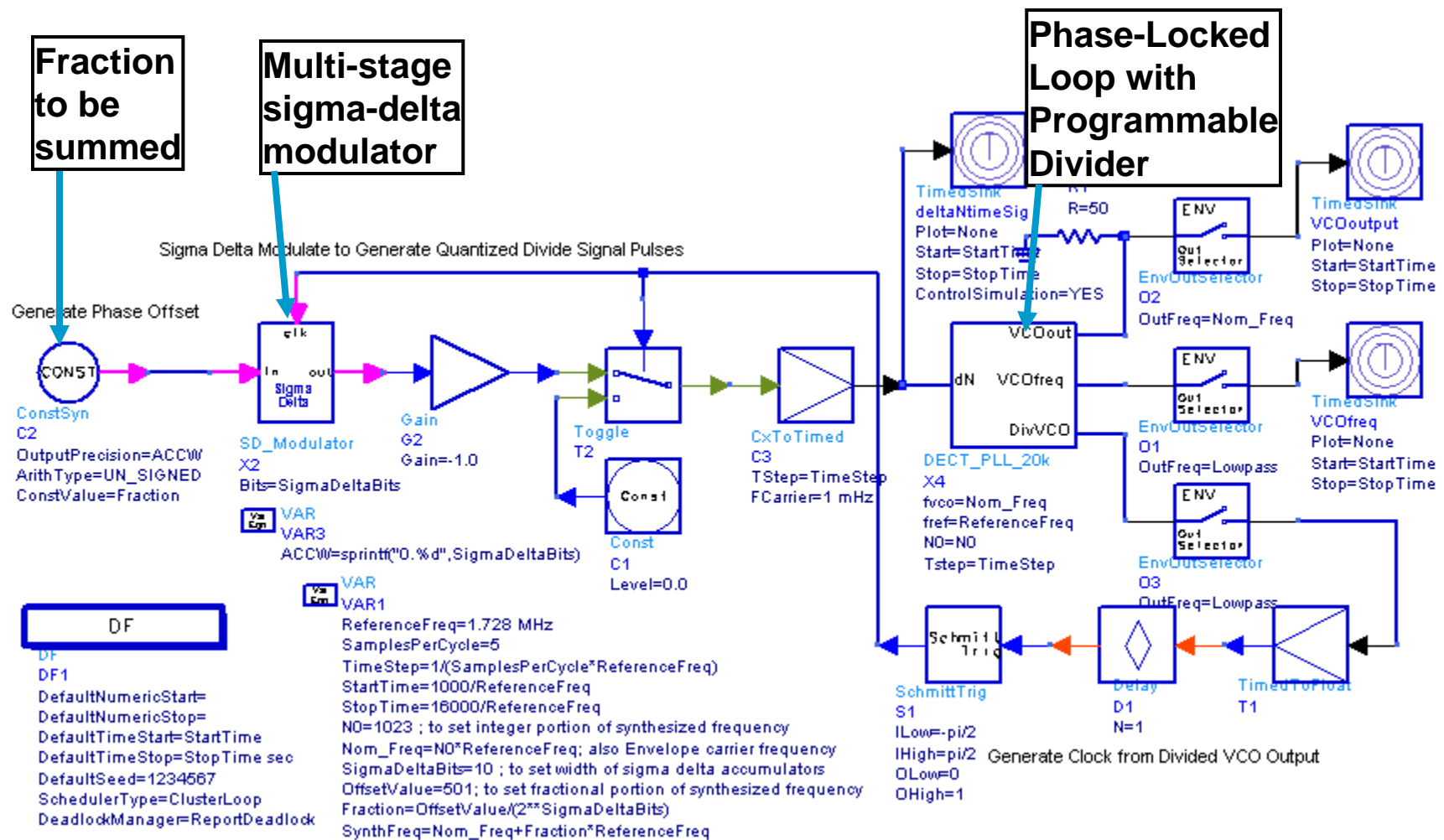


**0 Hz corresponds to $N0 \cdot \text{ReferenceFreq} = 1023 \cdot (1.728 \text{ MHz})$
 $= 1.767744 \text{ GHz}$**

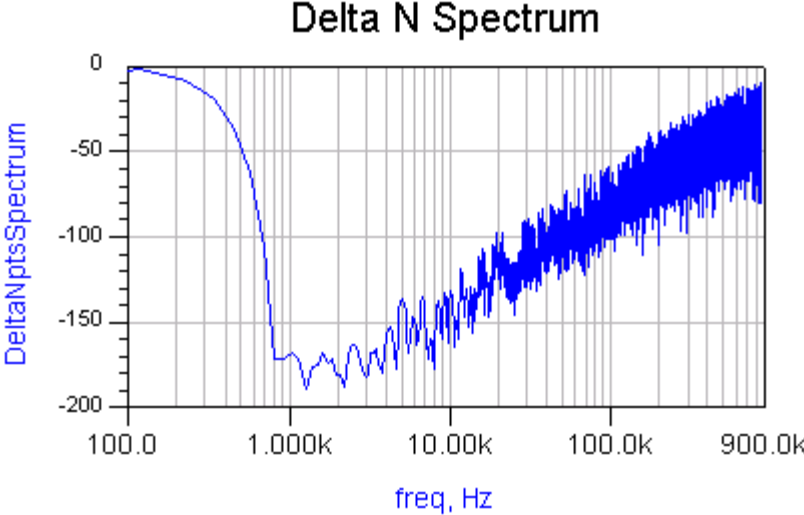
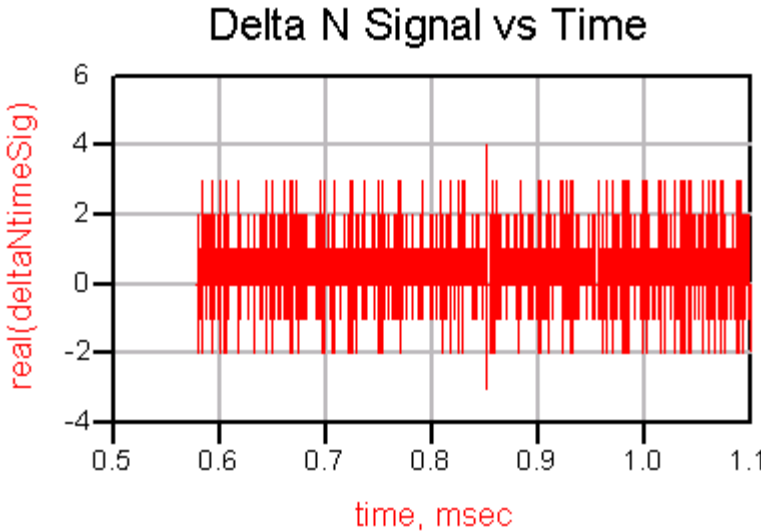
Fraction = $101 / (2^{10}) = 0.098633$

**Synthesized frequency = $(N0 + \text{Fraction}) \cdot \text{ReferenceFreq}$
 $= 1.767744 \text{ GHz} + 0.098633 \cdot 1.728 \text{ MHz}$
 $= 1.767744 \text{ GHz} + 170.438 \text{ kHz}$**

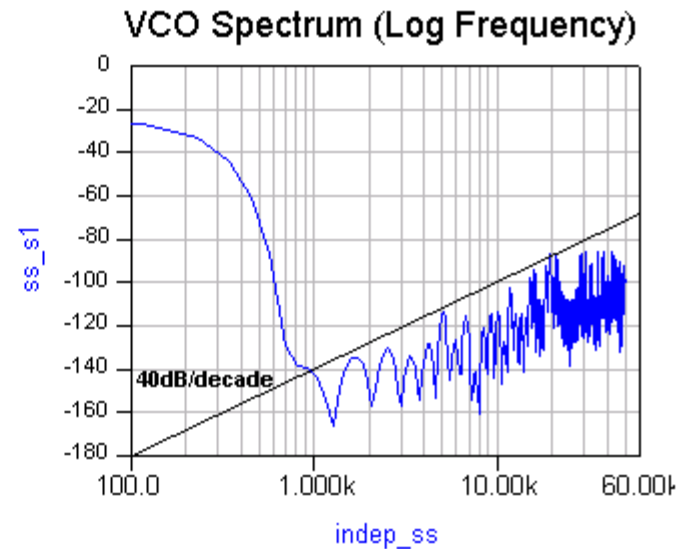
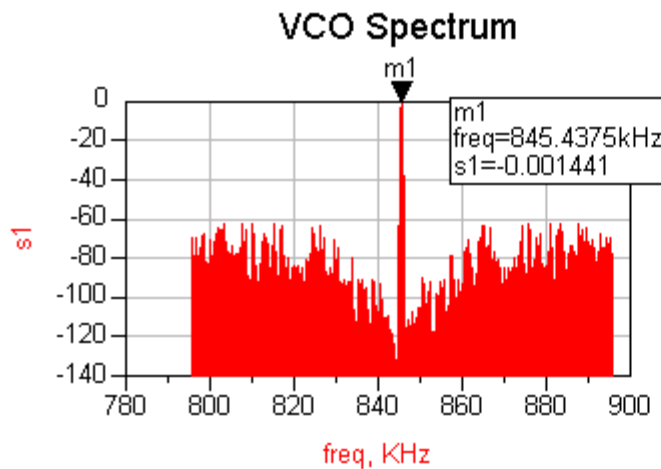
Simulating PLL with Multi-Stage Sigma-Delta Modulator



Delta N Signal and Spectrum



Resulting VCO Spectrum

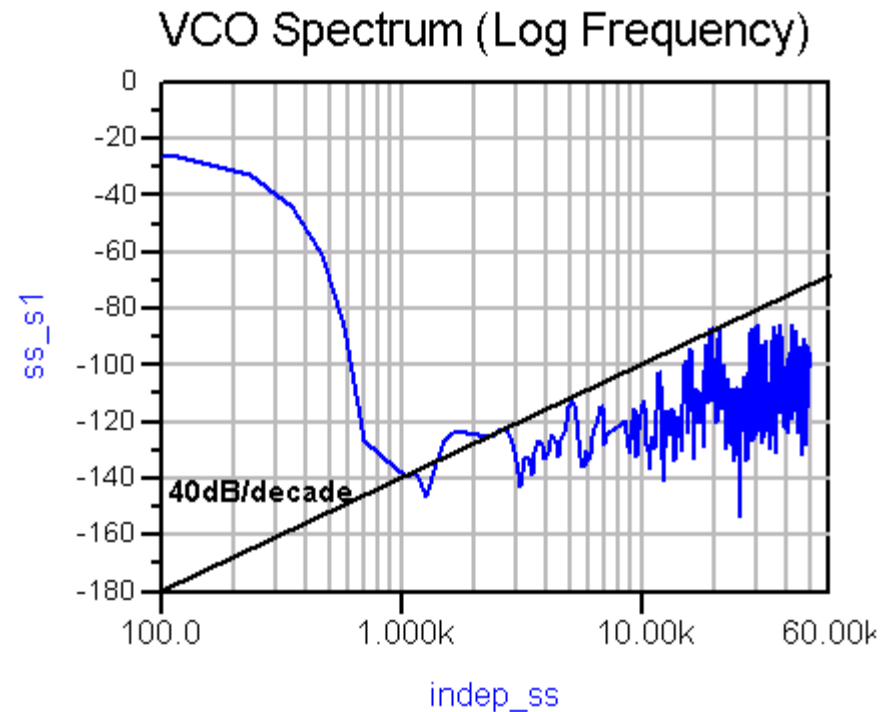
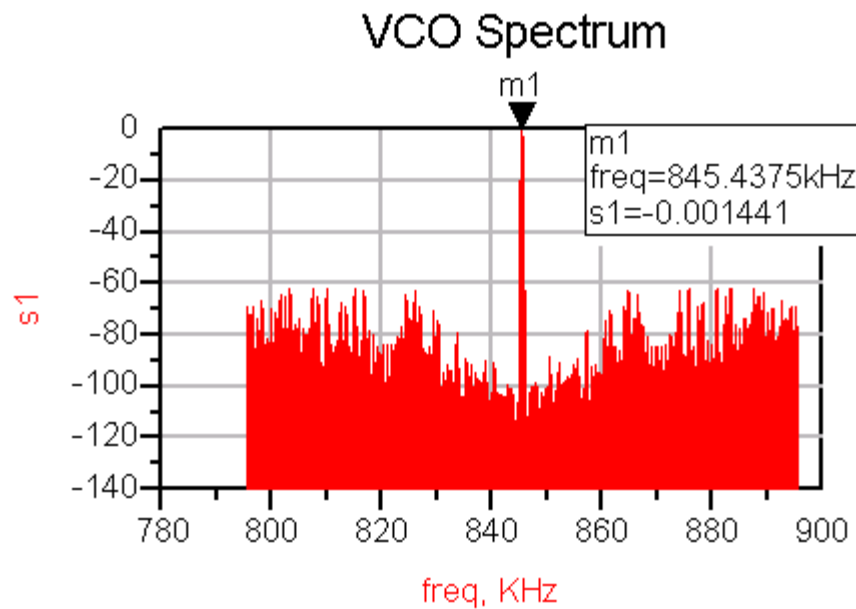


**0 Hz corresponds to $N0 \cdot \text{ReferenceFreq} = 1023 \cdot (1.728 \text{ MHz})$
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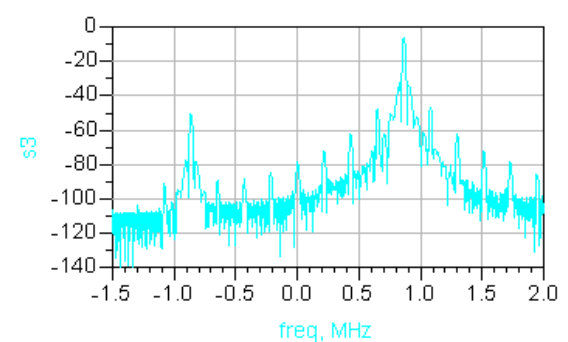
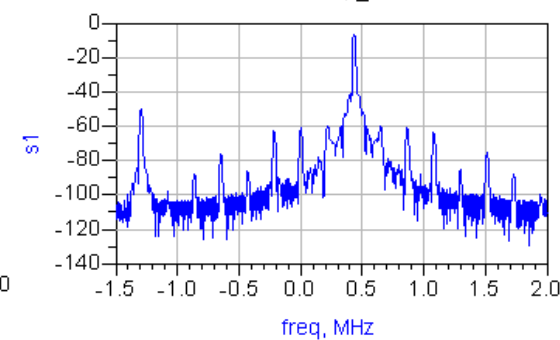
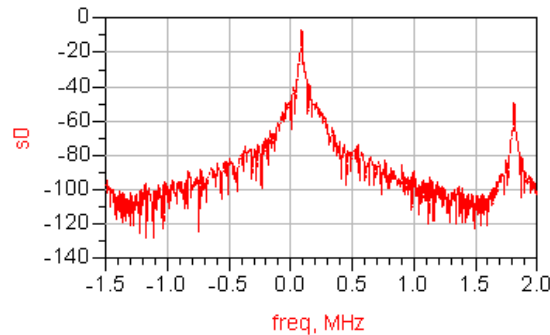
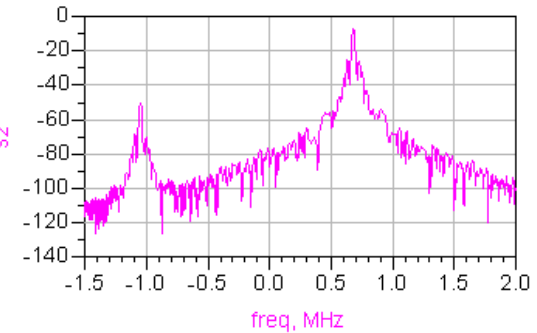
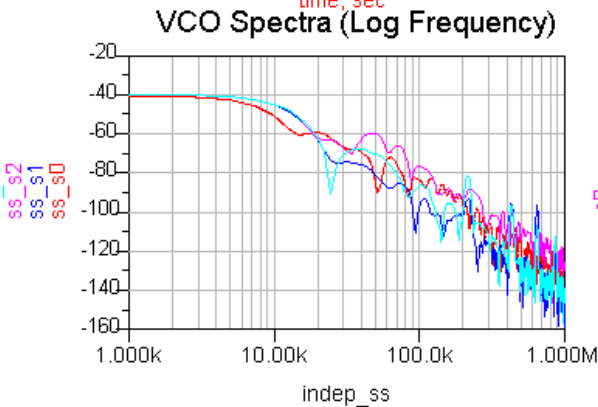
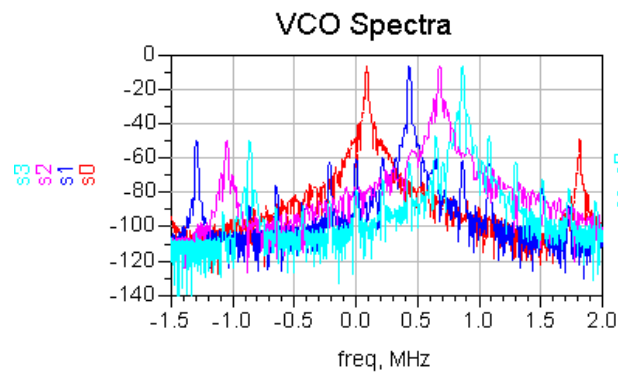
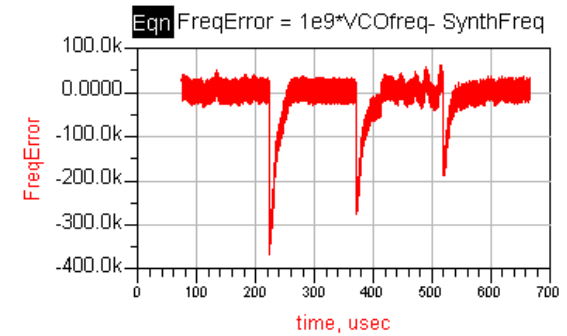
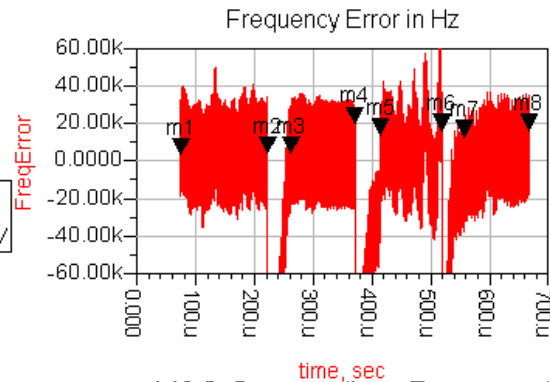
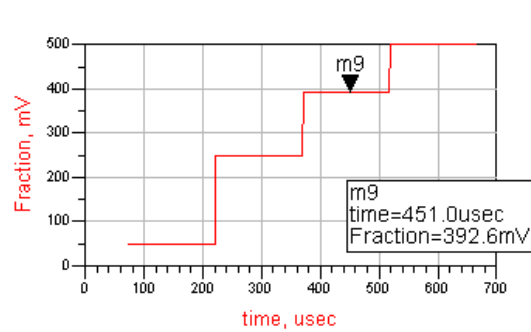
Fraction = $501 / (2^{10}) = 0.489258$

**Synthesized frequency = $(N0 + \text{Fraction}) \cdot \text{ReferenceFreq}$
 $= 1.767744 \text{ GHz} + 0.489258 \cdot 1.728 \text{ MHz}$
 $= 1.767744 \text{ GHz} + 845.438 \text{ kHz}$**

VCO Spectrum, within Sigma-Delta PLL, Including VCO's Phase Noise

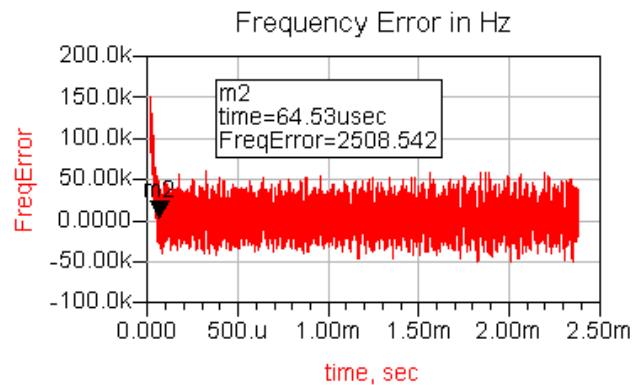


Stepping fraction, with transistor PFD/CP



Fraction constant, with transistor PFD/CP

Eqn FreqError = 1e9*VCOfreq- SynthFreq



Longer stop time gives better close-in resolution

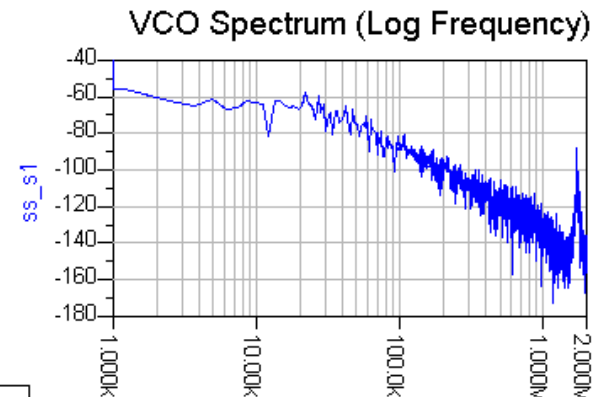
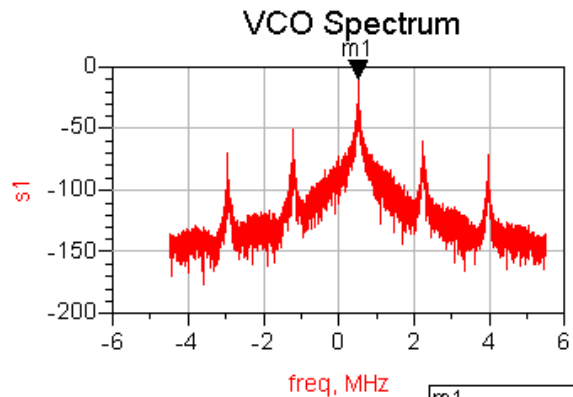
Fraction
0.294 / 0.000

Eqn Fc = real(Fraction*ReferenceFreq)

Eqn SynthFreq = real(N0*ReferenceFreq) + Fc

The VCO spectrum is plotted with the x-axis relative to the envelope analysis frequency at N0*ReferenceFreq. So the VCO is really at SynthFreq, which is Fc Hz above N0*ReferenceFreq.

real(N0*ReferenceFreq)	+	Fc	=	
1.767744 G		507.9375 k		
				SynthFreq
				1.768252 G



Eqn Fsp = 10 MHz

m1
freq=507.9375kHz
s1=-9.790311

Eqn s1=dBm(fs(VCOoutput/2,Fc-Fsp/2,Fc+Fsp/2,8*1024-1,,"Kaiser",win_param,indep(m2)))

Review and Summary

What ADS is able to simulate, concerning PLLs

Basic concepts about Envelope simulation and PLL component behavioral modeling

Deriving sensitivity of a transistor-level phase/frequency detector and charge pump

An all-behavioral-model PLL

How to add phase noise from various components

Open- and closed-loop phase noise and spurs

Running a fractional-N simulation

Using a sigma delta modulator to generate the divide ratio

Appendix: More information on Sigma-Delta Modulator simulation

Modeling the Accumulator

DF

DF
 DF1
 DefaultNumericStart=0
 DefaultNumericStop=50
 DefaultTimeStart=0 sec
 DefaultTimeStop=50 sec
 DefaultSeed=1234567
 OutVar="Fraction SigmaDeltaBits OffsetValue Bits"
 SchedulerType=ClusterLoop
 DeadlockManager=ReportDeadlock

VAR
 VAR1

SigmaDeltaBits=10 ; to set width of sigma delta accumulators
 OffsetValue=100; to set fractional portion of synthesized frequency
 Fraction=OffsetValue/(2**SigmaDeltaBits)

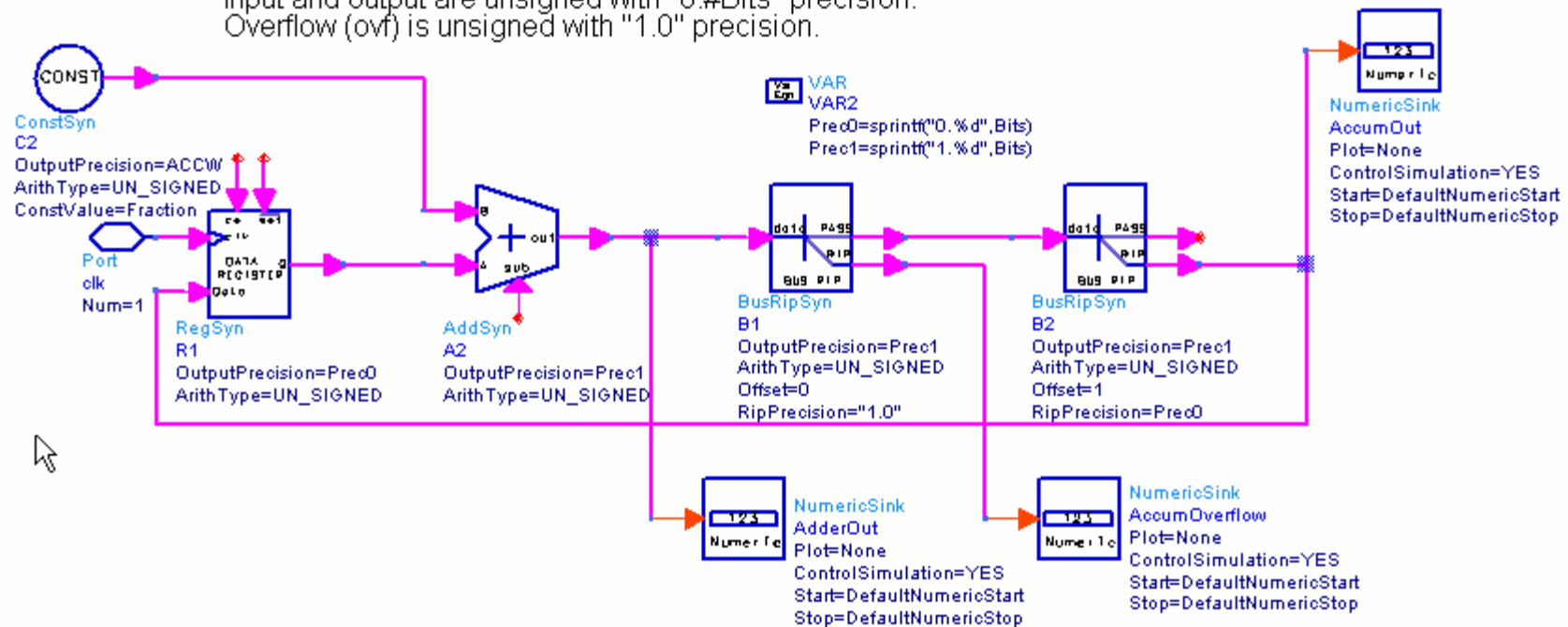
VAR
 VAR4

Bits=SigmaDeltaBits

VAR
 VAR3

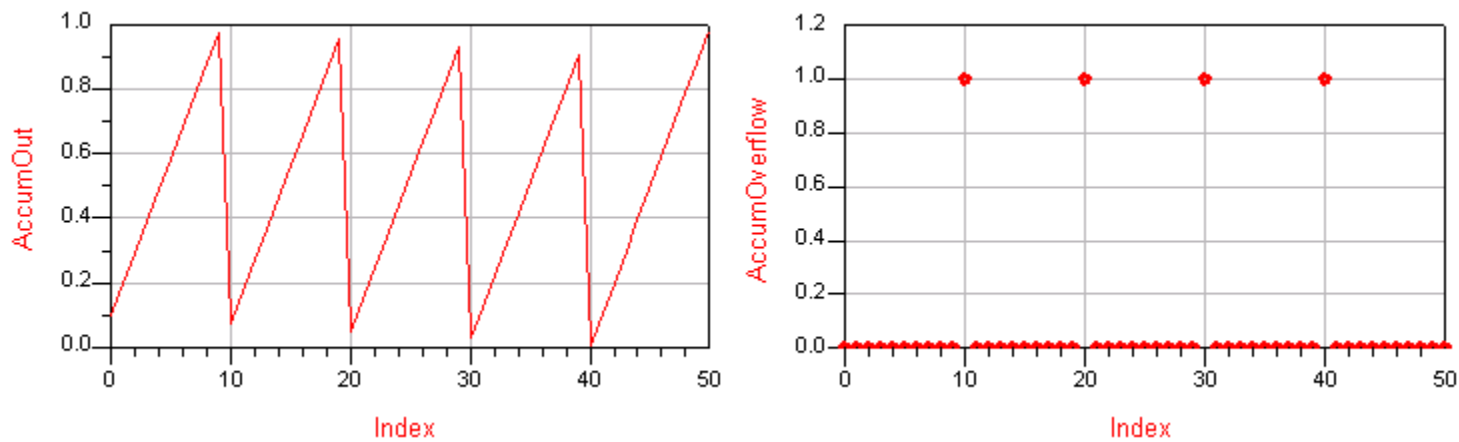
ACCW=sprintf("0. %d", SigmaDeltaBits)

An accumulator with overflow output.
 Input and output are unsigned with "0.#Bits" precision.
 Overflow (ovf) is unsigned with "1.0" precision.



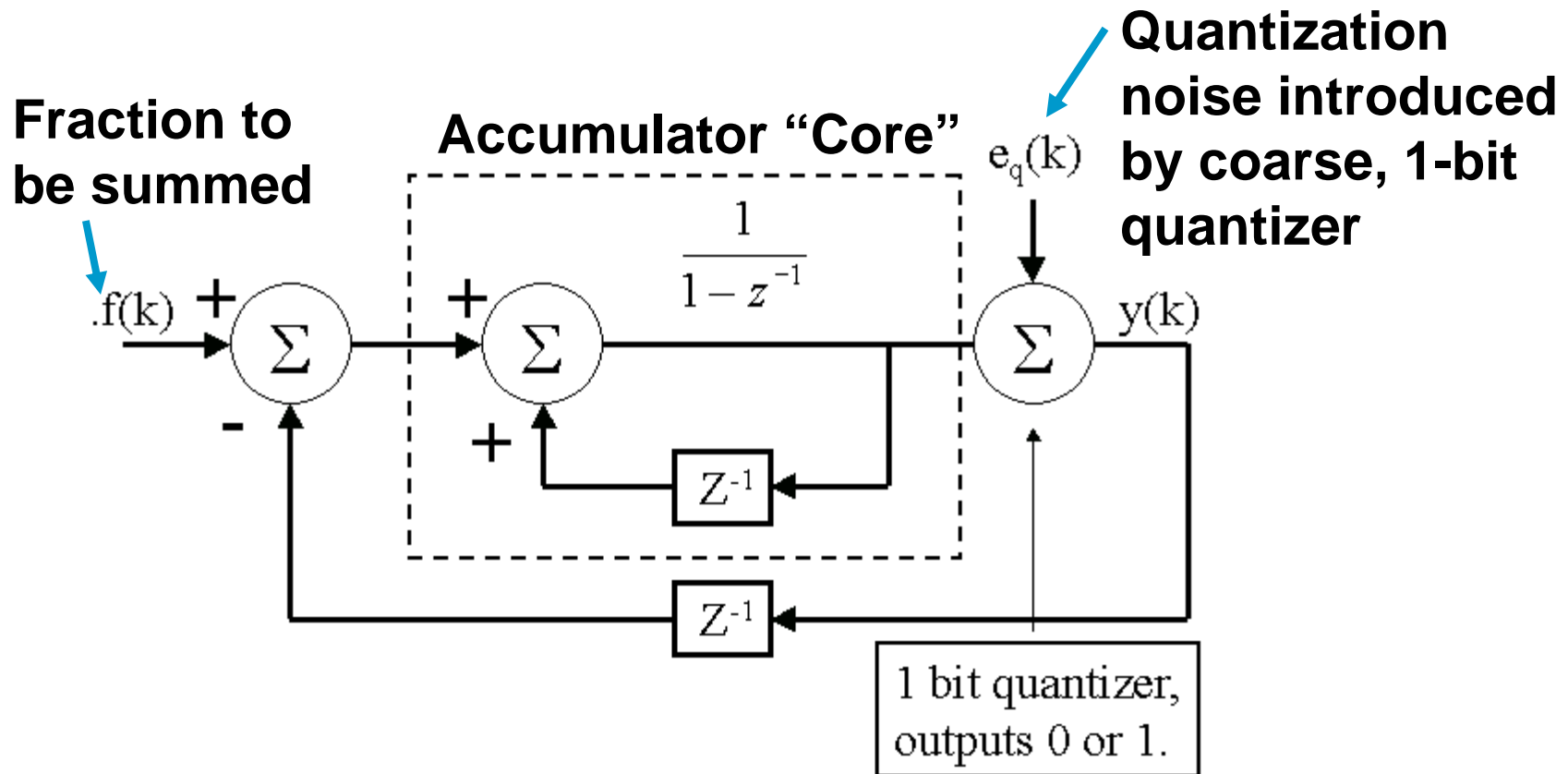
Accumulator Simulation Results

Fraction that is summed is $100/(2^{10})$, so the accumulator overflows about once every 10 clock cycles



Index	AccumOut	AccumOverflow	AdderOut
0	0.09765625000	0.00000000000	0.09765625000
1	0.19531250000	0.00000000000	0.19531250000
2	0.29296875000	0.00000000000	0.29296875000
3	0.39062500000	0.00000000000	0.39062500000
4	0.48828125000	0.00000000000	0.48828125000
5	0.58593750000	0.00000000000	0.58593750000
6	0.68359375000	0.00000000000	0.68359375000
7	0.78125000000	0.00000000000	0.78125000000
8	0.87890625000	0.00000000000	0.87890625000
9	0.97656250000	0.00000000000	0.97656250000
10	0.07421875000	1.00000000000	1.07421875000
11	0.17187500000	0.00000000000	0.17187500000
12	0.26953125000	0.00000000000	0.26953125000

Using a Sigma-Delta Modulator as an Accumulator



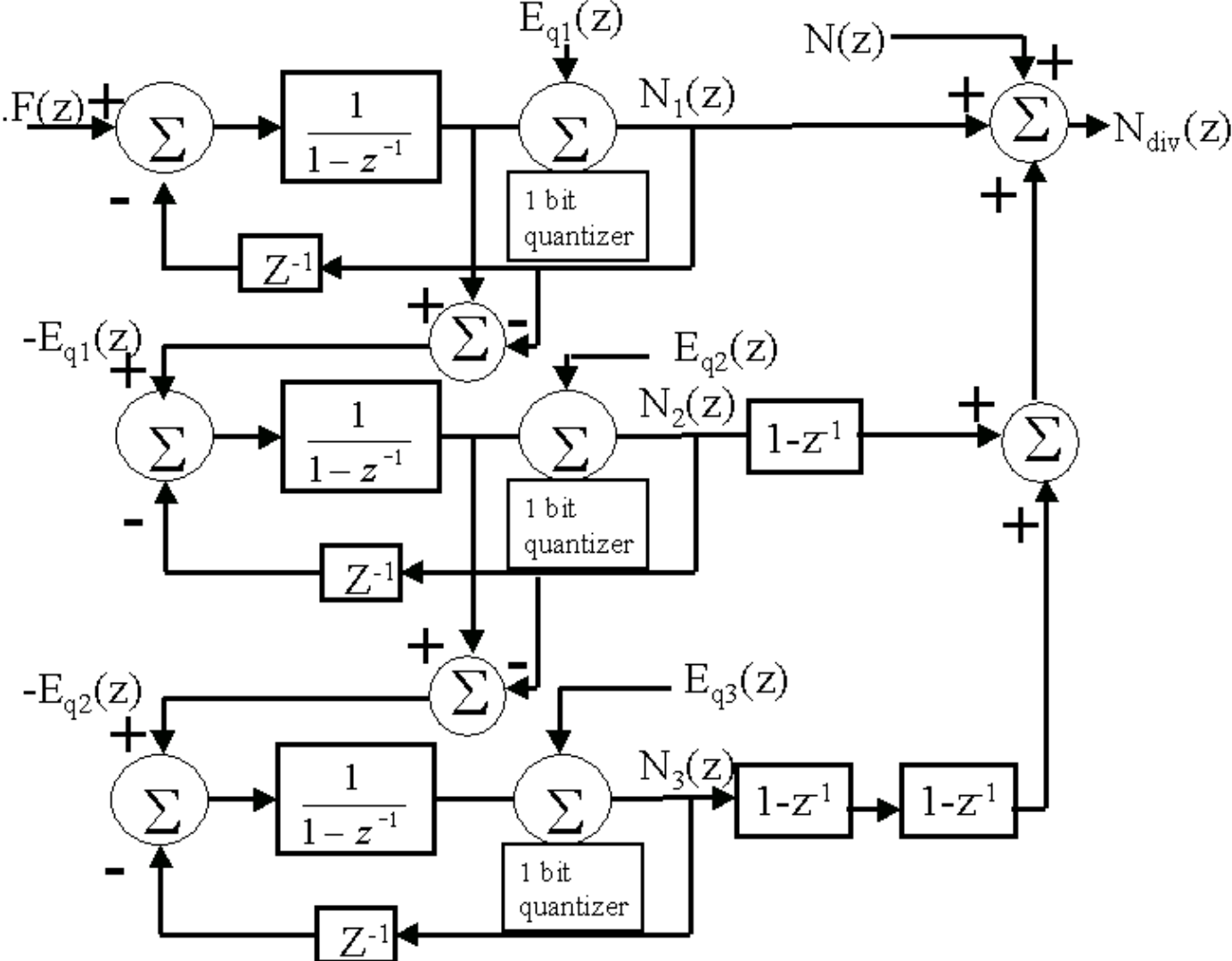
When accumulator core overflows, 1-bit quantizer outputs a 1.

Sigma-Delta Modulator Z-Domain Equation

$$Y(z) = .F(z) + (1 - z^{-1})Eq(z)$$

The quantization noise, $Eq(z)$, is high-pass filtered, (let $z = e^{j\omega}$ then $1 - z^{-1} = 1 - e^{-j\omega} \approx j\omega$ for ω small) if $.F(z)$ is sufficiently random. But the fraction is constant, so the quantization noise varies periodically, generating spurs.

Using a 3-Stage Sigma Delta Modulator



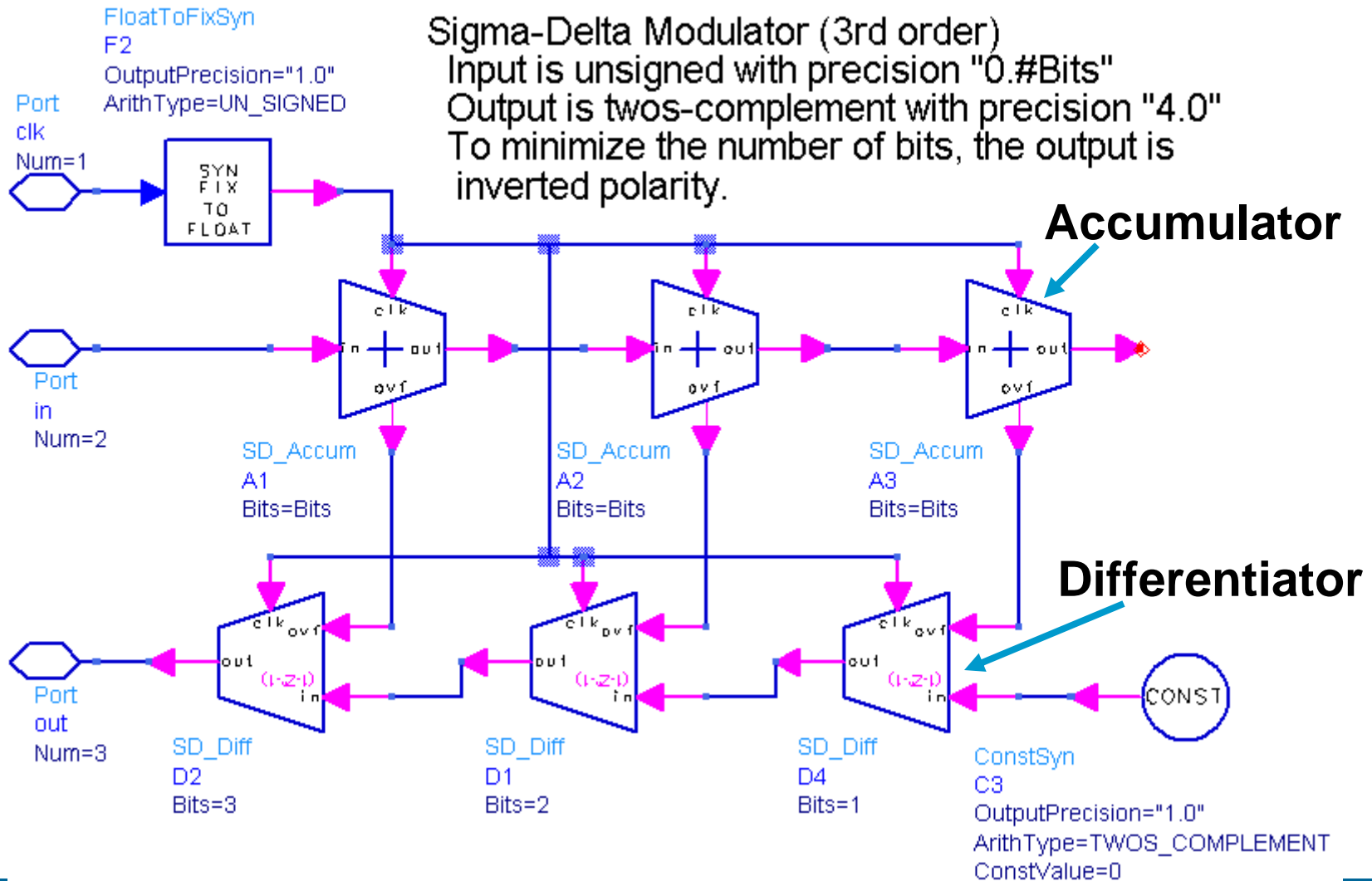
3-Stage Sigma-Delta Modulator Equation

Z-domain equation for frequency:

$$F_{out}(z) = N.F(z)F_{ref} + (1 - z^{-1})^3 F_{ref} E_{q3}(z)$$

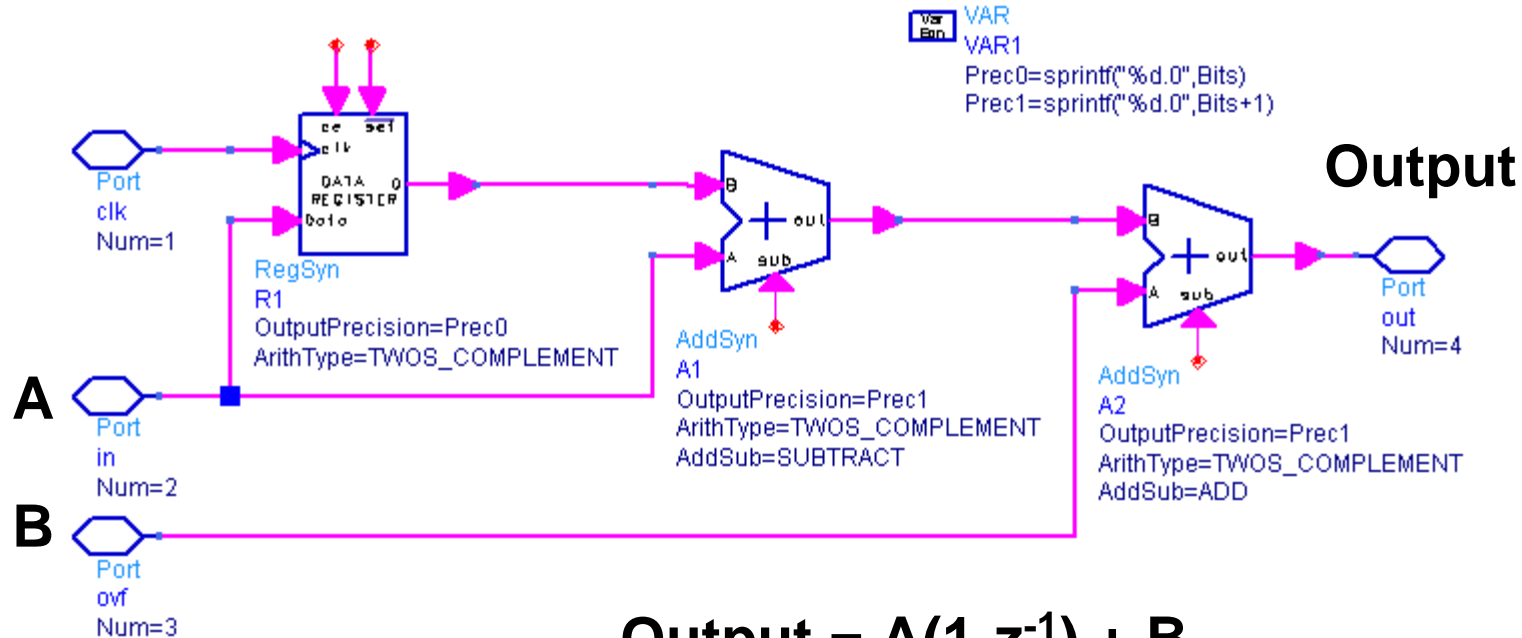
**3rd-stage quantization noise is more random than 1st,
and this noise has a more high-pass shape**

A Three-Stage Sigma-Delta Modulator



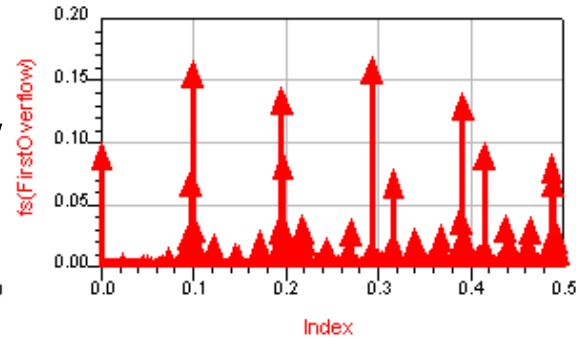
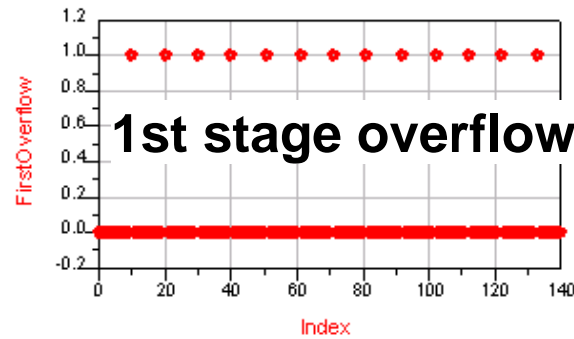
Differentiator in Ptolemy

A differentiator/summer block for the sigma delta modulator.
 ovf is a single input with "1.0" precision, that is treated as [0,-1] twos complement.
 Input is twos_complement with "Bits.0" precision.
 Output is twos_complement with "Bits+1.0" precision.

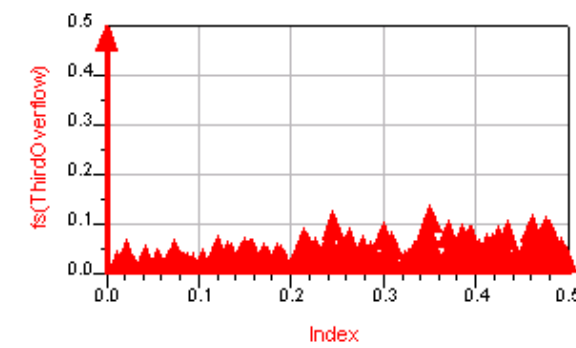
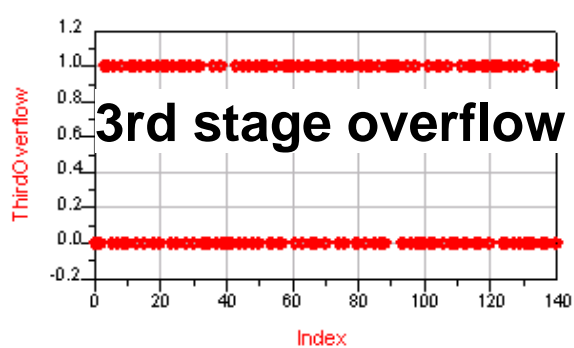
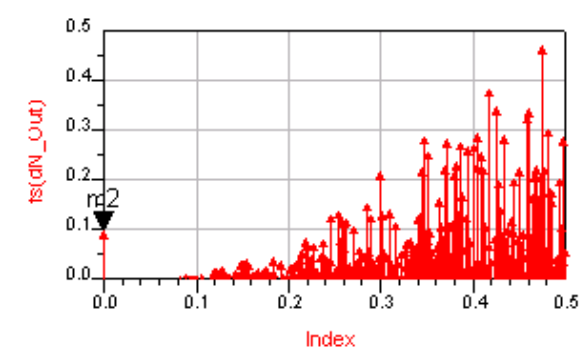
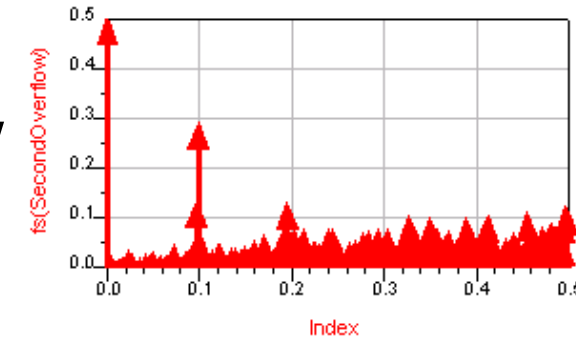
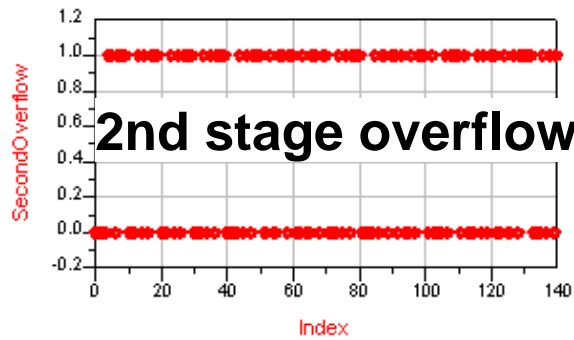
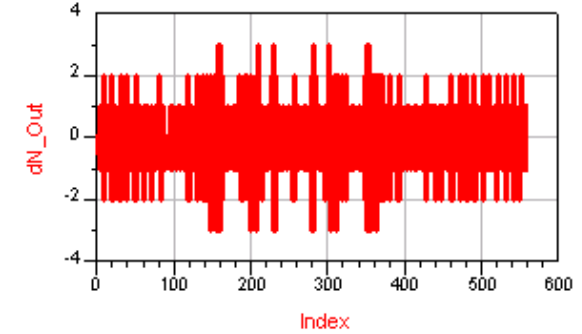


$$\text{Output} = A(1-z^{-1}) + B$$

3-Stage Sigma-Delta Modulator Signals



dN signal



```
m2
Index=0.0000000000
fs(dN_Out)=0.0982142857 / -180.0000000000
```

```
Fraction
0.0976562500 + j0.0000000000
```

```
mean(dN_Out)
-0.0962566845
```

Where are the examples that are referenced in this presentation?

Slide 5

Frequency response, phase margin, unity gain frequency:
examples\RF_Board\PLL_Examples\PLL_Freq_Resp_prj\PLL_Freq_Resp

Phase noise:

examples\RF_Board\PLL_Examples\PLL_PhaseNoise2_prj\PLL_Noise_Contrib or PLL_Noise_Contrib2 or

PLL_NoiseContrib3

examples\RF_Board\PLL_Examples\PLL_PhaseNoise1_prj\PLL_PhNoise

Slide 6

Various step responses, each from a loop with a different phase margin:

examples\RF_Board\PLL_Examples\DECT_LO_Synth_prj\PLL_Tran_SweptPhMargin.

“VCO spectrum” and “Frequency Error in Hz” are from a Knowledge Center example, “Simulation of PLL Using Sigma-Delta Modulator to Attain High Frequency Resolution.”

<http://edocs.soco.agilent.com/display/eesofkc/Simulation+of+PLL+Using+Sigma-Delta+Modulator+to+Attain+High+Frequency+Resolution>

Slides 9, 11, 12, 13, 14, 15

These are from the ADS project, PLL_ModelingSem_prj, which may be downloaded from:

<http://edocs.soco.agilent.com/display/eesofkc/PLL+component+behavioral+models>

Slide 16 and 17

Not in an example, but similar to examples\RF_Board\PLL_Examples\PLL_FracN_prj.

Slides 18 and 19

This is from Knowledge Center example “Adding phase noise from a text file to a reference osc. or VCO for time- or frequency-domain noise simulation” (ID #240058.) It is design RefOscPhNoiseTimeDom.

<http://edocs.soco.agilent.com/display/eesofkc/adding+phase+noise+from+text+file+reference+osc+or+vco+time+or+frequency+domain+noise+simulation>

Slides 20-24

These are from a Knowledge Center example (ID #301439.)

<http://edocs.soco.agilent.com/display/eesofkc/adding+phase+noise+behavioral+model+pll+simulations+time+domain>

Slides 25-30, 35-36, 41-43

These are from a Knowledge Center example (ID #216107.)

<http://edocs.soco.agilent.com/display/eesofkc/Simulation+of+PLL+Using+Sigma-Delta+Modulator+to+Attain+High+Frequency+Resolution>

Slides 31 and 32

These are from a Knowledge Center example (ID #301447.)

<http://edocs.soco.agilent.com/display/eesofkc/sigmadelta+modulator+pll+simulation+with+transistorlevel+pfd+charge+pump>

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