

Keysight Technologies

# Medalist i3070 Test Throughput Optimization

Application Note

This application note contains tips and tricks to effectively reduce test time, and consequently increase throughput on the Keysight *Medalist* i3070 In-Circuit Test system.

## Why does test time increase?

Firstly, know that longer test times can arise due to various reasons:

- The test generated from the Interactive Program Generator (IPG) may not be optimized for the specific production board revision
- Addition of test options when debugging tests the first time
- Addition of test options during production testing
- Incorrect interrupt analog test
- Incorrect power up
- Using default vector cycle to test digital devices
- Overly long wait during powered test
- Using "safeguard cool" command arbitrarily
- Overly complex test
- Immoderate wait in "testplan" file
- Incorrect GP-Relay usage
- Poorly maintained i3070 system hardware

## Optimizing test programs for the i3070 ICT system.

The i3070 ICT software offers various tools to help test engineers optimize their programs step-by-step.

### 1. Pins Test

The Pins Test verifies if there is good contact between the fixture and the printed circuit board currently being tested. Here is the syntax in the "testplan":

- The Pins Test is controlled by setting a flag in the "Set\_Custom\_Options" subroutine.
- Find the Chek\_Point\_Mode flag in Set\_Custom\_Options routine. It can be set to OFF, PRETEST or FAILURES. (e.g.: Chek\_Point\_Mode = Failures)
- OFF - Do not use Pins Test at all
- PRETEST - Run the Pins Test on every board, as the first test
- FAILURES - Run the Pins Test only after a failure has been detected.

#### Ideal setting for Pins Test usage

Only run Pins Test when a failure has been detected (Chek\_Point\_Mode = Failures).

This is the default mode.

### 2. Shorts Test

A very important setting to take note of in the Shorts Test is settling delay time. The default setting for settling delay is 50.00 us. This means there will be a 50-microsecond delay in between every node.

#### Ideal setting for Shorts Test

Set settling delay at 0 first, or remove all settling delays in debugging. Add in delay time only when actual conditions require.

#### Real-time example:

Using default settling delay, shorts test time was 5.563 seconds. After optimizing settling delay, shorts test time is reduced to 2.094 seconds.

For example:

```
report netlist, common devices
!!*****
threshold 15
!settling delay 50.00u
short "SMVREFCAP" to "SMVREFSOURCE"
short "UNNAMED_44_CAP_I136_A" to "FE0_RX-" !J4
short "UNNAMED_44_CAP_I136_A" to "FE0_RX+" !J4
short "UNNAMED_44_CAP_I135_A" to "FE0_TX-" !J4
short "UNNAMED_44_CAP_I135_A" to "FE0_TX+" !J4
short "V2P5_DCAP4" to "V_2P5"
!u27
short "H_GTLREF_MCH" to "H_GTLREF_MCH_A7" !u13
... ..
report phantoms
threshold 1000
!settling delay 6.165m
nodes "FAN_FB1"
!settling delay 55.00u
nodes "UNNAMED_56_CAP_I163_B"
nodes "PSU_TEMP"
... ..
settling delay 1m
nodes "UNNAMED_46_LTC4210_I46_SENSE"
nodes "UNNAMED_41_CAP_I65_B"
nodes "UNNAMED_39_CAP_I155_B"
nodes "UNNAMED_16_IC952601_I182_P33V"
nodes "UNNAMED_16_CAP_I161_A"
nodes "VCC3.3_CLK"
nodes "P3_3V"
nodes "V_1P25MEMVTT_B"
... ..
```

### 3. Quick Report

The Quick Report has the capability to evaluate a board directory, identify areas where test times can be reduced, and provide suggestions to strategically maximize throughput.

Quick Report can be generated via the PushButton Debug Macros or the BT-Basic window.

Under the board director, two files are generated, “throughput.summary” and “throughput.details”.

### 4. Analog Options

While some analog test options can increase test stability, these inadvertently increase test time. Examples of such analog test options are:

- Wait options: wa, dwa
- 6-wire tests: sa, sb, sl, en
- Line noise rejection: ed

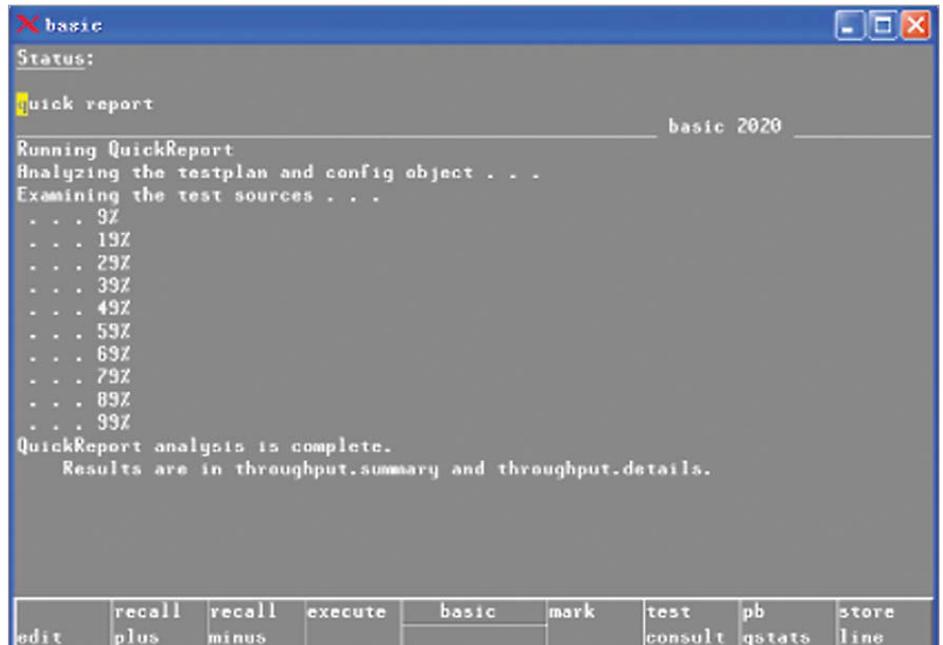
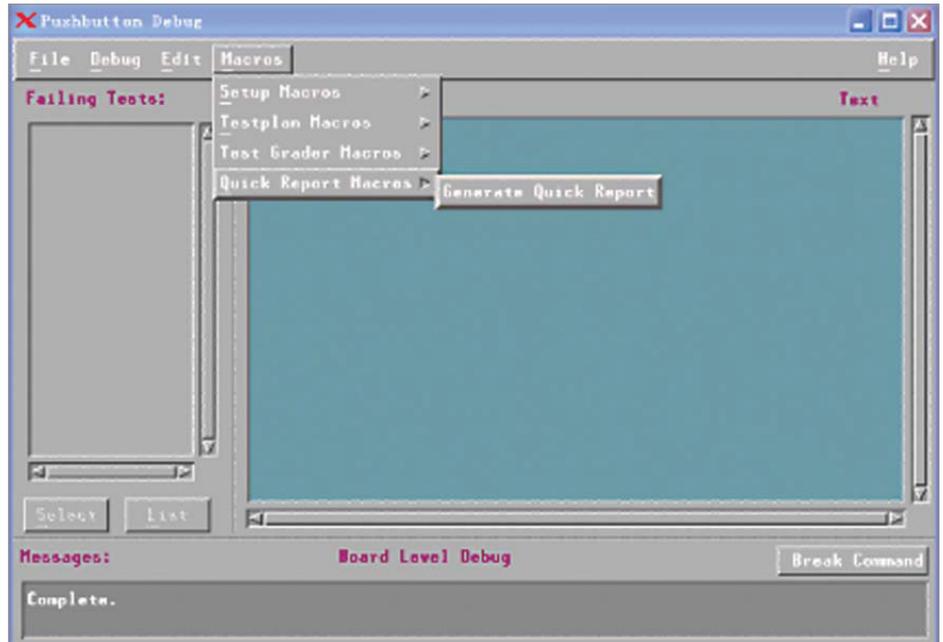
The following analog test options will not incur time penalty: am, ar, fr, of, ico, op, pf, pm, re, sm, wb.

#### Wait Options

**wa:** Wait option delays the test for the specified time (X seconds) to allow reactive components to stabilize. Do note that the “wa” option is a source wait!

- This wait is executed each time the voltage source is changed. After the signal is applied, a wait is enforced.
- A second wait is encountered when the voltage source is turned off. This allows reactive devices in the test circuit to discharge any power that might have been accumulated during the test. The total time added to the test is twice the time specified for “wa”.

**dwa:** Wait option delays the test for the specified time (X seconds) while the device stabilizes. It differs from the wait statement in that the delay is only applied before testing. Do note that the “dwa” option is a detector wait!



## 6-Wire Test

Here is an overview of the 6-wire tests:

- sa:** Senses the source voltage being applied to the component under test.
- sb:** Senses the detector voltage.
- sl:** Senses the guard point.
- en:** This enhancement option obtains multiple measurements on the device and the measurement circuit in the following manner:
  - i. The actual voltage output of the voltage source ( $V_S$ ) is measured.
  - ii. The voltage at the input of the Measuring Operational Amplifier (MOA VI) is measured.
  - iii. The voltage drop across the Reference Element is measured.
  - iv. Finally,  $V_{MOA}$  is measured.

A test line that uses the “en” option takes a longer time than the same test that does not use “en”.

## Line Noise Rejection

**ed:** Line Noise Rejection is used to integrate measurements over a line cycle. This results in a more stable measurement if the cause of instability is due to line noise.

The default measurement integration time is 500 us. If “ed”

## Reducing Redundant Test Options to Save Test Time

The best method is to remove extra test options, and use more guarding to ensure stability during analog tests.

For example, if other remote sensing or scanner sensing is present, you can turn the extra test options off.

If the “fr128” option has been set, change it to “fr1024”, and remove the “ed” option.

If the “en” option has been set, remove it.

If the “wa” or “dwa” option has been set, reduce the wait time, or remove it.

## AutoOptimizer

The i3070 software revision 07.00 and above comes with AutoOptimizer - a new tool for analog test optimization. Do note, however, that AutoOptimizer usage can only be enabled with a Control XTP card.

Table 1. Illustration of how extra test options result in significant increase in test times.

DC source voltage	Total test time	AC source voltage	Total test time
1 test @ 500 us/test	500 $\mu$ s	2 tests @ 500 us/test	1.0 ms
8 tests @ 500 us/test = 4ms		12 tests @ 500 us/test = 6ms	
Adding only “en”, and no other options. Measuring VS, VI, VRE and VMOA with specified source applied and with source set at 0 volts.	4 ms	Measuring VS, VI, VRE and VMOA for the imaginary signals (+90 and -90) and for the Real signal.)	6 ms
Integration time for adding “ed” (with no other options).	20 ms	Integration time for adding “ed” (with no other options).	20 ms
Adding en test: 8 en tests @20 ms	160 ms	Adding en test: 12 en tests @20 ms	240 ms
Adding ed, en: Waiting time to apply signal = 10 ms 8 en tests @20 ms each = 160 ms Waiting time for signal removal = 10 ms	180 ms	Adding ed, en: Waiting time to apply signal = 10 ms 12 en tests @20 ms each = 240 ms Waiting time for signal removal = 10 ms	260 ms

## 5. Power Up Sequence

- Use the “optimize” option for parallel power up, if DUT board is independent of the power sequence. This is the default setting for the Interactive Program Generator (IPG) to generate the testplan.
- Avoid “wait” option or reduce “wait” time.

## 6. Digital Test Optimization

Digital tests are based on vector time, hence any reduction of the “vector cycle” can save digital test time.

Occasionally, the “vector cycle” and “receive delay” times are not defined in digital tests. In such cases, the i3070 system will use the default vector time, 500 ns. The i3070 has three testhead options as shown in Table 2.

Table 2. i3070 testhead options.

i3070 Testhead Options	Testhead Speed	Range
Standard system	6 MHz	160 nanoseconds to 1.59 ms
Advanced system	12 MHz	80 nanoseconds to 1.59 ms
High accuracy system	20 MHz	50 nanoseconds to 1.59 ms

Typically, Boundary Scan and Silicon Nails testing take up significant test time, and this is where reducing the “vector cycle” would help.

For instance, a 6 MHz Standard i3070 system running a Boundary Scan test with 80,000 vectors records a test time of 40.0 milliseconds when the default vector cycle setting (500 ns) is used. By reducing the “vector cycle” to 160 ns, the test time on the 6 MHz i3070 system is significantly slashed to 12.8 milliseconds.

### Faster On-Board Programming

For existing test programs, use keyword “flash isp” instead of “flash” or use “flash” instead of “sequential” for faster test throughput. In addition, enabling “flash70” can accelerate the test by taking advantage of the new algorithms such as FF stripping and segment removal features.

### Mixed Test

Reduce the number of “continue analog” and “continue digital” statements.

### Using “Safeguard Cool”

The “Safeguard Cool” feature applies a cool down delay between tests. Digital tests are inhibited during this period for safety reasons, but the cool-down delays are enforced. Essentially, any Safeguard Inhibits command is ignored.

DO NOT use “Safeguard Cool” for every digital test! A good tool to check which digital IC requires a “Safeguard Cool” is the “compile “digital/IC\_Name”; list”.

```

S A F E G U A R D   S U M M A R Y
-----
Safeguard status:      Not inhibited
Estimated test time:   2.70e-05
Safe test time (device): 5.99e-01 (1ZU5)

```

Figure 1: This screenshot shows an example of a digital IC that does not require “Safeguard Cool”

```

S A F E G U A R D   S U M M A R Y
-----
Safeguard inhibit:     Test too long for upstream device(s)
                       1ZU107
Estimated test time:   1.57e-02
Safe test time (device): 5.62e-03 (1ZU107)

```

Figure 2: This screenshot shows an example of a digital IC test that has been inhibited by Safeguard, because the test time is too long. In such a case, “Safeguard Cool” can be used to proceed with the test.

```

S A F E G U A R D   S U M M A R Y
-----
Safeguard inhibit:     Non-digital device(s) upstream
                       1ZQ1ZCR1
Estimated test time:   3.99e-04
Safe test time (device): 5.99e-01 (1ZU8)

```

Figure 3: This screenshot shows an example of a digital IC test inhibited by Safeguard, because the upstream device is not a digital device. If the analog device is ignored, the “Safeguard Digital” test option can be used.

**CAUTION:** Precaution is needed if a transistor is driving the digital input and the safeguard level has been set to digital. Will the digital driver damage the transistor? Probably not, but you may want to adjust your driver levels to limit the amount of current the transistor has to source or sink.

### Reducing Extra Wait Time

Do not add superfluous “wait” in digital test. Check all the “wait” options in every digital test and either reduce or delete it accordingly.

### Overly Complex Libraries

Sometimes, digital libraries can become too complex. The test engineer can reduce some unused tests or re-generate a new library during debug.

## 7. Testplan Optimization

- Do not interrupt analog tests. The test controller will download all objective files into the RAM. If the test is interrupted, the test controller will re-download the objective files from the point of interruption. Instructions such as “unpowered”, “powered” and “if...then...” can interrupt the analog test.
- Reduce or delete “wait” time in the testplan.
- Reduce “GP-Relay” usage and do not use the same “GP-Relay” repeatedly!
- Do not add “Safeguard Cool” at the beginning of the subroutine. The i3070 system default setting is “Safeguard All” for every subroutine. So, realign the digital test sequence for the safeguard settings. For example:

```
sub Digital_Tests (Status_
Code, Message$)
global Status
if Message$ <> "" then
print tab(5);Message$
Status = Status_Code
test "digital/u14"
test "digital/u46"
test "digital/u47"
... ..
safeguard digital
test "digital/u101"
test "digital/u110"
... ..
safeguard cool
test "digital/u53"
subend
```

## Upgrade Legacy 3070 Hardware and Purchase the Latest Software License for Faster Speeds

Your legacy 3070 system hardware can lead to a significant increase in your test time due to the more complex boards it has to test today!

Keysight’s latest PC controller provides a more stable and faster running time. Here are some highlights of what the latest Keysight *Medalist* i3070 suite can offer you:

- ASRU N Revision and Control XTPA provide one of the fastest tests in the industry.
- 12 MHz or 20 MHz Hybrid Double Density Cards provide unparalleled speed and coverage
- Additional features available with latest i3070 software revisions 9.x and above.
- Panel test license.
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