This is the first in a series of application notes that addresses power optimization, characterization, and simulation challenges in embedded designs.
**Introduction**

If you are designing embedded systems, you face various power optimization and power characterization hurdles throughout the design process. You know what you want to output, simulate and measure—but you need a whole “toolbox” of instruments and hardware to do the job. Properly configuring the various tools into an accurate, dependable solution can be difficult and time consuming. When you need to rerun a test later, you may have to repeat the whole time-intensive process of configuring your test setup.

The challenges you face can be divided into three categories: properly powering on and off multiple power inputs, characterizing power needs under dynamic load conditions and simulating real-world power conditions. This application note will focus on properly powering on and off multiple power inputs in an embedded design. We will discuss a simple way to overcome power sequencing challenges without the need for a costly toolbox of hardware.

**Properly Powering On and Off Multiple Power Inputs**

Embedded systems can be made up of any combination of microcontrollers, FPGAs, ASICs and memory chips. These individual integrated circuits often have multiple power input requirements that must be properly sequenced on and off to prevent latch-up. Precise slew rates on each input at power on or power off may be required as well.

Latch-up may cause a wasteful initial surge of current at turn on, or it may be severe enough to inflict permanent damage to the semiconductor device. Even without the fear of latch-up, powering on your design can become complicated if the embedded system consists of multiple integrated circuits where some become active instantly and others require some time to configure or execute a start-up routine that must be retrieved from a memory device. In this situation, there may be power optimization advantages to establishing precise sequencing across the integrated circuits.

Existing solutions for providing multiple power inputs, sequencing and slew rates include fixed regulator circuits and programmable power supplies. In the initial design stage, you often will be able to leverage fixed regulator circuits from development boards or past designs. If you implement fixed regulators early in the design, you do not have the ability to adjust input sequencing timing and slew rates for minimum current draw at turn-on. Also, with fixed regulators you still need some type of measurement device to perform precise power measurements for optimization and troubleshooting during the design process.

Using programmable power supplies provides the flexibility to adjust input power settings during the design process for power optimization. Sequencing power supplies on and off with software requires extra time for programming, and it also injects a timing-error deviation. The problem with the software-only approach is your sequence delay accuracies are dependent on a computer operating system that shares processor time with multiple applications, so accuracy can vary by more than 10 ms. You could employ a real-time operating system, but this is a costly measure that still has limitations in timing accuracy. The other option is to employ hardware-timed switching. This comes with a high time overhead and extra cost, since you need to either create custom hardware or configure a DIO card to accurately time switch closures. These sequencing configurations often need to be reconfigured each time the design changes or a new design is started.

Setting up various slow rates on power inputs when you are using fixed regulator circuits requires some type of RC network at the output. Once again, this is an inflexible solution since it cannot be easily adjusted. Controlling slew rate on programmable power supplies may be possible through programming if you are working with a high-performance supply. Otherwise, you will need to use some type of RC network on the output of the supplies.

**Product Features**

**Solution**

The power input challenges embedded design engineers face can be solved with the Keysight Technologies, Inc. N6705A DC Power Analyzer. The N6705A provides four programmable power supply outputs each with dynamic measurement capability. Each of the four output’s characteristics is determined by which plug-in power module is used for that output. There are 21 different power modules available for the N6705A. Table 1 on page 7 shows a list of suggested modules for the N6705A and their key specifications that make them a good fit for embedded design development.

The N6705A’s power outputs have built-in sequencing capabilities. Sequencing time delays can range between 0 and 1 s in 1-ms steps or 0 and 1000 s in 1-s steps. The sequence timing is all done in the hardware of the instrument, which guarantees a high level of accuracy and repeatability. Precision slew rate control on each channel, as fast as 20 μs per volt, allows you to set voltage ramp up times on a per-channel basis. Other N6705A features that are applicable to embedded design:

- Oscilloscope-like display that can show voltage, current and power versus time on multiple channels. This feature allows you to view in real time the voltage, current and power events of your designs.

- Built-in data logger that continuously logs time-stamped data to a large color display and to a file. You can log data on all four outputs at the same time. Data log files can be saved to internal memory or to an external USB memory drive.

- Built-in waveform functions and arbitrary waveform capability. You can define an arbitrary waveform with up to 64k points.

- High-accuracy voltage and current measurement capability. Accurate current measurement capability down to the microampere level.

The following provides a detailed example of using the N6705A to properly power on an embedded design to lower the turn-on power draw of the design.
Example: Properly Powering On an Embedded Design

The embedded design for this example uses an FPGA, flash memory chip and various peripheral devices. The FPGA has three power inputs (VCCINT, VCCAUX, and VCCO), two of which have sequencing requirements (VCCINT and VCCAUX). The fourth power input on the embedded design powers the flash memory and peripheral devices (VPER). The memory chip needs to be fully powered up before the FPGA, because the FPGA uses the flash memory for configuration, so VPER is the first to be sequenced on. The whole setup is shown in Figure 1.
The particular FPGA that is being used in this example does not have strict sequencing requirements, meaning if sequencing is not used the FPGA will not be damaged. However, if the $V_{\text{Core}}$ is turned on before or at the same time as $V_{\text{CCAUX}}$, the FPGA will draw a surplus core current at turn on. The surplus current draw will wear down battery power faster and could force the power distribution designer to use a higher-current-handling power-hungry regulator.}

Figure 2 shows the sequencing, or Output On/Off Delay, setup screen of the N6705A. Notice $V_{\text{Core}}$ is sequenced to turn on 1 ms before $V_{\text{CCAUX}}$ on the N6705A. As a result, we can see on the N6705A's scope display an undesirable surplus current spike occurs at the core supply ($V_{\text{Core}}$) during turn-on because it was powered on before $V_{\text{CCAUX}}$.

Figure 3 shows the proper sequencing to avoid the surplus current spike of ICCINT at turn-on (left) and the output core current (right).

Figure 3 shows the proper sequencing to avoid the surplus current spike of ICCINT at turn-on (left) and the output core current (right).
To achieve the ramp rate requirements for \( V_{\text{CCINT}} \) and \( V_{\text{CCO}} \) (see Figure 1), the slew rates for channels 1 and 2 were adjusted. Figure 4 shows the N6705A display for changing a channel’s slew rate, which is expressed in volts per second (V/s). Below the slew rate settings screen is the rising slew rate of channel 1 and 2 on the N6705A outputs. The rise time is captured using the markers for the display.

**Figure 4. Core voltage and I/O voltage slew rate settings**
To ensure successful power-on, the FPGA power supplies must rise through their respective threshold-voltage ranges with no dips. Figure 5 displays each output from the N6705A with proper sequencing and ramp rates at turn-on time. Each output presents a smooth rise of voltage that is free of dips and other erratic behavior. Figure 5 also lists the power modules used for the example FPGA circuit tests. Since the example circuit uses low power (less than 2 A), any module from the N675xA Series or N676xA Series is a good fit for this demonstration. Up/down output speed, measurement accuracy, and output power capabilities are the main features you need to consider when choosing the proper N6705A power modules for your specific embedded system design needs. Refer to Table 1 on page 7 for information regarding recommended power modules and their specifications.

Figure 5. Power module voltages at turn-on

Sequencing Power Inputs of More Than Four Supplies

If the embedded design requires more than four separate power supply inputs, you can sequence multiple N6705A mainframes together. You can easily do this with the user-configurable digital I/O ports located on the back of the mainframe. The latency involved when communicating between multiple mainframes is trivial compared to the rise time of the power modules and the 1-ms sequencing step size. No programming or code writing is needed to take advantage of this feature.

Conclusion

N6705A DC Power Analyzer is an all-in-one toolbox for quickly and easily addressing power optimization, characterization and simulation challenges in embedded designs. Powering on and off embedded designs presents a challenge because integrated circuits such as FPGAs, microcontrollers, and ASICs often have power input sequencing and slew rate requirements. If these turn-on requirements are not met, it could cause damage to the embedded design (latch-up) or cause an unnecessary excessive power draw at turn-on.

The N6705A provides built-in adjustable sequencing and slew rate capability across its four outputs and across mainframes. You can access these built-in capabilities easily through the front panel to protect your design from damage and gain the flexibility to fine tune the turn on and off process for power optimization throughout the design process. The optimized power input timing data that is obtained from the N6705A can be employed when the power distribution portion of the design is done to ensure minimum power draw at turn on and off.
Table 1:
Key specifications of N6705A modules ideally suited for embedded design.

<table>
<thead>
<tr>
<th>DC output ratings</th>
<th>Voltage</th>
<th>N6751A/52A</th>
<th>N6754A</th>
<th>N6761A/62A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage</td>
<td>50 V</td>
<td>60 V</td>
<td>50 V</td>
<td></td>
</tr>
<tr>
<td>Current</td>
<td>5 A / 10 A</td>
<td>20 A</td>
<td>1.5 A / 3 A</td>
<td></td>
</tr>
<tr>
<td>Power</td>
<td>50 W / 100 W</td>
<td>300 W</td>
<td>50 W / 100 W</td>
<td></td>
</tr>
<tr>
<td>Max up-programming time with full R load</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Time from 10% to 90% of total voltage)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage change</td>
<td>0 to 10 V</td>
<td>0 to 15 V</td>
<td>0 to 10 V</td>
<td></td>
</tr>
<tr>
<td>Time</td>
<td>0.2 ms</td>
<td>0.35 ms</td>
<td>0.6 ms</td>
<td></td>
</tr>
<tr>
<td>Voltage change</td>
<td>0 to 50 V</td>
<td>0 to 60 V</td>
<td>0 to 50 V</td>
<td></td>
</tr>
<tr>
<td>Time</td>
<td>1.5 ms</td>
<td>2.0 ms</td>
<td>2.2 ms</td>
<td></td>
</tr>
<tr>
<td>Voltmeter/ammeter measurement accuracy</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(at 23°C ± 5°C) voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage high range</td>
<td>0.05% + 20 mV</td>
<td>0.05% + 25 mV</td>
<td>0.016% + 6 mV</td>
<td></td>
</tr>
<tr>
<td>Voltage low range (5.5 V)</td>
<td>N/A</td>
<td>N/A</td>
<td>0.016% + 1.5 mV</td>
<td></td>
</tr>
<tr>
<td>Current high range</td>
<td>0.1% + 4 mA</td>
<td>0.10% + 8 mA</td>
<td>0.04% + 160 µA</td>
<td></td>
</tr>
<tr>
<td>Current low range</td>
<td>N/A</td>
<td>N/A</td>
<td>0.03% + 15 µA</td>
<td></td>
</tr>
<tr>
<td>(at 100 mA, at 0 - 7 V)</td>
<td>N/A</td>
<td>N/A</td>
<td>0.03% + 55 µA</td>
<td></td>
</tr>
<tr>
<td>(≤200 µA)</td>
<td>N/A</td>
<td>N/A</td>
<td>0.5% + 100 NA (Option 2UA)</td>
<td></td>
</tr>
</tbody>
</table>

Related Keysight Literature

<table>
<thead>
<tr>
<th>Publication title</th>
<th>Publication type</th>
<th>Pub number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Keysight N6705A DC Power Analyzer</td>
<td>Data sheet</td>
<td>5989-6319EN</td>
</tr>
<tr>
<td>Powering DC-to-DC Converters Using the</td>
<td>Application note</td>
<td>5989-6452EN</td>
</tr>
<tr>
<td>Keysight N6705A DC Power Analyzer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Biasing Multiple Input Voltage Devices</td>
<td>Application note</td>
<td>5989-6454EN</td>
</tr>
<tr>
<td>in R&amp;D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FPGA Circuit Design: Overcoming Power-</td>
<td>Application note</td>
<td>5989-7744EN</td>
</tr>
<tr>
<td>Related Challenges</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Simulating Power Interruptions for DC</td>
<td>Application note</td>
<td>5989-6455EN</td>
</tr>
<tr>
<td>Input Devices</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
myKeysight
www.keysight.com/find/mykeysight
A personalized view into the information most relevant to you.

Three-Year Warranty
www.keysight.com/find/ThreeYearWarranty
Keysight’s commitment to superior product quality and lower total cost of ownership. The only test and measurement company with three-year warranty standard on all instruments, worldwide.

Keysight Assurance Plans
www.keysight.com/find/AssurancePlans
Up to five years of protection and no budgetary surprises to ensure your instruments are operating to specification so you can rely on accurate measurements.

For more information on Keysight Technologies’ products, applications or services, please contact your local Keysight office. The complete list is available at: www.keysight.com/find/contactus

Americas
Canada (877) 894 4414
Brazil 55 11 3351 7010
Mexico 001 800 254 2440
United States (800) 829 4444

Asia Pacific
Australia 1 800 629 485
China 800 810 0189
Hong Kong 800 938 693
India 1 800 112 929
Japan 0120 (421) 345
Korea 080 769 0800
Malaysia 1 800 888 848
Singapore 1 800 375 8100
Taiwan 0800 047 866
Other AP Countries (65) 6375 8100

Europe & Middle East
Austria 0800 001122
Belgium 0800 58580
Finland 0800 523252
France 0805 980333
Germany 0800 6270999
Ireland 1800 832700
Israel 1 809 343051
Italy 800 599100
Luxembourg +32 800 58580
Netherlands 0800 0233200
Russia 8800 5009286
Spain 0800 000154
Sweden 0200 882255
Switzerland 0800 805353
Opt. 1 (DE)
Opt. 2 (FR)
Opt. 3 (IT)
United Kingdom 0800 0280637

For other unlisted countries:
www.keysight.com/find/contactus

(BP-07-10-14)