Keysight Technologies
De-emphasized Signal Generation with the Keysight 81250A ParBERT

Application Note
Overview

De-emphasis and equalization are commonly used techniques when transmitting electrical and optical signals at gigabit data rates. The term de-emphasis is used to describe signal conditioning on the transmitter, while the term equalization is used on the receiver side.

De-emphasis and equalization compensate for signal integrity issues caused by the loss in the channel on printed circuit boards, backplanes, and fiber optic links. The most popular high-speed electrical standards require transmitter de-emphasis. These standards are: PCI Express®, SATA 3 Gb/s, fully buffered DIMM, CEI, and 10-Gb Ethernet.

Figure 1 shows the principle waveform of a de-emphasized signal (two-tap). Sometimes this is called pre-emphasis, as one could see a boost of amplitude for the first cycle after a transition occurs. However, usually the signal's amplitude is reduced after a delay of 1 unit interval (UI) when the data content does not change. From this point of view the method is called de-emphasis.

This document explains how a de-emphasis can be achieved when using the Keysight Technologies, Inc. 81250A ParBERT and covers the following topics:

- The problem with inter-symbol interference (ISI)
- Channel description, frequency domain
- The definition of a de-emphasis frequency domain
- Standards using a de-emphasis
- Implementing a de-emphasis with ParBERT channels
- How to configure the setup for IEEE 802.3ap (10 GBASE-KR) and IEEE 802.3aq (10 GBASE-LRM).

Note: As a prestudy, the De-emphasis Application Note and the Keysight N4916 De-Emphasis Signal Converter Signal Generation Data Sheet are recommended.
The Problem with ISI

Signal integrity issues on printed circuits, motherboards, and connectors arise from loss and reflections in the transmission channel that decreases signal performance. Loss causes eye closure or inter-symbol interference (ISI)-type of jitter.

Figures 3 to 5 show the eye closure/ISI from a data signal running through a 12-inch motherboard, while starting with a data rate of 2 Gb/s the data rate is doubled with each iteration. The eye closure/ISI reading is summarized in Table 1. The finding is that the eye closure/ISI jitter does not increase linearly with data rate. Instead, it increases with a higher magnitude than the data rate increases. This behavior results from the frequency-dependent loss of the trace on the motherboard. This is explained in the Channel Description section.

<table>
<thead>
<tr>
<th>Data rate</th>
<th>2 Gb/s</th>
<th>4 Gb/s</th>
<th>8 Gb/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eye closure</td>
<td>44 mUI</td>
<td>122 mUI</td>
<td>431 mUI</td>
</tr>
</tbody>
</table>

Figure 3. Signal from a PC board trace at 2 Gb/s
Figure 4. Signal from a PC board trace at 4 Gb/s
Figure 5. Signal from a PC board trace at 8 Gb/s
Channel Description

Frequency domain

One method to describe the channel characteristics is with the help of the scattering (S) parameters. S-parameters describe the insertion and transmission behavior as a function of frequency. S21 describes the transmission behavior; it is a complex figure with real (magnitude) and imaginary (phase) parts. Figure 6 is the example of the magnitude of S21 (|S21|) of the motherboard used for Figures 3 to 5. It is important to understand that Figure 6 displays the magnitude only, which can be expressed as the loss. This loss typically has three root causes:

- Di-electric conductivity
- Skin effect (resistance in the surface of the conducting material)
- Radiation

Figure 6 shows that the loss curve is not linear. The loss increases with a higher magnitude. The curve also shows some sharp dips. These dips are caused by two (or more) impedance mismatch points. Between such impedance mismatch points the PC board trace acts like a resonator for a certain frequency. At this frequency we obtain a standing wave within this resonator and this causes radiation, similar to that from an antenna. This specific radiation lowers the curve in the dips by another 10 to 20 dB.

The ISI cannot be explained by the |S21| alone. The S21 is a complex figure and can be represented with magnitude and phase relation. The phase relation is depicted in Figure 7. The S21 of an ideal device will show a straight line. The red curve shows the phase to rotate between −180 degrees to +180 degrees for frequencies above 7.5 GHz. This means the frequency content above 7.5 GHz may be earlier or later than the frequency constant at lower frequencies. This kind of representation is limited to ±180 degrees. It cannot be seen if there are frequency components earlier/later than ½ UI.
Channel Description (continued)

Time domain

Another way to describe ISI is with the help of the impulse/step response in the time domain. We send a single pulse into a PC board trace and record the output signal. Figures 8 and 9 depict the corresponding input and output signal with the same amplitude and timing scale for comparison. The pulse received from the PC board trace has changed in:

- Amplitude
- Edge speed
- Width
- Settling time

![Figure 8. Input signal to the PC board](image1)

The issues with the amplitude reduction and the settling time spreading out over multiple UIs are the reasons for the name ISI. The levels and the position of a pulse depend on the history. The settling explains why multiple consecutive bits are affected.

![Figure 9. Output signal from the PC board, the received pulse is attenuated and changed in 1 UI](image2)

The root cause of the distortion comes from the frequency-dependent loss and phase relation as discussed in the Frequency Domain section. The frequency-dependent phase can especially cause different distribution times for each of the frequencies involved, which is expressed as: the group delay is not constant.

![Figure 10. Output signal from the PC board, multiple bits from the PRBS pattern over time](image3)

In conclusion, we can say ISI is caused by pulse dispersion, or in the case of dispersion we will obtain ISI. The model of the pulse dispersion helps to understand the digital method of compensating for the ISI, which is explained further in this document.

![Figure 11. Output signal from the PC board, multiple bits from the PRBS pattern shown as an eye diagram](image4)

Such effect is well known for optical links. In that instance it is called dispersion. It makes sense to leverage the wording from the optical to the electrical domain.
Channel Description (continued)

How to compensate

Ideally the de-emphasis and the equalization invert the channel behavior. The first attempts to do so used analog high-pass filters for compensation, see Figure 10. As this degrades noise performance of a system, this was not widely accepted.

![Input signal](image1)

![Output signal](image2)

Figure 12. High pass filter to approximate channel inversion

Now the idea is to re-store the original shape by canceling out the energy before and after the cursor. Basically we pre-condition the signal by subtracting some energy before (pre-) and after (post-) the cursor. This is called pre- and post-cursor. As can be seen from Figure 9, the time of dispersion may spread over multiple UIs.

![Flip-flop chain approach](image3)

Figure 13. Flip-flop chain approach to approximate the inversion of the step response

Theoretically, we could think of dividing the time before and after the cursor in infinitesimal small windows and do the correction by adding/subtracting a small portion of energy. Practically, the granularity for the correction window is 1 UI, which can be derived from the underlying period in the data signal.

As a practical implementation, a chain of flip-flops clocked on UI basis is used, according to Figure 13. All flip-flop outputs are added together with variable gain. Consecutively we obtain a signal with advanced and delayed components, which add/subtract some adjustable energy to the original signal. As advanced signals are impossible to be generated, the implementation will use the main channel from the middle of the flip-flop chain.

As shown in Figure 9 the real world dispersion is asymmetrical, the dispersion is more in time and magnitude on the right side. This indicates the higher need for the delayed signal. Basically, a rule of thumb for setting up compensation is:

1. Add a delayed signal (+1 UI) to the original signal
2. Add a advanced signal (-1 UI)
3. Add a second delayed signal (+2 UI)
The Definition of a De-Emphasis

Figure 14 depicts a two-tap solution. One cursor is added to the main path; this cursor is delayed by 1 UI. This addition is a subtraction; the signal levels are lower after the 1 UI delay than after a transition.

The output parameters are defined by C(0) as the transitional amplitude and C(+1), which reduces C(0) to the de-emphasized amplitude. The relation of C(+1)/C(0) is defined by the parameter of the de-emphasis value either as the ratio shown in equation (1) or in dB as shown in Equation (2):

Equation 1
\[ R = \frac{V_{\text{pre}}}{V_{\text{de}}} \]

Equation 2
\[ R = 20 \cdot \log \left( \frac{V_{\text{pre}}}{V_{\text{de}}} \right) \]

In reality the signal gets subtracted after a 1 UI delay. This results in a waveform shown in Figure 15.

Figure 15. Definition of the amplitude parameters of a two-tap de-emphasis

Figure 16 depicts a three-tap solution. There is a cursor before and after the main transition. In reference to the two-tap solution. The third tap is the precursor.

Figure 16. Block diagram of a three-tap de-emphasis

The output parameters are defined by C(0) as the transitional amplitude, C(+1) and C(–1). The definition for the de-emphasis values are:

Equation 3
\[ R_{\text{pre}} = - \frac{V_{\text{pre}}}{V_{\text{ss}}} \]

Equation 4
\[ R_{\text{pst}} = - \frac{V_{\text{pst}}}{V_{\text{ss}}} \]

It should be noted that the valid ranges of C(1) and C(–1) coefficients may have positive or negative values. Figure 17 shows the definition of the amplitude parameters of a three-tap de-emphasis.

Figure 17. Definition of the amplitude parameters of a three-tap de-emphasis
Standards Using a De-Emphasis

PCI Express

The PCI Express standard defines the de-emphasis by:

Subsequent bits are driven at a differential voltage level (~3.5 ±0.5 dB at 2.5 GT/s and either ~3.5 ±0.5 dB or –6 ±0.5 dB at 5.0 GT/s) below the first bit. At 5.0 GT/s de-emphasis is selectable via configuration register bits. The two de-emphasis values defined for 5.0 GT/s operation permit optimum equalization for both short, reflection dominated channels, and long, loss dominated ones.

Note that individual bits, and the first bit from a sequence in which all bits have the same polarity, must always be driven between the minimum and maximum values as specified by VTX-DIFF-PP... The de-emphasis level is defined via CSR bits...

Figure 18 shows the de-emphasized signal as defined by PCI Express Rev 2.

![Figure 18. The de-emphasized signal as defined by PCI Express Rev 2](image)
LRM (Long reach multi-mode, IEEE 802.3aq)

The characteristics of the stressed test signal are defined in Chapter 68.6.9.2 of the IEEE 802.3aq standard and are based upon the parameters in Table 2. These parameters and the definition in Chapter 68.6.9.2 of the standard describe an ISI generator as a tapped delay line with four weighted taps having equally spaced delays. The resulting de-emphasis is illustrated in Figure 20. In addition to this impulse shaping, the standard requires the addition of Gaussian white noise as stress.

Table 2: Coefficients for the three defined channel characteristics of LRM

<table>
<thead>
<tr>
<th>Tap spacing, $\Delta t$, of ISI generator</th>
<th>$-$ 0.75 UI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre-cursor tap weights $(A_1, A_2, A_3, A_4)$</td>
<td>$(0.158, 0.176, 0.499, 0.167)$</td>
</tr>
<tr>
<td>Symmetrical tap weights $(A_1, A_2, A_3, A_4)$</td>
<td>$(0.00, 0.513, 0.00, 0.487)$</td>
</tr>
<tr>
<td>Post-cursor tap weights $(A_1, A_2, A_3, A_4)$</td>
<td>$(0.254, 0.453, 0.155, 0.138)$</td>
</tr>
</tbody>
</table>

Specific to this standard is the spacing of the cursors. In contrast to the prior examples shown in this document, here the spacing is less than 1 UI. The spacing required is 75 ps instead of 1 UI of 97 ps (10.3125 Gb/s) as illustrated in Figure 21.

The standard defines a comprehensive stressed receiver test procedure:

...the three ISI impairments...together with the appropriate OMA values...define six discrete signal conditions...select the required ISI...set the attenuator and Gaussian white noise source to obtain...the stressed sensitivity in OMA...Connect the test signal to the system receiver TP3 and a BER of better than $10^{-12}$ shall be achieved for each case

Refer to How to configure the Isetup for IEEE 802.3ap and IEEE 802.3aq to setup the PaRBERT 81250A for these requirements.
Implementing a De-Emphasis Using ParBERT Channels

Creating a three-tap de-emphasis with three generator channels

An 81250A ParBERT™, with three N4872A generators are used for the following experiment. The generator outputs are combined with help of two, 3-way 11636B power dividers as shown in Figure 22. The setup is asymmetrical for the three channels. A power divider comes with 6 dB attenuation (equals amplitude x.5) from input to output. Two channels run through two dividers, one channel through one only. So it is recommended to use the path with one divider only for the main channel and the channels responsible for pre- and post-cursor run through two dividers.

Figure 22. Two, 3-way divider combining the outputs of three modules

Timing wise, there is a propagation delay difference for the main channel which occurs ~250 ps earlier in the setup as shown. As a result, the setup needs a careful timing alignment. This is performed with the help of the deskew editor. The procedure is similar to that discussed in the next section of this document.

Figure 23. The three-tap signal at 10 Gb/s based on a repetitive 0000000011 11111111 pattern

Table 3. ParBERT programming for the three-tap signal

<table>
<thead>
<tr>
<th></th>
<th>Main</th>
<th>Post_1</th>
<th>Pre</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay</td>
<td>1 UI</td>
<td>2 UI</td>
<td>0 UI</td>
</tr>
<tr>
<td>Levels</td>
<td>±0.5 V</td>
<td>±0.3 V</td>
<td>±0.1 V</td>
</tr>
<tr>
<td>Polarity</td>
<td>Normal</td>
<td>Inverted</td>
<td>Inverted</td>
</tr>
</tbody>
</table>
Implementing a De-Emphasis Using ParBERT Channels (continued)

Creating a four-tap de-emphasis with four generator channels

Four generators are combined with help of one, 5-way power divider (Aeroflex/Weinschel 1594\(^{11}\). Refer to Figure 24. This setup is symmetrical as the five-way divider is symmetrical for all five connections.

![Figure 24. Five-way divider combining the outputs of four modules](image)

The four-tap signal is shown in Figure 25 with the programming values according Table 4. In this case, the second post-cursor is added inverted (subtracted) as the other cursors.

![Figure 25. The four-tap signal at 10 Gb/s based on a repetitive 0000000011111111 pattern](image)

<table>
<thead>
<tr>
<th></th>
<th>Main</th>
<th>Post_1</th>
<th>Pre</th>
<th>Post_2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay</td>
<td>1 UI</td>
<td>2 UI</td>
<td>0 UI</td>
<td>3 UI</td>
</tr>
<tr>
<td>Levels</td>
<td>±0.5 V</td>
<td>±0.25 V</td>
<td>±0.15 V</td>
<td>±0.15 V</td>
</tr>
<tr>
<td>Polarity</td>
<td>Normal</td>
<td>Inverted</td>
<td>Inverted</td>
<td>Inv (norm)</td>
</tr>
</tbody>
</table>

The experiments with various PC board traces show that the second post-cursor is needed without inversion. That is the reason why in Table 4 the polarity of post-cursor 2 is listed as “inv/(norm)”.

The delays of the four generators are adjusted to obtain a signal view as shown in Figure 26. It is important that the x-point of the four-channel occur at 50 percent of amplitude and with a 100 ps spacing (1 UI at 10 Gb/s.) The relative delay is important, not the absolute.

The Timing calibration of the channels is performed with help of the 81250A ParBERT deskew editor.

![Figure 26. Calibrated four-tap signal at 10 Gb/s with a repetitive 00000001 pattern in each channel](image)
De-Emphasis Labs with PC Board Traces

Lab 1: A short de-emphasis lab with three different PC board traces: The improvement while adding taps for a 320 mm PC board trace (one of three.)

All experiments on this and the consecutive pages are performed at data rate of 10 Gb/s and the setup with the five-way divider described in the prior section. All experiments begin with the main channel stimulating a PRBS7 pattern while the other channels send a PAUSE0. The post1-cursor is then added by sending the same PRBS7 delayed by 1 UI. The pre-cursor channel is added by sending the PRBS7 by 1 UI earlier (in reference to the main channel.) Finally, the post2-cursor is added by sending the PRBS7 by 2 UI later (in reference to the main channel.) All cursor amplitudes are varied until the optimum eye opening is obtained.

Table 5 lists the values for each of the cursors including the eye closure expressed by the remaining ISI value for a PC board trace 320 mm in length.

Again, the cursors are added incrementally from left to right in Table 5.

Table 5. Programming values and resulting ISI for the 320-mm trace

<table>
<thead>
<tr>
<th>320 mm</th>
<th>Main</th>
<th>Post_1</th>
<th>Pre</th>
<th>Post_2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay</td>
<td>1 UI</td>
<td>2 UI</td>
<td>0 UI</td>
<td>3 UI</td>
</tr>
<tr>
<td>Levels</td>
<td>±0.8 V</td>
<td>±0.18 V</td>
<td>±0.038 V</td>
<td>±0.038 V</td>
</tr>
<tr>
<td>Polarity</td>
<td>Normal</td>
<td>Inverted</td>
<td>Inverted</td>
<td>Inverted</td>
</tr>
<tr>
<td>ISI</td>
<td>0.36 UI</td>
<td>0.14 UI</td>
<td>0.13 UI</td>
<td>0.1 UI</td>
</tr>
</tbody>
</table>

Figure 27 shows the step response without any de-emphasis applied. This is taken with a pattern consisting of a single “1” surrounded by many “0”s. As can be seen, the step needs roughly 3 UI to settle 100 percent. Consequently, the eye is closed by roughly 1/3 as shown in Figure 28. Figure 29 adds the first post-cursor. The improvement of the eye opening is significant. The addition of pre- and post2-cursor (Figures 30 and 31) still improve the eye opening, but the necessary amplitudes for an optimization are small and the improvement is small.

Figure 30 depicts the step response with all three cursors in place (single one pattern, same as for Figure 25.) As can be seen, the step response is now clean and the signal settles mostly to 100 percent after one UI.
De-Emphasis Labs with PC Board Traces (continued)

Lab 1: A short de-emphasis lab with three different PC board traces: The improvement while adding taps for a 320 mm PC board trace (one of three) (continued)

Figure 31 shows the stimulus signal with all three cursors in place. The post1 cursor is dominant the pre- and post2-cursors are hard to see as the programming values are small at the optimum setting.

Figure 32 illustrates the corrected step response with the optimized 4-tap de-emphasis in place for the 320 mm pc board trace (repetitive pattern of 00000001). Figure 33 shows the waveform of the optimized 4-tap de-emphasized signal which is sent into the 320 mm pc board trace (repetitive pattern of 0000000011111111).

Lab 2: A short de-emphasis lab with three different PC board traces: The improvement while adding taps for a 535-mm PC board trace (two of three)

The second example is done with a PC board trace 535 mm in length. Figure 34 shows the step response without any de-emphasis applied (this is taken with a pattern consisting of a single “1” surrounded by many “0”s.) As can be seen, the step needs roughly 5 UI to settle 100 percent.

The eye is totally closed as shown in Figure 35 with the main signal only. Figure 36 adds the first post-cursor. The improvement of the eye opening is significant. The addition of pre- and post2-cursor (Figures 37 and 38) still improve the eye opening, but the necessary amplitudes for an optimization are small and the improvement is small.
De-Emphasis Labs with PC Board Traces (continued)

Lab 2: A short de-emphasis lab with three different PC board traces: The improvement while adding taps for a 535-mm PC board trace (two of three) (continued)

Table 6. Programming values and resulting ISI for the 535 mm trace

<table>
<thead>
<tr>
<th>535 mm</th>
<th>Main</th>
<th>Post 1</th>
<th>Pre</th>
<th>Post 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay</td>
<td>1 UI</td>
<td>2 UI</td>
<td>0 UI</td>
<td>3 UI</td>
</tr>
<tr>
<td>Levels</td>
<td>±0.8 V</td>
<td>±0.19 V</td>
<td>±0.02 V</td>
<td>±0.025 V</td>
</tr>
<tr>
<td>Polarity</td>
<td>Normal</td>
<td>Inverted</td>
<td>Inverted</td>
<td>Inverted</td>
</tr>
<tr>
<td>ISI</td>
<td>Closed</td>
<td>0.16 UI</td>
<td>0.14 UI</td>
<td>0.12 UI</td>
</tr>
</tbody>
</table>

Table 6 lists these values for each of the cursors including the eye closure expressed by the remaining ISI value for a PC board trace 535 mm in length.

Again, the cursors are added incrementally from left to right in Table 6.

Figure 35. Eye Diagram of the output of the 535 mm trace, PRBS7, no de-emphasis

Figure 36. Eye diagram of the output of the 535 mm trace, PRBS7, optimized two-tap de-emphasis

Figure 37. Eye diagram of the output of the 535 mm trace, PRBS7, optimized three-tap de-emphasis

Figure 38. Eye diagram of the output of the 535 mm trace, PRBS7, optimized four-tap de-emphasis

Figure 39. Step response of the 535 mm trace with optimized four-tap de-emphasis

Figure 39 depicts the step response with all three cursors in place (single one pattern). As can be seen, the step response is now clean, the signal settles mostly to 100 percent after 1 UI.
De-Emphasis Labs with PC Board Traces (continued)

Lab 2: A short de-emphasis lab with three different PC board traces: The improvement while adding taps for a 535-mm PC board trace (two of three) (continued)

Figure 40 shows the waveform of the optimized 4-tap de-emphasized input signal which is sent into the 535 mm pc board trace (repetitive pattern of 0000000111111111). The post1-cursor is dominating, the pre- and post2-cursors programming values are small at the optimum setting.

Lab 3: A short de-emphasis lab with three different PC board traces: The improvement while adding taps for an 850-mm PC board trace (three of three)

The third example is done with a PC board trace 850 mm in length. Figure 41 shows the step response without any de-emphasis applied. This is taken with a pattern consisting of a single “1” surrounded by many “0”s. As can be seen, the step needs more than 8 UI to settle 100 percent. The eye is totally closed as shown in Figure 42 with the main signal only. Figure 43 adds the first post-cursor. The improvement of the eye opening is significant. The addition of pre- and post2-cursor (Figures 44 and 45) still improves the eye opening, but the necessary amplitudes for an optimization are small and the improvement is small. The optimized eye opening is still bad as the transition time of the optimized eye is slow. This is also obvious from the Figure 46, which depicts the step response with all three cursors in place (pattern is repetitive 00000001).

As can be seen, the step response settles to 100 percent, but not within 1 UI.

The de-emphasis does not restore the transition time, so the bandwidth limitation of the long line cannot be compensated and the optimized eye opening remains marginal. Figure 47 shows the waveform of the optimized de-emphasized signal with all three cursors in place. The post1-cursor is dominating, the pre- and post2-cursor's programming values are small at the optimum setting. Note that the optimum post2-cursor in this example adds in contrast to the prior two experiments.
De-Emphasis Labs with PC Board Traces (continued)

Lab 3: A short de-emphasis lab with three different PC board traces: The improvement while adding taps for an 850-mm PC board trace (three of three) (continued)

Table 7 lists these values for each of the cursors including the eye closure expressed by the remaining ISI value for a PC board trace 850 mm in length.

Again, the cursors are added incrementally from left to right in Table 7.

Table 7. Programming values and resulting ISI for the 850-mm trace

<table>
<thead>
<tr>
<th>850 mm</th>
<th>Main</th>
<th>Post 1</th>
<th>Pre</th>
<th>Post_2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay</td>
<td>1 UI</td>
<td>2 UI</td>
<td>0 UI</td>
<td>3 UI</td>
</tr>
<tr>
<td>Levels</td>
<td>±0.8 V</td>
<td>±0.5 V</td>
<td>±0.05 V</td>
<td>±0.022 V</td>
</tr>
<tr>
<td>Polarity</td>
<td>Normal</td>
<td>Inverted</td>
<td>Inverted</td>
<td>Normal</td>
</tr>
<tr>
<td>ISI</td>
<td>Closed</td>
<td>0.3 UI</td>
<td>0.26 UI</td>
<td>0.23 UI</td>
</tr>
</tbody>
</table>

Lab summary

PC board traces have loss and bandwidth limitations, both increase with the length of the trace. The method with de-emphasis by multiple cursors compensates for the ISI caused by the loss and is able to open a totally closed eye. The method is limited for compensating bandwidth limitations: a degraded transition time cannot be compensated. Consequently, the method cannot correct every trace length at every data rate.
How to Set Up the ParBERT 81250A for IEEE 802.3aq (10 GBASE–LRM)

We use the setup of Figure 24: four modules combined with help of a five-way divider. The timing calibration has to be performed based on the 75-ps spacing and it has to be done channel by channel (in the overlay as shown in Figure 26 one could not see the transitions.) The output of the five-way divider is connected with a 7.46-GHz Bessel Thompson Filter to achieve the required shaping. Another important consideration is the bandwidth of scope to visualize the step response. The step response examples shown in this section assume a scope input bandwidth of 7.5 to 10 GHz.

When using higher bandwidth, additional filtering is required. The programming of the four ParBERT channels is given in Table 8. It lists delay, levels, and pattern. Patt1 is a segment consisting of 1000000000000000 (1x '1', 15x '0'). To visualize the step response, the pattern with a single one is recommended. For a real test the desired pattern (e.g. PRBS) has to be loaded in all four channels except where Table 8 lists the PAUSE.

Table 8. Programming values for pre-, symmetric, and post-cursor according to IEEE 802.3aq (base LRM)

<table>
<thead>
<tr>
<th>850 mm</th>
<th>Channel 1</th>
<th>Channel 2</th>
<th>Channel 3</th>
<th>Channel 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay</td>
<td>0 ps</td>
<td>75 ps</td>
<td>150 ps</td>
<td>225 ps</td>
</tr>
<tr>
<td>Pre</td>
<td>Levels</td>
<td>±0.158 V</td>
<td>±0.176 V</td>
<td>±0.499 V</td>
</tr>
<tr>
<td></td>
<td>Pattern</td>
<td>Patt1</td>
<td>Patt1</td>
<td>Patt1</td>
</tr>
<tr>
<td>Symm</td>
<td>Levels</td>
<td>±0.000 V</td>
<td>±0.153 V</td>
<td>±0.000 V</td>
</tr>
<tr>
<td></td>
<td>Pattern</td>
<td>Paused</td>
<td>Patt1</td>
<td>Paused</td>
</tr>
<tr>
<td>Post</td>
<td>Levels</td>
<td>±0.254 V</td>
<td>±0.453 V</td>
<td>±0.155 V</td>
</tr>
<tr>
<td></td>
<td>Pattern</td>
<td>Patt1</td>
<td>Patt1</td>
<td>Patt1</td>
</tr>
</tbody>
</table>

Figure 48. Channel characteristic from ParBERT 81250A for pre-cursor definition according IEEE 802.3aq (base LRM)

Figure 49. Channel characteristic from ParBERT 81250A for symmetric cursor definition according IEEE 802.3aq (base LRM)

Figure 50. Channel characteristic from ParBERT 81250A for postcursor definition according IEEE 802.3aq (base LRM)
References

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