MMIC/RFIC Packaging Challenges

Webcast
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HEESOO LEE
Agilent EEsof
3DEM Technical Lead
Agenda

1. MMIC/RFIC packaging challenges
2. Design techniques and solutions that improve package performance
3. The value of chip/package co-design
   - Case study: RFIC differential power amplifier
4. Conclusion
What Applications We Will Cover…

Agilent Custom TOPS Package  Agilent QFN Package  Solder Bumps for FC Package

Balun + Mixer IC Module  RFIC PA Co-Design
1. MMIC/RFIC Packaging Challenges
MMIC/RFIC Packaging Trends

- Smaller, Cheaper, Faster
- Smaller form factor packages and higher integration
  - Higher pin counts and smaller ball/pad pitch
  - Embedded passives on module level multi-layer substrates
  - Multi-technologies – RF, MEMs, Logic, Analog, DRAM...
- Lower cost and low power packages
- More wafer level packaging process
- Emerging 3DIC packaging technology
- Increasing thermal challenges
Packaging Technologies and Modeling Approaches

High Speed Digital Package

• Larger and complex
• Typically use time-domain simulations
• Spice models are generally required: Provide Intuitive physical meaning for package structures
• Tedious and time consuming process for model extraction where EM simulations are extensively used

MMIC/RFIC Package

• Smaller and simpler
• Typically use frequency domain simulations
• Spice models are not always necessarily required but good to have them
• Possible to use EM models directly, which are multi-port S-parameters
• Broadband Spice Models can also alternatively be used but no intuitive physical meaning for the package
3D EM Simulation Technologies

- **FDTD** (Finite Difference Time Domain)
- **FEM** (Finite Element Method)
- **MoM** (Method of Moment)

**FDTD**:
- 3D arbitrary structures
- Full Wave EM simulations
- Handles much larger and complex problems
- Time Domain EM
- Simulate full size cell phone antennas
- EM simulations per each port
- GPU based hardware acceleration

**FEM**:
- 3D Arbitrary Structures
- Full Wave EM Simulation
- Direct, Iterative Solvers
- Frequency Domain EM
- Multiport simulation at no additional cost
- High Q

**MoM**:
- 3D Planar structures
- Full Wave and Quasi-Static
- Dense & Compressed Solvers
- Frequency Domain
- Multiport simulation at no additional cost
- High Q
Agilent EEsof’s Integrated 3D EM Flow

Package Designers

EMPro Platform

Parameterized 3D Components

Layout CAD Data

FDTD Simulator

FEM Simulator

Momentum Simulator

MMIC/RFIC Designers

ADS Platform

Agilent Technologies
2. Design Techniques and Solutions that Improve Package Performance
Example 1: Agilent’s High Performance Custom TOPS Package

TOPS Package features:

- Micro-circuit performance up to 50 GHz and 40Gb/s with SMT Technology
- Excellent thermal (heat dissipation) capability
- Small form factor (10 mm x 10 mm) and non-hermetic molded LCP (Liquid Crystal Polymer)
- Low cost and high volume assembly/test with fast coax E-cal process
Measured Transition Performance of TOPS Package

(PCB – Package – BondWire – ThinFilm Load)

Excellent performance up to 50GHz

Cal PCB data used to correct for PCB and connector losses

Less than 20dB
Design Techniques Used to Improve TOPS Package Performance

1. Double wedge bonding for reducing effective inductance
   - 26 µm Diameter, 25µm bond height

2. Optimized bond pad size for low pass configuration
   - 30 fF shunt capacitance with 200µm X 100 µm

3. Optimized via and pad size for reducing reflections

4. High frequency PTFE for package substrate

Circuit Model

Bondwire Performance (Model vs. EM)

Return Loss

Phase Response
Example 2: Agilent 3x3 [mm] 16 Pin QFN Package

Top metal – 0.1 mm thick

Bottom metal – 0.1 mm thick

Plastic encasement
0.2 mm thick

Bottom View

Die Paddle

Top View
Non-Optimized QFN Package Performance With 50Ohm Thru Line on Al Substrate

- Microstrip line on Al Substrate
- Chip
- Board Microstrip Feed
- PCB vias from QFN to ground
- Double bond wires
- Board

Good Up to 15 GHz!
Design Techniques Used to Improve QFN Package Performance

Increase the width of input/output transmission lines to 50 Ω impedance – Easy to optimize in ADS

Use two lead frames to maintain a good transitional impedance profile and split the double bondwires onto the two leads

1. Wider transmission line (50 Ω)
2. Use split bond wires onto two leads
Improved Package Performance

![Graph showing dB(S11) and dB(S21) vs. freq, GHz. The graph compares Red & Blue: Improved Design with Cyan & Dark Green: Original Design.]
3D Component Technology for 3D EM Simulations

Bridges IC and package designers in 3D EM and circuit simulation space

Augments ADS 2D layout drawing into 3D EM space for packages

Two types of 3D components

- ADS default 3D components
- Custom Parameterized 3D components
Example 3: Solder/Wafer Bumps for Flip Chip Packaging

Solder/Wafer Bumps are very typical interconnect technology for Flip-Chip, CSP, and WLP applications

3D full wave EM simulations are required to characterize it and analyze board interactions with face-down flip chip
Solder Ball/Bump ADS Default 3D Component

Greatly reduce the risk that comes with the final integration by co-designing the circuit, package, and board interface together. Use solder bumps from ADS default 3D component library, and get the most accurate prediction of the overall behavior.
Simulated Isolation Performance between Bumps

Isolation Characteristic

dB(S(2,1))

freq, GHz

Simulation Time: Only 5 min 25s on quad-core processor!

Less than 20 dB Isolation
Build Custom Package 3D Component Library for ADS Circuit/EM Co-Simulations

Build a set of package 3D component library for ADS

- Very useful library when a package is often combined with a layout
- Makes dynamic EM simulations for package plus layout a lot easier
- Multiple packages can be added to the package 3D EM component design kit
Example 4: Mixer on DFN Package with Merchant LTCC Balun

Drop-in DFN on module layout

3D View

LTCC Balun
Simulated Performance (IC, Package, Balun...)

Noise Contributor Listing

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LO2F isolation=27.654 dB
RF2F Isolation=31.67 dB
RF2LO Isolation=33.5 dB

Agilent Technologies
3. The Value of Chip/Package Co-Design
Sequential vs. Co-Design Process

**Sequential Design Process**

- Project Start → DR1 → DR2 → DR3 → DR4 → Integration
- DR1 → DR2 → DR3 → DR4

**Con-current Co-Design Process**

- Project Start → DR1 → DR2 → DR3 → DR4
- DR1 → DR2 → DR3 → DR4

Integration

OK? → Y → Done

N → Done
Chip/Pkg/Module Co-Design Case Study
RFIC Differential Power Amplifier Test Board

- Bondwires
- Single Ended PA Input
- Single Ended PA Output
- PCB
- LTCC Balun
- Si PA
- LTCC Balun
- Package
The Old Way, Sequential Design Process

Chip Design  
Meet Spec? 100%

Package Design  
100%

Module Design  
100%  Meet Spec?

Final Integration  
On PC Board!

Expect 100% x 100% x 100% = 100%
Let’s Prove Whether The Integration Works
RFIC PA + Balun

RFIC PA, integrated with Ideal and LTCC Balun, meets the performance goals
Let’s Prove Whether The Integration Works
Final Integration of Balun + RFIC PA + Package
Unexpected or Unpredicted Parasitic Resonance Caught in Last Minute Final Integration Test!

Unexpected parasitic resonance around 1.7 GHz

How will this unexpected or unpredicted behavior impact on the development schedule?
Last Minute Design Failure Could Impact Greatly on Design Wins and Time to Market

What if, this is a design failure to meet the spec?
So, will you re-spin the chip? $$$ & TTM
Or re-spin the package? $$$ & TTM
Or bandage the design or just blame others?
Integrated 3D EM for Successful IC Designs

MMIC/RFIC designers must take the package performance into consideration since IC design is not finished until it is packaged.

Integrated 3D EM allows MMIC/RFIC designers to test, verify, and optimize IC circuits with 3D packages continuously and quickly without leaving their circuit design environment.
Proposed Chip/Package/Module Co-Design (Concurrent) Process
4. Conclusion

In modern MMIC/RFIC designs, the package performance is the critical success factor for product design wins.

Integrated 3DEM design flow makes product design cycle shorter and much more efficient.

Co-design process for chip and package enables faster and cheaper product designs.
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