Applications for lower operating rates

In addition to the 9.85 – 11.35 Gb/s standard operating rates, the new enhanced data rates include many standardized protocol rates. The standards covered by the new range of operation include:

- 1 GbE (1.25 Gb/s)
- SONET OC-48 STM-16 (2.488 Gb/s)
- 2x GbE (2.5 Gb/s)

Specifications for N4962A serial BERT 12.5 Gb/s

The range of each data rate is:

<table>
<thead>
<tr>
<th>Data Rate</th>
<th>Synth Mode</th>
<th>Minimum Step</th>
<th>Maximum Range</th>
<th>Minimum Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 Gb/s</td>
<td>1</td>
<td>10 MHz</td>
<td>11.35 Gb/s</td>
<td>9.850 Gb/s</td>
</tr>
<tr>
<td>5 Gb/s</td>
<td>2</td>
<td>5 MHz</td>
<td>5.675 Gb/s</td>
<td>4.925 Gb/s</td>
</tr>
<tr>
<td>2.5 Gb/s</td>
<td>4</td>
<td>2 MHz</td>
<td>2.837 Gb/s</td>
<td>2.462 Gb/s</td>
</tr>
<tr>
<td>1.25 Gb/s</td>
<td>8</td>
<td>1 MHz</td>
<td>1.418 Gb/s</td>
<td>1.231 Gb/s</td>
</tr>
</tbody>
</table>

Table 1. Data ranges and step sizes
In Figure 1, the block diagram of the N4962A serial BERT 12.5 Gb/s is shown with the addition of blocks 4 and 5, which contain the external programmable clock dividers.

In block 4, the transmitter clock output (TX CKO) is connected to the divider input. The TX clock may optionally have jitter injected onto the source. In block 5, the receiver clock output (RX CKO) is connected to the divider input. This clock is separately divided, as it may not have the optional jitter injected onto the TX clock.

Both TX and RX clock dividers are controlled via the front panel interface, or the GPIB programming interface.

Figure 1. 10 Gb/s BERT system block diagram
The programmable external dividers are controlled through the front panel with the `synth` configuration command. The values for `synth` are shown on Table 1. This option allows the internal clock to be disabled, and directs the divider to operate in the clock loops.

When supplying an external clock to RX CKI and TX CKI, with `synth = 0`, the frequency of operation must be programmed on the display. The display for frequency will show “X 10.000” meaning 10Gb/s and the X denotes an external source.

The clock rate based on the divider amount for the internal synthesizer is shown in Table 1 where `synth` is set to 1, 2, 4, 8. The corresponding frequency ranges are shown in the Table 1.

The minimum step size for the frequency changes with the divide ratio changes if controlled with the front panel. Table 1 shows the step sizes which are used on the display with the front panel control. The GPIB allows for 1 MHz step sizes regardless of the divider rate.

**GPIB control of divider option**

The GPIB control is also set using the `source` command. Using the `INternal` step without any divider is the 10Gb/s range.

<table>
<thead>
<tr>
<th>Data rate</th>
<th>Rms jitter</th>
<th>Tj (pp jitter)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10.0 Gb/s</td>
<td>1.05 ps</td>
<td>6.22 ps</td>
</tr>
<tr>
<td>5.0 Gb/s</td>
<td>1.23 ps</td>
<td>6.67 ps</td>
</tr>
<tr>
<td>2.5 Gb/s</td>
<td>1.25 ps</td>
<td>7.78 ps</td>
</tr>
<tr>
<td>1.25 Gb/s</td>
<td>1.27 ps</td>
<td>7.78 ps</td>
</tr>
</tbody>
</table>

*Table 2. Performance of divided data rates*

It is very important to program the correct frequency which corresponds to the divider rate selected. The system error of –222 will result if this procedure is not followed. With the GPIB interface, the frequency step size is 1 MHz, regardless of the divider rate.

Examples:

```
:SOURCE:ROSC:SOURCE  INT
:SOURCE:ROSC:FREQ 1125

:SOURCE:ROSC:SOURCE  DIV2
:SOURCE:ROSC:FREQ 4990

:SOURCE:ROSC:SOURCE  DIV4
:SOURCE:ROSC:FREQ 2500

:SOURCE:ROSC:SOURCE  DIV8
:SOURCE:ROSC:FREQ 1250
```

The following example shows how to “incorrectly” program for an external divider.

```
:SOURCE:ROSC:SOURCE  INT
:SOURCE:ROSC:FREQ 1250
```

Result: System errors=-222, “Data out of range”
Conclusion

The divider option for the N4962A serial BERT 12.5 Gb/s allows for multiple data rate testing over a large range without using an external synthesizer.

The jitter performance is maintained across all divider ratios for both random and deterministic jitter as shown in Table 2. The jitter measurement shown in Figure 2 was taken at 5.0 Gb/s, and illustrates the excellent performance.

The amplitude and phase controls still work without any changes. The jitter injection feature also works over all data ranges. The total amount of jitter injected on the waveform is reduced by the divider rate. This may require higher signals to be applied to the jitter input port for the same UI of jitter induced at the higher data rate.

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