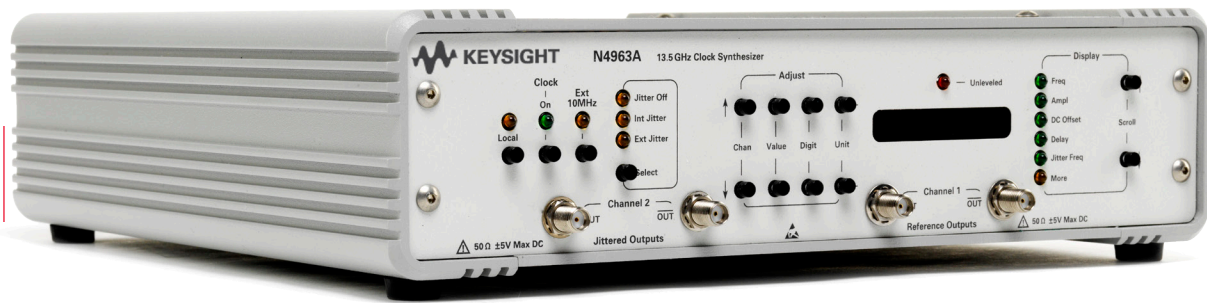


Keysight

N4963A Clock Synthesizer 13.5 GHz

Data Sheet





Introduction

Applications

- Designed to extend the operation of the Keysight Technologies, Inc. N4962A serial BERT 12.5 Gb/s for continuous operation from 500 Mb/s to 12.5 Gb/s.
- XAUI BERT tester using four N4962A serial BERT 12.5 Gb/s and the N4963A clock synthesizer 13.5 GHz to enable a synchronous four lane BER tester at a fraction of the cost from competitors.
- Stand alone lab clock source for general purpose use.

Features

- Small compact size
- Wide range 500 MHz to 13.5 GHz square wave generator
- Jitter injection capability from 1 Hz to 100 MHz
- Six pairs of differential outputs, 3 pairs jittered and 3 pairs unjittered
- One set of differential outputs offer independent delay adjustment relative to the other outputs
- Wide range of amplitude (600 to 2000 mV)
- DC offset adjustable for driving different logic types (-2.0 to 2.0 V)
- GPIB controllable for automated use
- Very low jitter typically < 1.5 ps rms

Specifications

Specifications	
All clock outputs	
Frequency of operation	0.5 to 13.5 GHz
Frequency resolution	1 kHz when GPIB controlled 1 kHz at frequencies < 1GHz when front panel controlled 1 MHz at frequencies \geq 1 GHz when front panel controlled
Frequency accuracy	+/- 5 ppm maximum
Rise/fall times (20 to 80%)	< 50 ps typ from 0.5 to 10 GHz < 25 ps typ from 10 to 13.5 GHz
Jitter	2.6 ps rms typ from 0.5 to 2.5 GHz 1.5 ps rms typ from 2.5 to 13.5 GHz
Front panel outputs (channel 1 and channel 2)	
Amplitude	0.6 to 2.0 V from 0.5 to 7.5 GHz 0.6 to 1.5 V from 7.5 to 13.5 GHz
Amplitude resolution	1 mV
Offset voltage	-2.0 to +2.0 V
Offset voltage resolution	10 mV
Phase adjust (channel 1 only)	-180 to +178 °
Phase adjust resolution (channel 1 only)	2 °
Interface	Differential. DC coupled, 50 Ω nominal, female SMA (May be operated single end without unused output terminated into 50 Ω)
Rear panel outputs (channels 3A, 3B, 4A, 4B)	
Amplitude	0.2 to 0.8 V from 0.5 to 7.5 GHz 0.2 to 0.6 V from 7.5 to 13.5 GHz
Amplitude resolution	1 mV
Interface	Differential. AC coupled, 50 Ω nominal, female SMA (May be operated single end without unused output terminated into 50 Ω)
Jitter injection (Option 101)	
Jitter injection source	Internal or external
Jittered outputs	Channel 2 (front panel) and channels 4A and 4B (rear panel)
Jitter injection frequency range	1 Hz to 100 MHz
Jitter injection frequency resolution (internal)	1 Hz from 1 Hz to 1 MHz injection frequency 1 kHz from 1 to 100 MHz injection frequency
Jitter injection range ¹	0 to 32 UI from 1 to 75 kHz 0 to 16 UI from > 75 to 150 kHz 0 to 8 UI from > 150 to 300 kHz 0 to 4 UI from > 300 to 600 kHz 0 to 2 UI from > 600 kHz to 1.2 MHz 0 to 1 UI from > 1.2 to 2.4 MHz 0 to 0.6 UI from > 2.4 to 100 MHz
Jitter injection resolution	0.01 UI
External jitter input voltage	1 V pp max
External jitter injection interface	DC coupled, 50 Ω nominal, female SMA

1. At 5 GHz

Specifications	
Trigger output	
Type	Divided clock trigger
Trigger divide range	Division ration 8 to 511 in steps of 1
Trigger frequency	Clock frequency/trigger division ratio
Amplitude	> 400 mV typ
Interface	AC coupled, 50 Ω nominal, female SMA
Nominal timebase specifications	
Reference frequency	10 MHz internal or external
10 MHz external input frequency	10 MHz \pm 10 ppm
10 MHz external input amplitude range	0.5 to 2 Vpp
10 MHz reference output	500 mVpp
Interface	AC coupled, 50 Ω nominal, female BNC
General and mechanical parameters	
General and mechanical parameters	
Operating temperature	+10 °C to +40 °C
Storage temperature	-40 °C to +70 °C
Power requirements	42 W external AC adaptor (included) 100 to 240 V AC, 47 to 63 Hz
Weight	3.4 kg (7.5 lbs)
Regulatory standards	
EMC	
Complies with European EMC Directive 2004/108/EC	IEC/EN 61326-1 CISPR Pub 11 Group 1, class A AS/NZS CISPR 11 ICES/NMB-001
	This ISM device complies with Canadian ICES-001. Cet appareil ISM est conforme a la norme NMB-001 du Canada.

Rear view of N4963A clock synthesizer 13.5 GHz

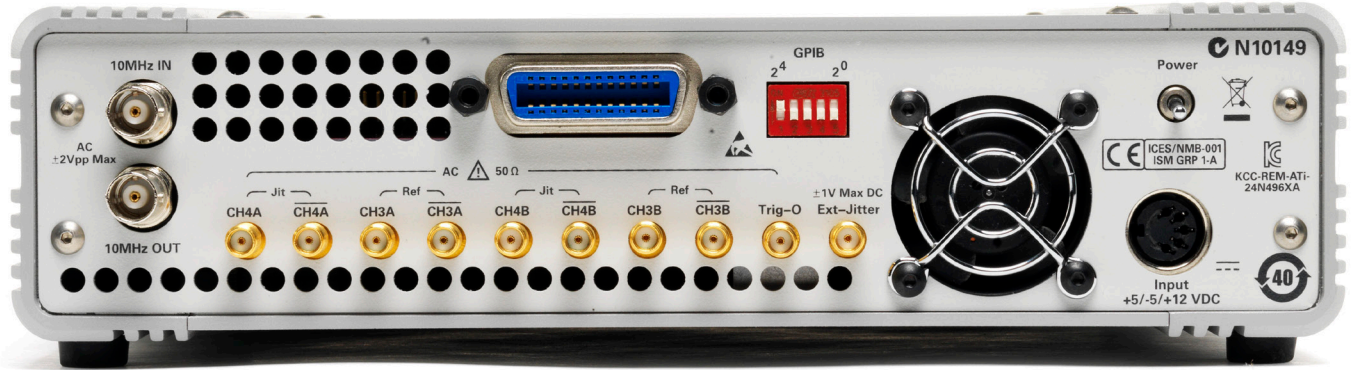


Figure 1. Rear view

Block diagram

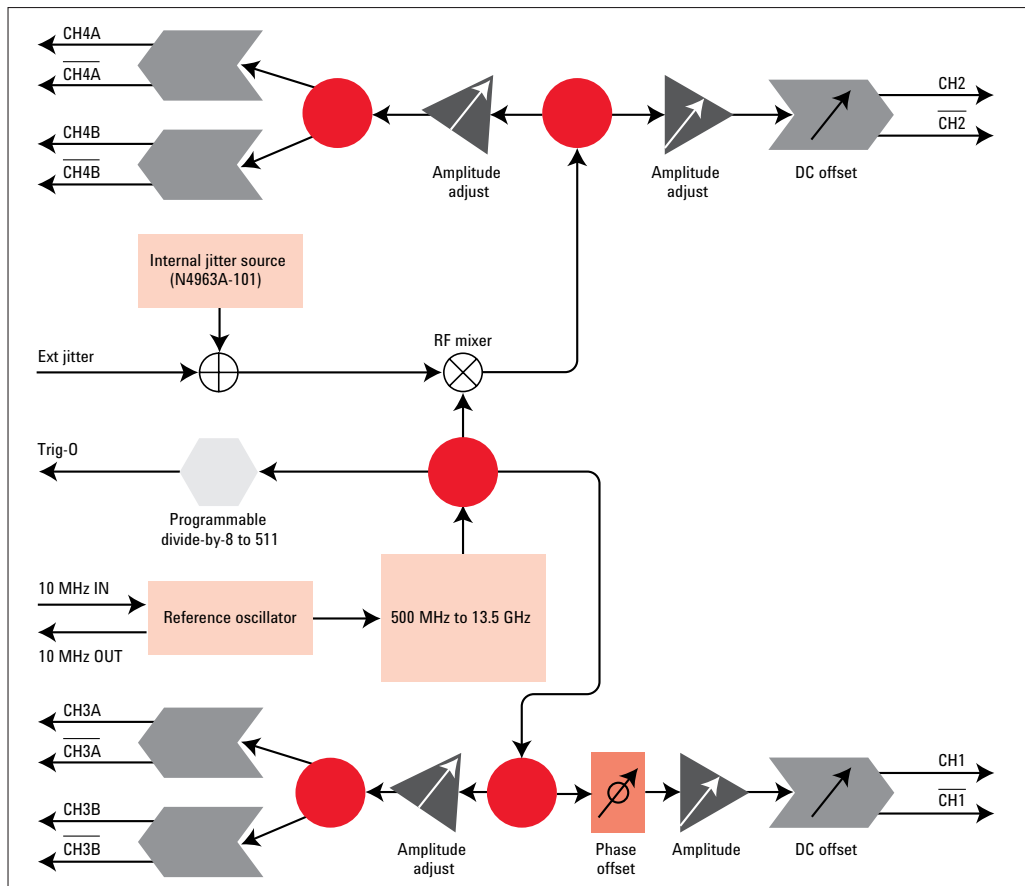


Figure 2. Block diagram

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