Keysight Technologies
Increase Multi-Antenna Array Test Throughput with the M9703A AXIe Digitizer

Application Note

Abstract

Smart antenna architectures incorporating multiple antenna elements in an array are used in many applications. Wireless communications standards like 802.11ac, radio astronomy and array RADARs are all examples of applications where multiple antennas are employed for various requirements derived from spatial signal processing. Though the types of processing used and beamforming techniques differ by application, there is a common test challenge. It is difficult to align the antennas in an array in phase and amplitude so they can be used together effectively. As the number of antennas increase in an array, the test time to do the alignment increases drastically. This application note addresses the challenge of aligning the antennas in an array precisely, while reducing test time. The note also provides details on a multichannel, phase coherent test solution which can be customized to quickly and precisely align antenna elements in an active array, both in phase and amplitude. This test solution is built from modular components and is easily scalable to the number of antennas in the array being tested. Further, it provides parallelism to the test process to increase test throughput. The test system described offers flexibility to provide good sensitivity in both the wideband and narrowband measurement scenarios using the same hardware.

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Introduction

Extra production test time adds manufacturing cost. For active antenna arrays, a significant amount of production test time is spent on calibration. As engineers face pressure to reduce manufacturing cost, they also want to expand their test system flexibility to cover testing broad use cases and ensure they have a test platform that can also test higher performance arrays with even faster frequency switching performance and higher bandwidths.

Engineers traditionally rely on CW tone testing for aligning multiple antennas during their integration in a phased array. But, the choice of using only CW tones is often driven by bandwidth limitations of the existing test systems, such as vector network analyzers, which may not test an array's full range of intended operation. In some applications or operating modes the multi-antenna array will be transmitting or receiving signals that have bandwidth, such as pulsed RF, other types of modulation. A test solution with greater bandwidth is beneficial as long as it also offers good sensitivity for narrowband CW measurements. The dilemma of having wide bandwidth while also providing good narrowbandwidth sensitivity is often problematic since a wideband analyzer integrates more noise power across its wider bandwidth, thereby inherently reducing sensitivity.

This application note provides an overview of the key issues in a phased antenna array test system related to the use and selection of a digitizer. Further, it offers a solution to increase test throughput using the modular Keysight AXIe M9703A ("digitizer").

Figure 1. M9703A AXIe 12-bit digitizer.

Figure 2. M9703A AXIe 12-bit digitizer and M9536A embedded AXIe controller in M9505A 5-slot chassis.

Key issues faced by antenna array test engineers

This application note addresses test challenges faced by antenna array engineers including:

- The need for fast wideband, high resolution sampling of IF signals post downconversion.
- The need to achieve phase coherent sampling across all input channels, providing relative magnitude and phase measurements
- The need to make different trade-offs between sensitivity and analysis bandwidth per the test scenario

First, the antenna signal enters a microwave mixer block to down-convert the µW/RF coming off the antenna array to an IF within the 3 dB analog bandwidth of the digitizer. There are a variety of choices for the mixer block and local oscillator depending on the input frequency and acceptable conversion loss. The carrier frequencies can range from S to Ka band (2 to 40 GHz).

Second, the signal passes through several possible attenuation/gain and filter stages to maximize the use of the digitizer's dynamic range and front-end characteristics.

Finally, the signal is discretely sampled by the digitizer. If the IF bandwidth needed is significantly narrower than the approximate 800 MHz of Nyquist (1.6 GSa/s) bandwidth from the digitizer, then a digital down conversion (DDC) process can be used to tune and zoom full bandwidth analog-to-digital converter output data to the narrower frequency analysis band of interest. Using the DDC will reduce the integrated noise power in-band and therefore increase signal to noise ratio (SNR). The noise power decreases by

$$10 \text{ x } \log\left(\frac{BW_{Fin}}{BW_{Init}}\right)$$

if the noise power is random and spread evenly over the entire spectrum.

Sample rate	Analysis bandwidth
1.6 GS/s[1]	800 MHz
400 Ms/s	300 MHz
200 Ms/s	160 MHz
100 Ms/s	80 MHz
50 Ms/s	40 MHz
$50/2^n$ Ms/s	$40/2^n$ MHz

Figure 3. M9703A-DDC sampling rate and bandwidth modes.

1. At 1.6 GS/s, full non-interleaved sampling rate without DDC.

Using the M9703A to accelerate resting

The M9703A digitizer offers unique features that:

- Enable multiple parallel measurements to increase test throughput
- Provide more bandwidth and larger synchronous input channel counts than any network analyzer solution on the market
- Provide possible configuration for measurements from narrow to wide frequency spans with optimized sensitivity and resolution.

The digitizer integrates eight high speed, high resolution digitizer channels into a single card. Multiple units of the digitizer can be integrated into a single Keysight AXIe chassis. The Keysight M9505A chassis can hold five units providing 40 channels of data acquisition in a single desktop system. With a 50 Ohm DC coupled input, the digitizer can be easily combined with several upstream signal conditioning and downconverter modules to create a total test solution. The solution can be adapted to accommodate different power levels coming from the antenna array elements, test solution IF frequencies selected and physical form factor requirements. Keysight provides a wealth of products and measurement expertise to help with the best application fit.

Synchronization of the system can be achieved using a choice of external or system reference clock inputs. Timing and triggering signals available from the AXIe backplane include:

- System 100 MHz clock
- 100 MHz PCIe clock
- Point to point star trigger from the embedded system module (ESM)
- Bi-directional point-to-point star trigger
- 12 lane parallel trigger bus.

The M9703A provides two I/O outputs that provide status signals to enable engineers to optimize test plan synchronization between arming the digitizer's trigger to starting the device under test (DUT) in the next test phase. One example of this is the "Acquisition Running" status signal. When the acquisition state changes from "running" to "idle" the output level changes and notifies the engineer that the test system is ready for a DUT state change. Connection to a controlling PC can be made via a cabled PCIe connection to the ESM, or alternatively, an embedded processor such as the M9536A can be used to control the acquisition system from one of the AXIe slots.

Summary

Using this M9703A as the digitizer core of an antenna array test solution means you recognize the value of increasing test throughput by making multiple measurements in parallel to increase production capacity. While testing fast often is associated with lower resolution measurements, using the M9703A's multiple channels allows the same tests to be performed, just with multiple tests running in parallel in one AXIe chassis. Furthermore, with the use of DDC digital signal processing algorithms, you can trade-off analysis bandwidth for signal to noise ratio to customize the solution for each test without swapping out the digitizer hardware.

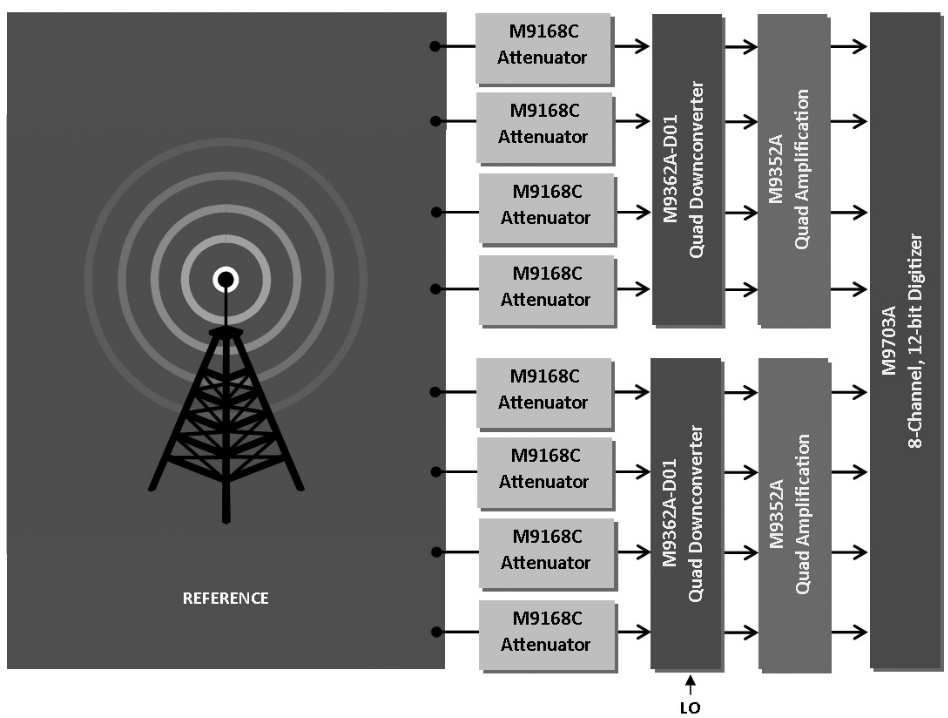

Figure 3. Example of an antenna array test range configuration

Ordering information

Model	Description
M9703A	AXIe 12-bit Digitizer
Base Configuration Options	
M9703A-SR1 [1]	1 GS/s Sampling Rate
M9703A-SR2	1.6 GS/s Sampling Rate
M9703A-INT	Interleaved Channel Sampling
M9703A-F05 [1]	650 MHz Maximum Analog Bandwidth
M9703A-F10	1 GHz Bandwidth Additional Path
M9703A-M10 [1]	1 GB (64 MS/ch) Acquisition Memory
M9703A-M20	2 GB (128 MS/ch) Acquisition Memory
M9703A-M40	4 GB (256 MS/ch) Acquisition Memory
M9703A-DDC	Digital down-conversion firmware
Related Products	
M9502A	2-slot AXIe Chassis
M9505A	5-slot AXIe Chassis
M9536A	Embedded AXIe Controller
M8190A	AXIe 12 GSa/s Arbitrary Waveform Generator

1. These options are included in the default configuration of the M9703A.

Software information

Chassis slot compatibility: AXIe, ATCA	
Supported operating systems	Microsoft Windows XP (32-bit) Microsoft Windows 7 (32/64-bit) Microsoft Windows Vista (32/64-bit) Linux
Keysight IO Libraries	Includes: VISA Libraries, Keysight Connection Expert, IO Monitor
Typical System Configuration	
M9703A	8-channel, 12-bit, AXIe Digitizer
M9703A-SR2	1.6 GS/s Sampling Rate
M9703A-DDC	Digital down-conversion firmware
M9505A	5-slot AXIe Chassis
M9048A	PCIe desktop PC adapter
89601B	89600 VSA software, transportable license

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