Conventional ADC testing solution can be complex and expensive

The servo-loop based ADC testing method (Figure 1) is widely used to evaluate an ADC's differential & integral non-linearity (DNL/INL). However, this technique has several issues:

– Issue 1: This test method requires many different components, such as a voltage/current source, a digital multimeter (DVM), servo circuitry, etc. It also requires a complicated program to control and synchronize everything.

– Issue 2: Conventional voltage/current sources used in the servo-loop test require significant averaging to eliminate noise as well as frequent PC communication, creating lots of test overhead time.

– Issue 3: The histogram testing method is the most desirable technique due to its simplicity and efficiency; however, most conventional instrumentation does not have the required resolution, noise floor and linearity to test high bit ADCs.

B2961A/62A with LNF option streamlines 14-bit ADC testing

– Solution 1: The B2961A/62A with its low noise filter (LNF) has superior source resolution that does not require external monitoring by a DVM. This improves and simplifies ADC testing.

– Solution 2: The superior noise performance of the B2961A/62A with its LNF reduces averaging times. In addition, its external trigger input and 100k point waveform memory reduce PC communication frequency. All of these factors improve ADC testing efficiency.

– Solution 3: The B2961A/62A's excellent arbitrary waveform generation function linearity supports ramp voltage histogram evaluation of 14-bit ADC DNL/INL. Using the simple test setup shown in Figure 2, two examples of DC performance testing for off-the-shelf ADCs will be shown on the next page.
Example 1: 12 bit ADC step voltage test using external trigger and waveform memory

DUT:
*ATXMEGA256A3BU MCU built in 12 bit SAR ADC
Vref = 2.0 V
Step voltage source:
B2961A with LNF
20 uV * 100 k steps, 0 V to 2.0 V

Unlike the servo-loop based method, the simpler B2961A/62A test setup eliminates the convergence loop and reduces PC communication frequency. The B2961A/62A’s 6.5 digit source resolution and better noise performance eliminate the need for DVM monitoring. In addition, the external trigger port and internal waveform memory improve ADC testing efficiency. As a result, the B2961A/62A with LNF allows you to implement simpler ADC testing methods and speed-up your testing.

Figure 3 shows DNL error of 12 bit ADC measured by B2961A with 0.04 LSB size steps of voltage based on Figure 2 test setup.

Example 2: 14 bit ADC linear ramp voltage histogram test for DNL/INL measurement

DUT:
ADS8324EVM 14 bit SAR ADC evaluation board
Vref = 1.6 V
Ramp voltage source:
B2962A with LNF
30 sec ramp, -50 mV to 3.25 V
Averaged 8 times

An ADC’s DNL/INL performance can also be tested by applying a ramp voltage using the B2962A (histogram test). In this test method the ADC samples the ramp voltage at even intervals. This method requires a very linear voltage source, but the measurement time is shorter and the ADC controller can be simpler as compared to the step voltage method. The B2961A/62A’s arbitrary waveform generation function has the necessary linearity to permit evaluation of 14 bit ADC DNL/INL using a ramp voltage.

Note: The B2961A/62A can also generate low distortion sinusoidal voltages.

Keysight B2961A/B2962A Low Noise Power Source Key Specifications and Characteristics

<table>
<thead>
<tr>
<th>Product Number</th>
<th>Option</th>
<th>Max DC output</th>
<th>Source Resolution</th>
<th>Output Noise 1 (10 to 20 MHz)</th>
<th>Source Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>B2961A</td>
<td>….</td>
<td>210 V/3.03A</td>
<td>6 1/2 digit</td>
<td>3 mVrms</td>
<td>– Arbitrary waveform generation</td>
</tr>
<tr>
<td>B2962A</td>
<td>LN1</td>
<td>42 V/105 mA</td>
<td>6 1/2 digit</td>
<td>10 μVrms</td>
<td>– Programmable output resistance</td>
</tr>
<tr>
<td></td>
<td>LN2</td>
<td>210 V/3.03 A</td>
<td>6 1/2 digit</td>
<td>350 μVrms</td>
<td>– Time domain waveform viewer</td>
</tr>
</tbody>
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1. Supplemental characteristics