Keysight Technologies
Modifying DDR Libraries for Silicon Nail Test Generation on the x1149 Boundary Scan Analyzer
1. When silicon nail test is not generated during the Keysight Technologies, Inc. x1149 test:

   ![Image](image1.png)

   The output message shows that the following nodes “MQ0_SDR0_DM” and “MQ0_SDR0_ZQ” are not connected to a boundary scan cell or resource.

2. Check the output message:

   ![Image](image2.png)

   The output message shows that the following nodes “MQ0_SDR0_DM” and “MQ0_SDR0_ZQ” are not connected to a boundary scan cell or resource.

3. Check the board details to find out if the “MQ0_SDR0_DM” and “MQ0_SDR0_ZQ” are connected to a DDR and the boundary scan device pins.

4. The node “MQ0_SDR0_DM” in the node list shows the DDR pins D03 and E07 are shorted and connected to resistor “R981” and the pull down is set to “GND”.

5. Do the same for the other node “MQ0_SDR0_ZQ”, which is connected to resistor “R971”, with the pull down set to “GND”.

6. The nodes “MQ0_SDR0_DM” and “MQ0_SDR0_ZQ” are not connected to any boundary scan cell or resource. This is the reason why the silicon nail test could not be generated.
7. In order to generate the silicon nail test for the u901 DDR3, the DDR3 library has to be modified as follows:

7.1 Change the pin usage of the group DM (u901.E07 and u901.D03) and ZQ (U901.L08) from inputs to non-digital.

7.2 Comment the vector where the DM and ZQ are declared.

8. Once the DDR3 library has been modified, regenerate the silicon nail test.