Keysight Technologies

W2309EP/ET DDR Bus Simulator and W2317EP/ET DDR Bus Simulator Distributed Computing 8-pack

Data Sheet

Introduction

The W2309EP/ET double data rate (DDR) Bus Simulator quickly generates accurate bit-error-rate (BER) contours, masks, and margins between the two, for the DDR4 memory bus specification published by the JEDEC Solid State Technology Association.

The simulator achieves this by use of statistical simulation, meaning no lengthy and time-consuming bit pattern is needed. Instead, it constructs the eye diagram from the transmitter, channel, and receiver impulse responses, and from the stochastic properties of a conceptually infinite non-repeating bit pattern. In doing so, it avoids the pitfalls associated with precarious dual-Dirac extrapolation of a limited bit pattern from either SPICE-like simulation or from convolutional channel simulation.

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Key Features

- Rigorous DQ and DQS eye calculations to arbitrarily low BER levels
- Built-in driver de-emphasis and receiver continuous-time-linear-equalizer models
- Mix-and-match between built-in, IBIS and circuit models of driver and receiver
- Accounts for crosstalk between signal lines
- Captures asymmetry between rise and fall edges
- Comprehensive margin measurements versus JEDEC DDR4 Rx mask at target BER
- Batch simulation for design space exploration and design of experiments
- Optional parameter sweeps on a compute cluster

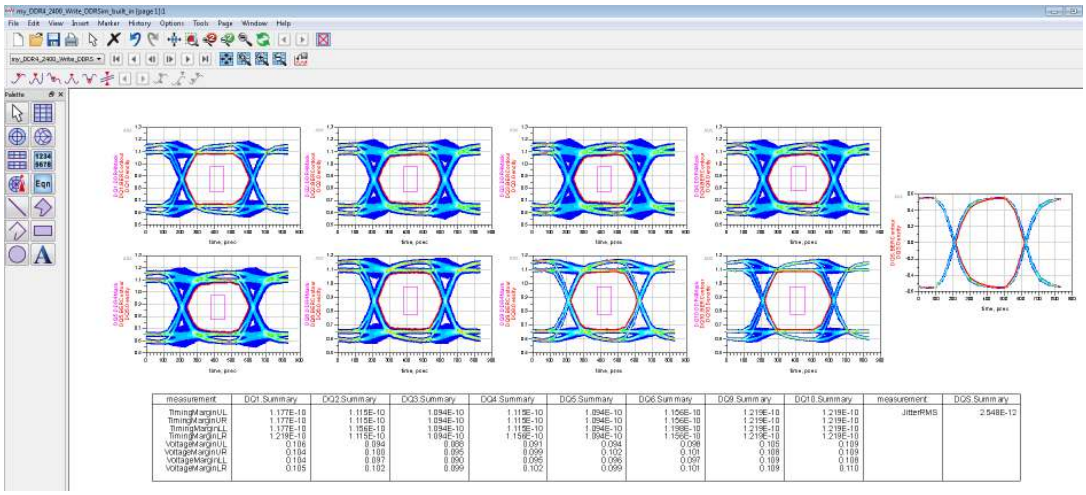

Figure 1. Eye diagrams for a byte lane.

Speed Up Simulation Time

Individual simulations are fast so designers can run in batch mode to quickly explore the design space. An additional product, the W2317EP/ET DDR Bus Simulator Distributed Computing 8-pack, enables you to farm out parameter sweeps to a compute cluster.

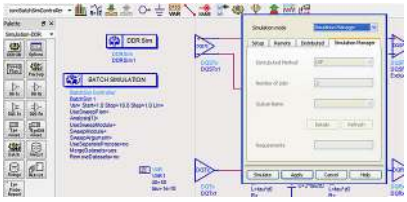

Figure 2. DDR batch simulation.

Rigorous DQ and DQS Eye Calculations

The DDR Bus Simulator offers rigorous DQ (DDR Data Input/Output) and DQS (DDR Data Strobe) eye calculations to arbitrarily low BER levels, including the 1E-16 contour specified by JEDEC, accounting for crosstalk and for asymmetry between rising and falling transition times. It provides comprehensive timing and voltage margins between the selected BER contour and the DDR4 receive mask specification.

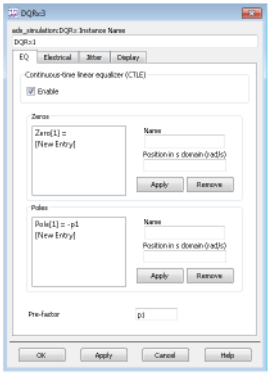

Figure 3. The built-in transmitter includes an optional pre-emphasis.

Mix-and-Match between Built-in, IBIS and Circuit Models

The product allows for three IC model types: built-in, Input/output Buffer Information Specification (IBIS), or circuit models. The built-in driver and receiver model de-emphasis and continuous-time linear equalization (CTLE), respectively. Designers can “mix-and-match” model types in their schematic.

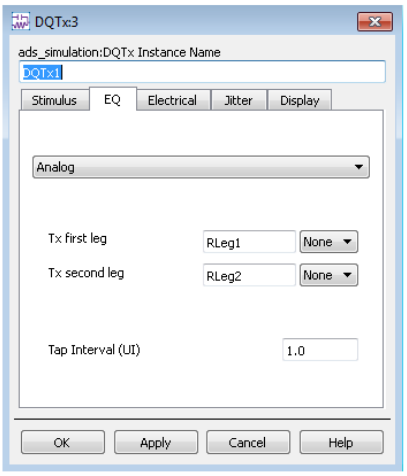

Figure 4. The built-in receiver includes CTLE capability.

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