Keysight Technologies
Using an Infinium V-Series Mixed-Signal Oscilloscope to Debug and Validate DDR4/LPDDR4 Signals

Application Note
Introduction

With increasing data rate speeds, more complex testing methodology, and shrinking margins, memory designers and engineers face new challenges when debugging and validating their memory designs. The JEDEC LPDDR4 specification has a maximum data rate of 4266 MT/s, requiring you to pay more attention to high-speed signal integrity issues. The complex testing methodologies included in both the DDR4 and LPDDR4 specifications require more than the standard setup and hold time measurements commonly used for testing. Smaller margins mean you must venture through bit error rate (BER) measurements when validating eye margins to ensure compliance.

This application notes describes how you can meet these challenges and make fast, accurate DDR4/LPDDR4 measurements by using a Keysight Infinium Mixed-Signal Oscilloscope (MSO).

Using an MSO to Separate Read and Write Data

The JEDEC standard requires you to separate read and write data to perform data validation. With the DDR4 JEDEC specification, you need to perform tests on eye diagrams with different masks to ensure you have a wide enough margin window for error-free data transfer. These tests are Rx timing window (TdlVW) and Rx mask voltage (VdlVW). To complete these measurements, you must first be able to separate the read and write data.

Unlike most serial standards, in DDR both the reads and writes travel across the bus at the same time. You must therefore know which piece of data is related to reads and which is related to writes. In the previous DDR3 technology you could separate writes from reads by knowing that read and write burst preamble patterns are different. Read preamble pattern goes from hi-Z state to low state for about a quarter to half clock cycle before data starts to transition, while write preamble pattern goes from hi-Z to one clock cycle before data starts to transition. For DDR3 engineers, the preamble difference makes identifying the read and write cycles fairly easy. In DDR4, however, both the read and write cycles have the same preamble pattern, which is one clock cycle on the burst (DQS) before data (DQ) transitions. DQ remains in high state when it is not clocked by DQS. To separate the reads and writes in DDR4, you must look at the DQS-DQ phase difference. On a write cycle, DQS is center-aligned with DQ. On a read cycle, DQS is edge-aligned with DQ.
Problems may occur on the DQS-DQ phase because signal integrity issues at high-speed data rates often create alignment issues. If the phase is not precisely edge-aligned with DQS, read data may be mistaken for write data. If the phase is not center-aligned, write data may be mistaken for read data. These issues can make it difficult to correctly identify the read and write cycles.

One potential solution to this alignment issue is to program a specific read-only or write-only data pattern to be sent to the memory devices so you can be sure you are only testing read or write data and not having to perform read and write separation work. However, you would need to have access to and control over the memory controller, and the expertise to reprogram it. The only other option is to use the command truth table of the JEDEC specification to tell if it is read or write data. The command truth table uses logic from CS, RAS, CAS, and WE signals to decode the read or write command protocol. Logic analyzers and protocol analyzers can probe these digital channels, but they lack the analog view that an oscilloscope provides. Specifically, using an MSO is an efficient way to perform parametric or physical layer testing. The Infiniium V-Series MSO models have 16 digital channels and 4 analog channels, so you can use the digital channels to probe the command signals and analog channels to look at the analog behavior of CLK, DQS, and DQ.
Decoding the DDR Commands

Another way an Infinium MSO model can help you is by ensuring that you can accurately characterize the start of the burst of the read or write data. Read and write data has latency, meaning it transitions after a certain amount of clock cycles. A normal command trigger would place the trigger point at the start of the command rather than where the actual read or write begins. Keysight’s V-Series MSO technology has built-in protocol decode software to decode the DDR commands so you do not need to build your own symbol file, which takes time and can cause inaccuracies. For example, Keysight’s MSOV334A model has DDR protocol trigger capability that allows the trigger to be placed at the start of the burst of the corresponding read or write data. With an MSO model you can now make accurate timing and eye diagram measurements without having to make a symbol file.
Creating a Real-Time Eye with an MSO

You likely use real-time eyes to validate the data valid window. A predefined mask in the JEDEC DDR4 specification is used to ensure there is no write data corruption, built from the TdIVW and VdIVW specification. This mask testing is new to DDR4 technologies. With the increased speed of DDR4, a traditional setup and hold time measurement is no longer sufficient to characterize write data, and setting up the eye diagram measurement is complicated in a DDR4 system. DQS is a bursty clock, causing idle states where data is not transitioning yet gets folded into the eye. Therefore, if you are trying to set up the real-time eye to include the entire oscilloscope acquisition, the eye may appear invalid. Likewise, if the start of the burst is not properly set to be after the one clock cycle of preamble pattern, you would be folding the data in the preamble state where DQ would still be in high state. Both scenarios would cause a decrease of the margin on VdIVW measurement.

By using the horizontal gating math function of a V-Series MSO model, you can set the real-time eye correctly. The horizontal gating function let you gate the measurement based on the start and end of the write burst, which eliminates the idle states and the preamble states. You can now turn on eye diagrams using the gated DQS as the explicit clock and gated DQ as the data to build the eye diagram. You can also add a mask to the eye to perform mask testing. If a violation occurs, you can unfold the eye diagram and navigate to the waveform where it violates the mask to perform electrical or timing measurements to determine the root cause.
Testing Faster and More Efficiently with DDR Compliance Test Software

Given the variety of software tools available, you can perform DDR test, debug, and characterization quickly and efficiently. With the automated DDR compliance test software available with the V-Series MSO models you can automate all the tests in accordance with the JEDEC standard. The V-Series models also have a simulation tool so you can model the memory controller, memory device, and transmission lines for optimal performance. With the complexity of designing at higher speeds, you may need to perform simulations before releasing a design for board fabrication. Then you have the challenge of correlating the simulation results with the actual device by testing on a common platform for easier debugging and characterization.

To ensure compliance and characterize margins, you need a way to test the simulated data against the JEDEC specification. With the DDR compliance software you can perform offline testing on both your personal computer and a V-Series oscilloscope with saved waveform files. The saved waveform files can be acquired either by the oscilloscope or from simulation software output. You can run the simulated waveforms on the DDR compliance software to ensure they comply with the JEDEC standard before releasing the design for production. Then, when the actual device is ready for testing, you can correlate the test results you got from live testing with the simulated waveform test results to find the problem areas. This method saves you both money and time.
Summary

As a memory designer or engineer, you face new challenges in designing to ever-increasing data rates. You need to use more complex testing methodologies for verifying a data valid window to ensure accurate and reliable data transfers. You also need a more reliable and efficient method to separate read and write data to make the measurements and ensure they are valid. A Keysight V-Series Infiniium MSO oscilloscope is just what you need to meet all these challenges. It correctly separates reads and writes, so you can be confident that the measurement results are accurate. Along with an interposer to provide signal accessibility, a V-Series MSO provides protocol command decode and trigger functions and accurate eye diagram measurements. Its offline testing capability lets you perform simulations for optimal design, and then correlate test results with live signals so you can quickly find problem areas. Using a Keysight Infiniium mixed-signal oscilloscope saves you time, money, and design cycles, and ultimately gets your new DDR designs to market faster.
Evolving Since 1939

Our unique combination of hardware, software, services, and people can help you reach your next breakthrough. We are unlocking the future of technology. From Hewlett-Packard to Agilent to Keysight.