Physical Layer Validation and Functional Test of DDR4 and LPDDR4 Memory

With the ever-growing demand for more speed, lower power consumption and a smaller footprint, double data rate (DDR) memory technology continues to evolve. Released in 2014, fourth-generation DDR4 and low-power DDR4 (LPDDR4) offer evolutionary improvements in speed, density, power and heat. For developers, interoperability is the overwhelming concern, and validating DDR4 performance requires a wide range of measurements at the physical and protocol layers.

A key test challenge: verifying compliance with the JEDEC specification

Although JEDEC defines the specification, there are no formal verification labs or test centers. As a result, developers must decide on the appropriate procedures, methods and equipment for compliance testing. This presents a variety of challenges in the physical and protocol layers.

Signal integrity is crucial for reliable operation of memory systems. The higher clock rates of DDR4 memory cause issues such as reflections and crosstalk, which cause signal degradation and logic issues.

Testing signal integrity starts with the physical layer, where data is transferred on both the rising and falling clock edges. The JEDEC standards require input and output measurements for electrical, timing and eye-diagram tests, and this yields an extensive list of testing operations that ensure correct, error-free operation.

The increase in memory speed has several consequences for functional testing and validation, as well. An upsurge in random jitter is one result, which will cause the data-valid window to shrink. Another outcome is shorter clock cycles, which translates to a smaller jitter budget, thereby making jitter reduction quite complex.

Validating active signals

With faster data rates, margins decrease and error rates increase in DDR4 memory. The DDR4 test requirements address these issues directly.

With an oscilloscope, displaying a captured waveform as a real-time eye (RTE) offers insights into jitter within serial data signals. By showing when bits are valid (high or low), the RTE provides a composite picture of physical-layer characteristics such as peak-to-peak edge jitter and noise. Although this is not a required test, eye height and width provide an easy way to check signal integrity and estimate the data-valid window.

Getting full insights into the data-valid window and expectations of bit failure requires measurements of the worst-case margins in timing (tDIVW) and voltage (vDIVW). This is done using eye diagram mask testing (Figure 1).

FIGURE 1. Eye diagram mask testing ensures that signals are not violating the bounds of the mask, where jitter and errors can occur.
Performing functional testing and validation

Generally, a logic analyzer is used to view timing relationships among many signals. Using a logic analyzer to follow signal flow in DDR4 and LPDDR4 memory offers complete insight into the actual behavior of a memory system. To accurately capture data on a bus, the analyzer’s setup/hold time must fit within the data-valid window of the signal being sampled. Because the location of the data-valid window relative to the bus clock is different for each type of bus, the position of the setup/hold window must be adjustable relative to the sampling clock, with fine resolution, within the data-valid window.

Validating essential system activities

After inspecting individual DDR4 signals, developers should validate three essential activities in the system: that it’s sending the correct DDR commands; that it’s properly addressing memory banks; and that it’s not creating any protocol violations.

Keysight logic analyzers combine reliable data capture with powerful analysis and validation tools that enable DDR4 developers to quickly and confidently validate and debug high-speed digital designs operating at up to 4 Gb/s with eye openings as small as 100 ps by 100 mV. The Keysight U4154B logic analyzer also features a DDR setup assistant that includes time-saving trigger features optimized for DDR measurements (Figure 2).

Gaining a competitive advantage

As an active member of the JEDEC standards committee, Keysight is better able to incorporate the latest solutions for compliance testing into our oscilloscopes and logic analyzers. This helps developers gain deeper insights earlier in the design cycle and offers opportunities to take corrective action sooner. Ultimately, this also helps meet goals for product quality, interoperability and time-to-market.

![FIGURE 2. The Keysight U4154B logic analyzer burst trigger feature helps you achieve greater insight faster when working with DDR memory.](image-url)